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DESIGN OF AN OPTIMIZED CIC COMPENSATION FILTER USING A FIR FILTER BASED ON CSD GROUPING

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Abstract

In high-speed signal processing, the multirate transformation is a widely used method for decimation and interpolation. The comb-based decimation filters with low complexity and strong alias rejection are preferably used in wireless applications. A linear phase FIR filter namely a cascaded-integrator-comb (CIC) filter can be used as a decimation filter. Since this filter doesn't contain a multiplier, it occupies less area and has a higher speed than other decimation filters. In digital systems, the redundant number system is frequently used to enhance the computational efficiency, which can then be further improved by an architectural change made at the circuit level. However, the frequency characteristics are also optimized by reducing the passband droop and increasing attenuation in the folding band using a compensation FIR filter. In this paper, a design of a CIC filter by using a signed digit (SD) number system-based compensation filter has been proposed and analyzed. The analysis of delay and hardware requirements in filter operation was performed. The results show improvements in average operating frequency and a reduction in LUTs of 12.32% and 15.65%, respectively, in comparison to other techniques. Further, the analysis of frequency characteristics of the proposed filter design shows that the average passband droop is reduced by 24.60% and attenuation in the folding band is increased by 22.01% in comparison to binary based filter structures.

Keywords:

Cascaded-Integrator-Comb (CIC) filter, Canonic Signed Digit (CSD), Common Sub-expression Elimination (CSE), Grouping Methods, Sample rate converter (SCR)

1. INTRODUCTION

Real time digital signal processing (DSP) systems are being used more frequently because of the development of artificial intelligence (AI) and machine learning (ML)-based applications in different fields, including multimedia, speech processing, medical imaging, wireless communication, and software-defined radio. Data processing at more than one sampling rate is required in many digital signal processing applications. In multimedia application, the filter operation must have the ability to work at a high frequency. While in other applications, such as cellular telephones, the circuit needs to consume low power at high throughput. The sampling rate conversion process arises the spectral aliasing and spectral imaging during signal processing. Moreover, digital system process on a signal with a larger nyquist interval requires more computations. Therefore, it is desirable to design a filter with a narrow band which efficiently decimates or interpolates the incoming signals. Multirate and multistage implementation of the digital system can result in a significant computational saving over single rate processing with a small nyquist interval. Thus multirate processing is essential to realize the sampling rate conversion efficiently in modern digital signal processing.

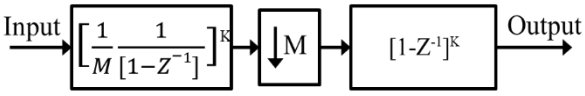

Fig.1. Block diagram of CIC filter structure

There are several benefits of a fast sampling rate that include the capability to digitize large band signals, less complexity of anti-alias filter operation and low noise power. The basic building blocks of a sample rate conversion process are decimation and interpolation filters. The decimation filter is a sample rate converter that also downsamples and provides low-pass filtering. As a result, it is frequently employed in audio processing and wireless applications. In the decimation filter, a cascaded integrator comb filter is used for oversampled ADC due to its high efficiency despite its simple structure. The computational efficiency is high because all filter coefficients are 1 and it performs the multiplier-less operation. It consists of only adder and delays elements that consume less power in operation. The CIC filter is comprised of two sections: a cascaded integrator and a comb that are connected by a down sampler as illustrated in Fig.1. In this structure, the integrator part operates at a high data rate and the differentiator part at a low data rate. Thus, it consumes less chip space and has low power consumption. However, the frequency response of the filter structure exhibits significant passband droop and low folding band attenuation, which is unfavorable in several applications. To overcome these issues, a compensation filter can be used with CIC structure to improve its spectral characteristics. There is several compensation techniques presented in the current research. Details are mentioned in the next section.

In this paper, a multistage compensated CIC decimation filter is proposed. The decimation factor is divided into two stages of decimation in a nonrecursive structure. This multistage is performed at a low sampling rate to minimise the computational load on the filter operation. The compensation filter is cascaded with two-stage CIC filter as shown in Fig.6. In this way, the magnitude response is significantly improved by decreasing passband droop in the wideband and increasing the attenuation in the stopband of the comb filter. Since the frequency characteristics of the compensation filter are the opposite of those of the CIC filter, it provides the sharp transition band and compensates for the passband drop of the CIC filter. In the compensation section, it is hereby proposed to use the FIR filter which is based on a redundant number. This filter is used to speed up the arithmetic computation. Thus, the proposed CIC compensation filter structure based on a signed digit number system is an efficient method to speed up the filter operation with low power consumption and improved magnitude characteristic.

The rest of the paper is organized as follows. Section 2 describes the details of the literature review. The CIC filter and CSD-based FIR filter are illustrated in Section 3. CSD grouping

based compensation method in the CIC decimation filter is outlined in section 4. The proposed approach to design compensated CIC filter is explained in section 5. The evaluation of results and discussion are shown in section 6. The conclusion of the paper is mentioned in Section 7.

2. RELATED WORK

In the last decade, the CIC filter design has drawn interest due to its numerous applications in many different domains, like digital signal processing and wireless systems. Several implementation techniques for CIC filters have been presented in the literature. However, techniques for designing an efficient filter with reduced passband ripple and improved attenuation in the stopband remain an important issue. Mondal et al. [1] suggested the modified CIC filter structure to enhance the performance of the sample rate converter (SRC). The complexity of the proposed filter design is reduced in comparison with traditional CIC filter. The spread of delays in the CIC filter comb stages forms a novel design for the CIC filter functions [2-5]. For the processing of wideband signals, a technique for global optimization of the SCIC filter without multiplier based on the maximization of minimum stopband attenuation is presented [6]. The three-section of CIC filter design with decimation followed by a 128-tap multichannel FIR decimation is presented for sample rate conversion as an input signal of 70 MHz to 137 kHz. [7]. A multiplier-free cosine-based compensator without integrator and having three adders is proposed [8] that provides a better compensation at a high input rate and has a simple structure. This structure has strong stopband attenuation and a low passband ripple. A. Abinaya et al. [9] introduced a CIC filter design that uses several parallel adders. In comparison to the existing compensated CIC filter, the suggested CIC design employs a new polynomial approach that reduces stopband attenuation by 41.14% and passband droop by 33.33%. In real-time multi-rate signal processing, a CIC filter is designed for digital down-conversion and implemented on FPGA [10]. Garcia Baez et al. [11]-[12] presented a method for improving the comb magnitude characteristics in both the passband and the stopband by combining corrector filters with a cosine-squared filter. An optimized CIC decimation filter is presented that includes a Gain compensator to enhance the magnitude characteristics [13]-[16]. A modified cosine-based decimation filter design with large stopband attenuation than conventional filters has been proposed [17]. The common subexpression in a CSD based filter operation is eliminated, which reduces the complexity of the FIR filter. To reduce the computation required for filter operation, a grouping approach for the CSD based filter coefficient has been devised [18-21]. Dolecek and Laddomada [22]-[23] introduced a class of decimation filters with a cascade of two cosine filters at a high input rate to improve alias rejection in the comb folding bands. The alias rejection is optimized by introducing cosine filters into an appropriate stage of a comb structure. The placement of cosine filters in the structure results in a tradeoff between alias rejection improvement and hardware resources.

3. CIC FILTER AND CSD BASED FIR FILTER

The basic definitions of the terms in context of the subject are given below,

3.1 CIC FILTER

The CIC filter includes two blocks of N stage each namely integrator and comb section. The transfer function can be expressed as given below.

Integrator section:

$$H_1[z]=\left(\frac{1}{1-z^{-1}}\right)^N \text{ c} \tag{1}$$

Comb section:

$$H_2[z]=\left(1-z^{-DM}\right)^N \tag{2}$$

The transfer function of the resulting filter can be represented as given below.

$$H_{CIC}[z]=\left[\frac{1-z^{-DM}}{1-z^{-1}}\right]^N \tag{3}$$

where *M* and *N* are the parameters for the number of samples per stage and the total number of filter stages, respectively. Here, there is only one sample at each stage and *D* is the decimation ratio. The Eq.(3) can be rearranged as:

$$H_{CIC}[z]=\left[\frac{1}{D}\cdot\frac{1-z^{-D}}{1-z^{-1}}\right]^N \tag{4}$$

The transfer function of two-stage CIC filter can be written as:

$$H_{CIC}[z]=\left[\frac{1}{D_1}\cdot\frac{1-z^{-D}}{1-z^{-1}}\right]^N\cdot\left[\frac{1}{4}\cdot\frac{1-z^{-D}}{1-z^{-D_1}}\right]^N \tag{5}$$

$$H_{CIC}[z]=H_1^N[z]\cdot H_2^N[z] \tag{6}$$

where,

$$H_1^N[z]=\left[\frac{1}{D_1}\cdot\frac{1-z^{-D}}{1-z^{-1}}\right]^N \tag{7}$$

$$H_2^N[z]=\left[\frac{1}{4}\cdot\left(1-z^{-D_1}\right)\left(1-z^{-2D_1}\right)\right]^N \tag{8}$$

Here $H_1^N[z]$ and $H_2^N[z]$ are two CIC filters with decimation factor D_1. The first section of CIC filter with decimation factor D_1 operates at the high sample rate and the next section at the lower rate as shown in Fig.2.

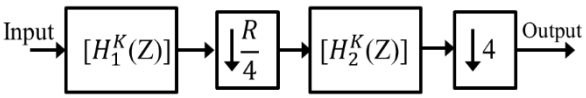

Fig.2. Two stage CIC decimation filter

The frequency response of the CIC filter is presented in exponential form.

$$H_{CIC}\left[z=e^{j\omega}\right]=\left[\frac{\sin\frac{\omega D}{2}}{D\sin\frac{\omega D}{2}}e^{-\frac{j\omega(D-1)}{2}}\right]^N \tag{9}$$

3.2 CSD ARITHMETIC FOR COEFFICIENTS OF COMPENSATION FILTER

The number of additions carried out in a coefficient multiplication for filter operation is generally one less than the total number of nonzero bits present in the filter coefficient, which is a well-known fact. Hence, the filter coefficient can be expressed in a number system with the least number of nonzero bits to minimize the power demands and hardware requirements. The CSD number system is preferred to represent the filter coefficient since it contains the fewest nonzero bits. A CSD representation is a specific case in which the set {1 0 -1} is used to express a radix-2 signed digit.

The coefficient bi in FIR filter can be presented in a CSD number system as given,

$$b_i = \sum_{j=0}^{M_i-1} C_{ij} 2^{-S_{ij}} \tag{10}$$

The transfer function of an N order FIR filter can be expressed as given below.

$$y[n] = \sum_{i=0}^{N-1} b_i x[n-i] \tag{11}$$

where $x[n\text{-}i]$ is the input sampled signal at moment $[n\text{-}i]$, $y[n]$ is the output signal, N is the order of the filter, and b_i is the filter coefficient of the i^{th} order. As a result, Eq.(11) might be rearranged as:

$$y[n] = \sum_{i=0}^{N-1} C_{ij} 2^{-S_{ij}} x[n-i] \tag{12}$$

where M_i is the total number of bits that are nonzero in the coefficients b_i and $S_{ij} \in \{0,..W\text{-}1\}$, $C_{ij} \in \{1\ 0\ \text{-}1\}$ where W represents the word length of the quantized coefficient. The complexity of the FIR filter is further simplified by applying a CSD number system based on common subexpression elimination in the design process, as discussed in the next section.

4. CSD GROUPING BASED COMPENSATION METHOD IN CIC DECIMATION FILTER

In the design of a decimation filter, the magnitude response is an important consideration. The output of a multistage CIC decimation filter is not directly applicable for real-time applications and requires an appropriate filter design parameter to ensure that the signal waveform remains stable. However, the magnitude response of this filter structure presents high ripple in the passband and low stopband attenuation bands which is undesirable.

To overcome the problem of large passband distortion and low stopband attenuation of conventional CIC filter, the compensation filter can be cascaded with CIC structure to improve its spectral characteristics. There are two types of compensation filter that are used viz. cosine filter and gain compensation filter. The cosine filter increases the attenuation in the folding band whereas a gain compensation filter is used to suppress the passband droop.

4.1 COMPUTATIONALLY EFFICIENT COMPENSATION FILTER

The magnitude characteristics of the FIR filter are basically the inverse of the CIC filter. Thus, it provides the sharp transition band and compensates the ripple in the passband of the CIC filter. Therefore, a FIR filter based on a redundant number system is used as a compensation section. This proposed structure based on arithmetic operations using a signed digit number system may be used as a method to speed up the filter operation and low power consumption with improved magnitude characteristics.

4.2 GROUPING IN CSD COEFFICIENTS OF COMPENSATION FILTER

A new approach for eliminating the common subexpression method for CSD representation-based filter coefficients by grouping method has been described [1]. The fundamental goal of this approach was to identify and eliminate redundant computation in filter operations. However, the CSD representation of the coefficient is more widely used since it has around 30% fewer nonzero bits than the binary representation of the filter coefficient [16]. Thus, less hardware resource is required to implement the CSD coefficient multiplier as compared to binary representation. The number of adders and subtractors in the realization of the coefficient multiplier in filter operation has been further decreased by the grouping approach in the filter coefficient. This grouping technique is used to enhance the computational efficiency using hardware sharing structure by removing the repeated computation in filter operations as shown in Fig.3. The flowchart for grouping technique of the CSD number based 16 bit quantized coefficient of FIR filter bi can be separated into three common subexpressions e.g. i) [10-1] ii) [100-1] and iii) [101].

In the redundant operation of multiple constant multiplications, the subexpression elimination of a common variable can be employed. This filter design comprises a pre-processing subsection and a cascade of identical filter sections depending on the order of the filter.

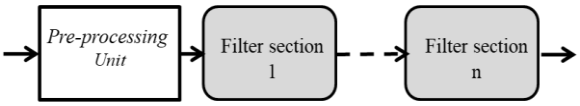

Fig.3. Compensation FIR filter with CSD grouping.

As shown in Fig.5, the preprocessing unit functions as a common computing engine to produce the partial product of common subexpressions suggested in the grouping process. The filter section is used to further process the partial product produced by the pre-processing unit. These precomputed terms Y1, Y2, Y3, Y4, and Y5 are fed to the corresponding five buses in the filter section. Thus, the preprocessing unit and filter section are used to generate the filter output.

This proposed compensation filter is cascaded with a two-stage CIC structure to improve the magnitude response by the reduction in passband ripple in the wideband and increase the attenuation in the folding band of the comb filter. It can be used to reduce the computation time in the lower bound on the clock period of the circuit.

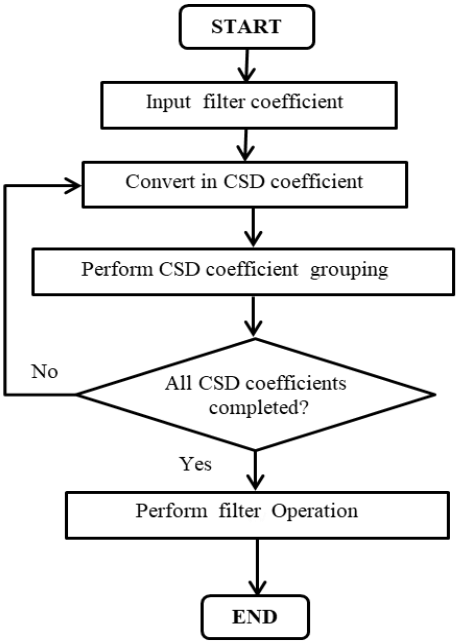

Fig.4. Flowchart of CSD coefficient grouping in filter operation

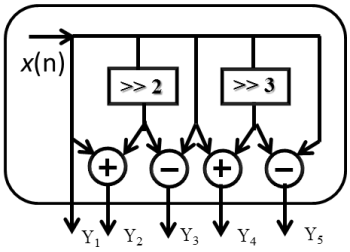

Fig.5. Layout of pre-processing unit

5. PROPOSED APPROACH TO DESIGN COMPENSATED CIC FILTER

As discussed in section 2, the multiplier-less CIC decimation filter provides high performance about sampling rate conversion and hardware complexity than other digital filters. It consists of only adders and delays elements that consume less power in filter operation. Whereas the magnitude response of this filter structure has a high passband droop and low attenuation in folding bands, which is undesirable. To design an efficient compensator filter to significantly improve the frequency response by decreasing passband droop and attenuation in the folding band, we follow the design steps as,

- The two-stage (K=2) CIC filter with a decimation factor of 4 to 16 is considered as a basic decimation filter.
- To overcome the problem arising from the number of cascaded CIC filters and to improve the frequency characteristic, the CSD-based FIR filter is introduced with two-stage CIC filter as illustrated in Fig.6. A linear phase FIR filter with a symmetrical architecture is used as a compensator. It has a logic unit to reduce computation complexity in filter operations by using CSD number system-based filter coefficients. This unit performs as a computation engine, generating the intermediate result during the filter operation.
- The performance of proposed filter design is analyzed by varying number of sections in CIC filter design and result is mentioned in next section.

This modified structure by using a combination of two-stage CIC filter and compensation filter based on CSD grouping method in filter operation is optimized for the overall performance parameter in terms of the delay, hardware utilization and frequency characteristic and compared to binary based CIC compensation structure.

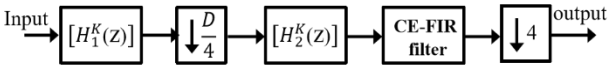

Fig.6. Proposed compensated CIC filter

Table.1. Sample Filter specification

Sample CIC filter	**Specifications**
Filter Structure Input word length 16 bits Number of Sections 2-32	CIC Decimator
Decimation Factor	4-16
Input word length	16 bits
Number of Sections	2-32
Compensator filter	
Filter Structure	FIR Filter
Filter Order	4
Transition Band $\lvert\omega_s - \omega_p\rvert$	0.01
Used Number System	CSD Representation

Table.2. Comparison of passband ripple and stopband attenuation with compensator filter

Number of sections	**Without Compensator filter**		**With Compensator filter**		**Ratio-I With CIC/Comp-CIC**	**Ratio-II With CIC-Comp/CIC**
	Passband ripple	**Stopband attenuation**	**Passband ripple**	**Stopband attenuation**		
4	0.087	45.96	0.070	56.18	24.28%	22.23%
8	0.090	45.28	0.074	55.71	21.60%	23.03%
16	0.096	44.36	0.078	53.84	23.07%	21.37%
32	0.110	43.40	0.085	52.70	29.41%	21.42%
Average reduction in passband ripple and improvement in stopband attenuation by					**24.60%**	**22.01%**

6. IMPLEMENTATION RESULTS

The proposed compensated CIC filter with a FIR filter is synthesized through the FPGA family: Virtex-4, Package-SF363 and Device: XC4vFx. This logic family is popular due to its high packing levels and low dynamic power demands. The number of sections in the proposed filter design varied from 2 to 32 and decimation ratio varied from 4 -16, with a small transition band between the passband and stopband frequencies in normalized

mode ω_p and ω_s respectively. The complexity parameters such as hardware resource and delay are extracted and compared.

6.1 COMPARISON OF PASSBAND RIPPLE AND STOPBAND ATTENUATION

The frequency characteristic of proposed CIC compensated filter is analysed and compared with conventional CIC filter as illustrated in Fig.7 to Fig.9. The average Passband ripple and Stopband attenuation in the suggested filter design for small transition region as ω_s-ω_p ranging for 0.01π to 0.05π is lowered by 24.60% and attenuation increased by 22.01% respectively when compared to filter design without compensation filter as shown in Table.1.

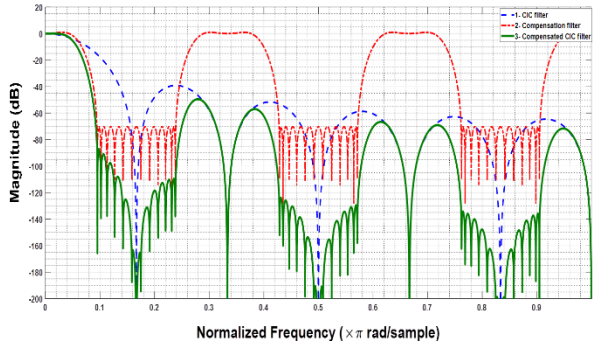

Fig.7. Overall gain response of proposed filter design

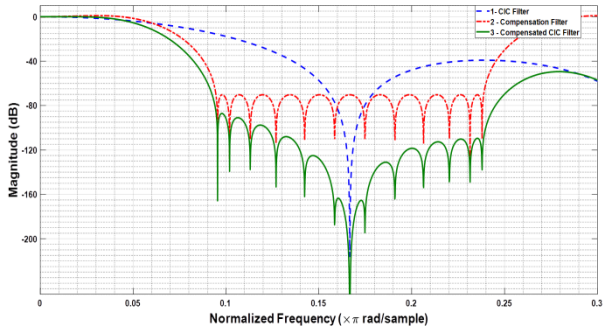

Fig.8. Stopband zoom of gain response

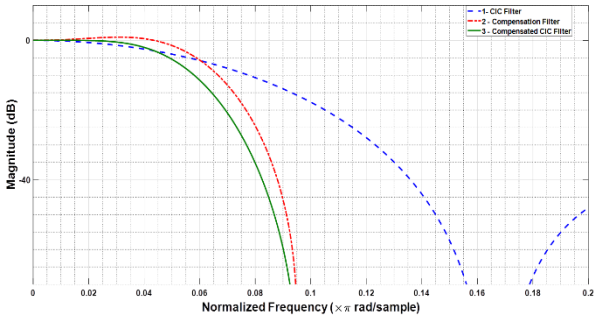

Fig.9. Passband zoom of gain response

6.2 COMPARISON OF NUMBER OF LUTS UTILIZED

The proposed CIC filter with a CSD-based FIR filter is compared with that based on a binary compensation filter for the number of LUTs utilized. The result shows a reduction of 15.65% as mentioned in Table.3.

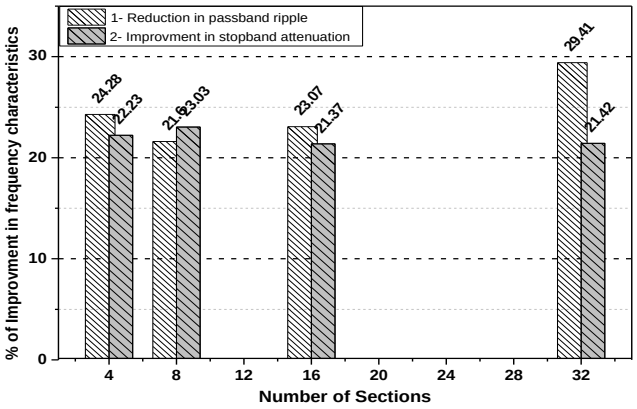

Fig.10. Improvement in frequency characteristics

Table.3. Comparison of Number of LUTs utilized in filter.

Number of section	Compensated CIC filter with binary num	Proposed Compensated CIC filter with CSD grouping	Ratio-I with Binary/ Proposed
4	7237	6142	17.82%
8	7368	6391	15.28%
16	7652	6613	15.71%
32	7790	6845	13.80%
Average number of LUTs reduce by			15.46%

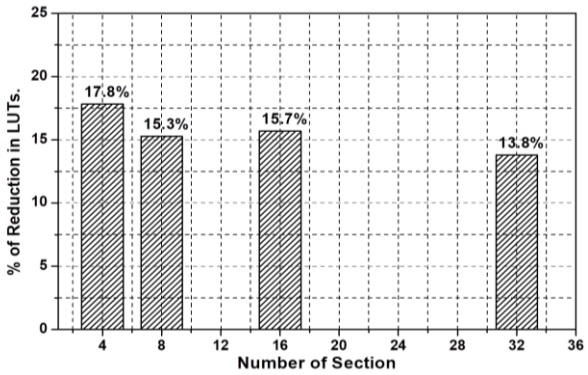

Fig.11. Comparison of average LUTs utilized with no. of sections

6.3 COMPARISON OF AVERAGE MAXIMUM FREQUENCY

The comparison of the average maximum frequency of the proposed compensated CIC filter with its binary counterparts is illustrated in Fig.12.

Table.4. Comparison of maximum frequency in filter operation

Number of sections	Compensated CIC filter with binary (MHz)	Proposed Compensated CIC filter with CSD grouping (MHz)	Ratio-I with binary/ Proposed
4	20.89	22.67	8.52%

8	19.16	21.63	12.89%
16	17.52	19.50	11.30%
32	15.31	17.85	16.42%
Average maximum frequency increased to			12.32%

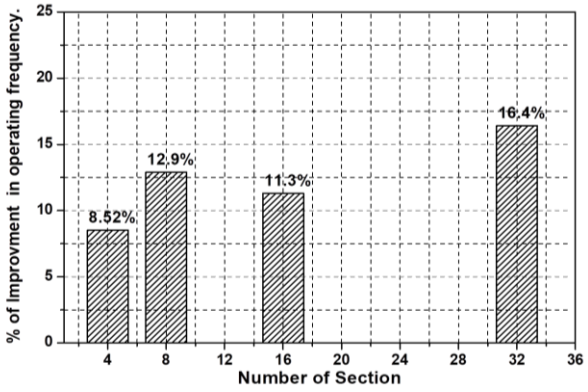

Fig.12. Comparison of average maximum frequency

The average maximum frequency of the proposed filter design is improved by 12.32% when compared to the binary coefficient-based filter design which implies that the number of computations in filter operation is significantly decreased. The results are shown in Table.4.

7. CONCLUSION

A CIC compensation filter was designed using an FIR filter based on CSD grouping and the performance was analyzed in comparison to binary based CIC compensation filter. The results of the simulation demonstrate that the average passband droop is reduced by 24.60% and stopband attenuation is increased by 22.01% for the suggested filter design. In addition, the average number of LUTs utilized is reduced by 15.65% in comparison to the binary based compensated CIC filter. The average maximum frequency is also improved by 12.32%. Thus, the performance of compensated CIC filter is improved in terms of hardware resources and speed of operation. Therefore, it can be concluded that the proposed design of a CIC filter with an FIR filter based on CSD grouping is a viable alternative to improve the performance of compensated CIC filter.

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