DOI: 10.21917/ijme.2022.0234

# PULSE WIDTH MODULATOR USING OTRA BASED TIMER CIRCUIT

**Dheeraj Singh Rajput[1], Ritu Gupta[2], Sankalp Shukla[3] and Deep Kishore Parsediya[4]**

[1,2,3]*Department of Electronics and Communication Engineering, Indira Gandhi Engineering College, India*

[4]*Department of Electronics and Communication Engineering, Madhav Institute of Technology and Science, India*

***Abstract***

***This paper proposes a modified PWM circuit using OTRA based analog timer circuit. Designing a pulse width modulator circuit by employing the proposed analog timer circuit results in a waveform having variable duty cycle and time period. The timer circuit consists of comparators designed using OTRA and flip flops. The fabrication of timer circuit on a monolithic integrated circuit is easier as the carrier signal type is exponential and no additional circuitry is needed unlike for triangular and sawtooth pulses. The process parameters of 0.5 µm CMOS have been used for performing an intensive simulation of the proposed PWM circuit.***

***Keywords:***

***Timer Circuit, Pulse Width Modulator (PWM), OTRA, Flip-Flop***

## 1. INTRODUCTION

Analog Signal processing is irreplaceable in today's world as all real signals are analog in nature. In fact, for digital processing also, we need analog blocks to convert analog signal to digital signals like data convertors, voltage oscillators etc. Recently current mode analog signal processing has captured attention of scientific community due to its ability to curtail voltage swings which results in an improved capability to handle signals particularly at low power supply. This makes it a viable option to employ in mixed signal design circuits functioning at 3.0 Volts supply voltage, which in near future, is expected to be a standard value for the CMOS industry.

As technology length shrinks from micron to submicron region, the supply voltages requirement has also been lowered to 1.5 Volts. At this reduced supply voltage, it is nearly impossible for a voltage mode transistor circuit to be designed which possesses a wide dynamic range and high linearity. In recent times, current mode circuits have substituted voltage mode circuits in most of the future applications due to their inherent advantages over the latter [2].

The timer circuits are being widely employed in the analog industry. Conventionally, op-amp, a voltage mode circuit is being used to design classical analog timers [3]. It has its own limitations as compared to current mode circuits. Voltage mode circuit generally has low slew rate and lower bandwidth as compared to current mode circuits. The constituents of current mode circuits like Current Conveyor, Operational Trans-conductance Amplifier, Current Differential Trans-Conductance Amplifier, Operational Trans-resistance Amplifier etc. have a wider dynamic range and bandwidth. They also have larger linearity than their voltage mode counter parts like op-amps [4].

Therefore, such functional blocks are a better alternative than op-amp for designing of timer circuits [5] [6]. The PWM circuit is extensively used to govern the speed of DC motors [11] [12], manage the power supplied to electrical devices [7]-[10], communication, RADAR detection and so on. In this proposed paper, an OTRA based timer circuit which operates at low voltages has been employed to design pulse width modulator (PWM). Realization of active blocks is extensively discussed in Section 2 and Section 3. The methodology of proposed Pulse Width Modulator is discussed in Section 3. In section 4, we analyze and compare the features and parameters of proposed PWM with other PWMs.

### 1.1 ACTIVE BLOCK - OTRA

OTRA is a current controlled voltage source. It has a large bandwidth, high gain and a high slew rate which is independent of gain. It has no parasitic effects due to its virtually grounded input terminals [15]. Different CMOS structures of OTRA have been surveyed in literature [17,18]. The Fig.1 shows the basic block diagram of OTRA and its output $V_o$ is computed using its port characteristics given in Eq.(1), where $R_m$ is the transresistance gain of OTRA [19].

$$\begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ i_z \end{bmatrix} \quad (1)$$

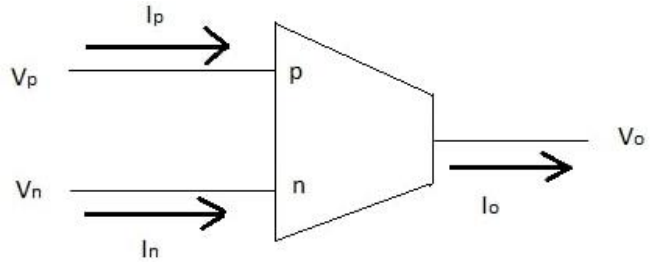


Fig.1. Block diagram of OTRA

The Fig.2 depicts the CMOS structure of OTRA [20]. The cascaded inverter [M15-M18] takes the output of this circuit which provides voltages to $V_{CC}$ and ground respectively.

### 1.2 OTRA BASED TIMER CIRCUIT (CIRCUIT DESCRIPTION)

The OTRA based timer circuit is shown in Fig.3 [27]. It has 2 comparators, namely comp_1 and comp_2, S-R flip-flop, NMOS M1 and multiple resistors [21]. It has 3 input pins, namely, threshold pin, trigger pin, discharge pin, output pin ($V_{out}$) and ground pin. The ground pin is connected to common ground. The function of comparator is to compare the input voltage/ current with the reference voltage/current. In the current work, OTRA is used to design a comparator which compares the current input to the two terminals resulting in an output voltage which may be positive or negative. The inverter takes the output of this circuit, thereby providing voltages to $V_{CC}$ and ground respectively.

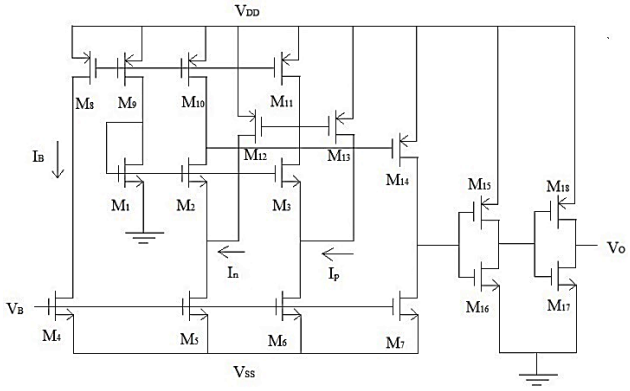


Fig.2. CMOS Realization of OTRA

## 2. PROPOSED PWM CIRCUIT

The Fig.4 shows the proposed PWM circuit. A modulating current signal is applied at input ($I_n$) of comparator_1 (comp_1). The amplitude of modulating signal is less than total current $I_n$. $I_1$ and $I_2$ are defined such that $I_1$ is the current when the amplitude of modulating signal is higher and $I_2$ is current when the amplitude of modulating signal is lower. $I_{total}$ is the total current provided by the power supply.

### 2.1 OPERATION

Initially, the capacitor is in discharge condition, so voltage across the capacitor $C_1$ is zero. The current at *p*-terminal of comparator_1 is zero and at *n*-terminal of comparator_1 is the addition of $2/3*I_{total}$ (due to current divider circuit) and modulating current signal, hence, the output of comparator_1 is zero. Also, the current at *n*-terminal of comparator_2 is zero (since the voltage across the capacitor $C_1$ is zero) and current at *p*-terminal of comparator_2 is $1/3*I_{total}$ due to which output voltage of comparator_2 is $V_{cc}$. Output of comparators in circuit is connected to the S-R flip-flop as shown in Fig.2 (*S* is connected to output of Comparator_1 and *R* is connected to output of Comparator_2), hence, the inputs of S-R flip flop are $S$=0, $R$=1. The output of S-R flip-flop for $S$=0, $R$=1 will be Q=0. This output of S-R flip-flop is connected to the gate of NMOS $M_1$. Due to zero gate voltage, NMOS $M_1$ will be in OFF condition. Capacitor $C_1$ starts charging towards supply voltage $V_{cc}$ through resistors $R_3$ and $R_5$. When capacitor $C_1$ gets charged to such a value that the current through n-terminal of comparator_2 becomes greater than or equal to the current through *p*-terminal, i.e., $1/3*I_{total}$, output of comparator_2 becomes 0 Volt. However, the current through p-terminal of comparator_1 is still less than the addition of $2/3*I_{total}$ and modulating signal and therefore output of comparator_1 is at 0V. Now, the inputs of S-R flip-flop will be $S$=0 and $R$=0. So, the output will remain in its previous state which means $Q$=0. The NMOS $M_1$ is in OFF condition due to which capacitor $C_1$ continues to charge towards a voltage so that the current through p-terminal of comparator_1 becomes more than addition of $2/3*I_{total}$ and modulating signal resulting in its output to become 1. Although, the output of Comparator_2 remains 0V resulting in the S-R flip flop's inputs being $S$=1, $R$=0 and its output will be $Q$= 1. NMOS $M_1$ will now be in ON condition and hence capacitor $C_1$ begins discharging to such a voltage level that the current through the p-terminal of comparator_1 becomes less than the current through n-terminal (i.e., $2/3*I_{total}$). The output of comparator_2 stays unchanged at 0 Volt. So, the flip-flop inputs are now $S$=0, $R$=0 resulting in an unchanged output, i.e., $Q$=1. NMOS $M_1$will now be in ON condition and therefore capacitor $C_1$ keeps discharging to 0V through NMOS $M_1$. As capacitor $C_1$ continues to discharge, at some point of time the current through n-terminal of comparator_2 becomes less than the p-terminal current (i.e., $1/3*I_{total}$) due to which the output of comparator_1 stays unchanged at 0V. Now, the flip flop inputs are S=0, R=1, so its output is in $Q$=0 state. Therefore, NMOS $M_1$ turns OFF and capacitor $C_1$ stops discharging through the NMOS $M_1$ path. Subsequently, the current level at n-terminal of comparator_1 becomes equal to the sum of $2/3*I_{total}$ and modulating current signal resulting in repetition of the same cycle. But the time required for charging and rise in voltage level with charge in capacitor is different which are lesser compared to the values when sinusoidal current was $I_1$. The aforementioned process is repeated continuously with the application of a periodic pulse used for triggering. The waveform obtained at the output of proposed PWM modulator is shown in Fig.10.

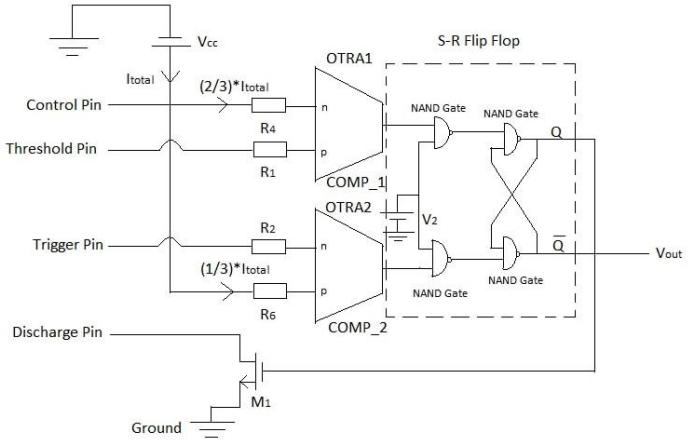


Fig.3. OTRA based timer circuit

## 3. SIMULATION AND EXPERIMENTAL RESULTS

This operation of the PWM modulator being proposed is established by an intensive simulation in SPICE using .5$\mu$m CMOS technology. The timer circuit is constructed using the CMOS structure of OTRA shown in Fig.2. The parameters being used are:

- Supply voltages: ±1.5V
- W/L ratio of NMOS transistor $M_1$ used in timer circuit: 2$\mu$m /100$\mu$m
- W/L ratios of transistors used in the OTRA are $M_{1,2,3}$: 100/2.5, $M_{4,7,12,13}$: 10/2.5, $M_{5,6}$: 30/2.5, $M_{8,11,14}$: 50/0.5

The Table.1 shows the component values being used in the PWM circuit. The duty cycle is calculated using the formula given below:

$$\text{Duty Cycle}=T_{on}/(T_{on}+T_{off}) \quad (1)$$

The Fig.7 shows the voltage across capacitor $C_1$ and Fig.8 shows the output voltage without modulating current signal. In the current PWM circuit, a modulating signal is applied at *n*-terminal of comparator_1 as shown in Fig.4. Applying a modulating signal

with 10KHz frequency results in an output which is shown in Fig.9. Similarly, applying a modulating signal with 20KHz frequency results in an output which is shown in Fig.10. The Fig.11 and Fig.12 show the frequency domain representations for the modulating signal with a frequency of 5 KHz and the output signal respectively. Since the exponential voltage waveform across the capacitor is being used as carrier wave, therefore, no additional circuitry is needed for the triangular/sawtooth waves.

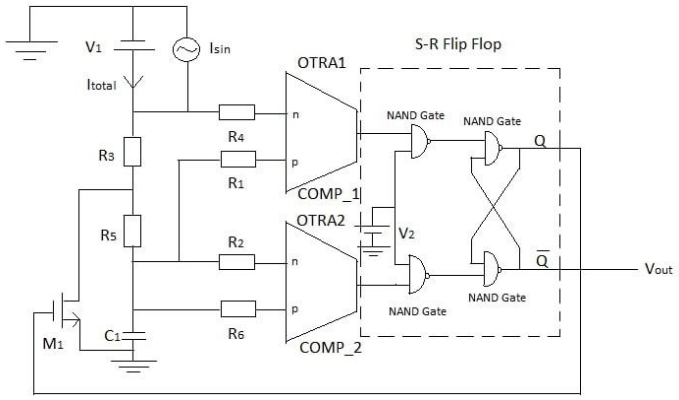


Fig.4. Proposed PWM using OTRA based timer circuit

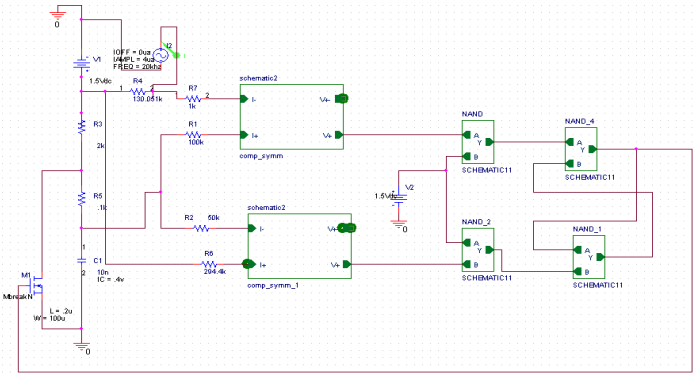

Fig.5. Spice schematic of proposed circuit

Table.1. Component values used in proposed circuit

| Component | Values |
|---|---|
| $R_1$ | 100 kΩ |
| $R_2$ | 50 kΩ |
| $R_3$ | 2 kΩ |
| $R_4$ | 129.68 kΩ |
| $R_5$ | 0.1 kΩ |
| $R_6$ | 294.4 kΩ |
| $R_7$ | 1 kΩ |
| $C_1$ | 100 pF |

Table.2. Comparison of proposed PWM circuit with existing PWM circuits

| Active Components | Passive Components | Carrier Signal | Electronic Tunability |
|---|---|---|---|
| 1 CC-II, 2 op-amps [22] | 1 C, 3 R | Triangular | No |
| 1 op-amp [23] | 1 C, 3 R | Exponential | No |
| 3 Operational Trans-conductance Amplifier [25] | 1 C, 2 R | Triangular | Yes |
| 4 Operational Trans-conductance Amplifier [26] | 1 C | Triangular | Yes |
| Proposed 2 OTRAs, NAND gate-based Flip Flop | 1 C, 6 R | Exponential | Yes |

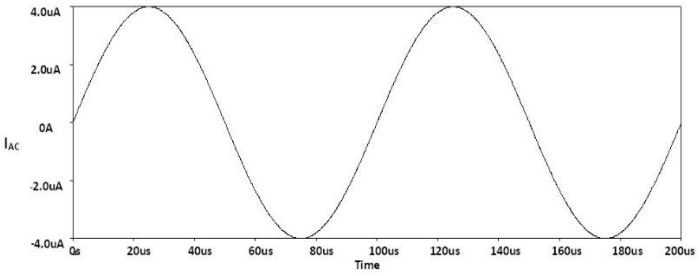


Fig.6. Modulating current signal

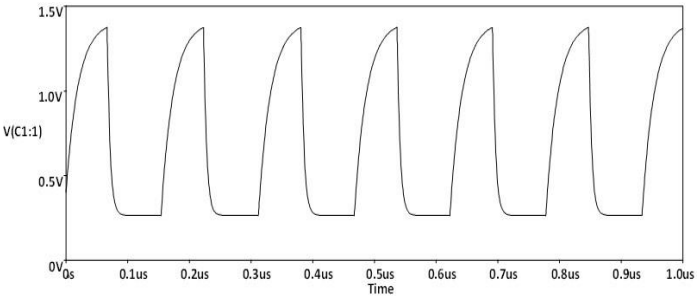


Fig.7. Voltage across capacitor without modulating signal

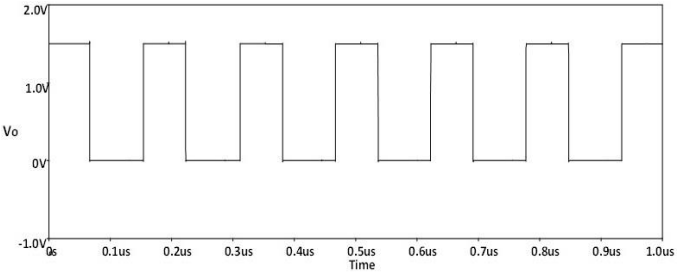


Fig.8. PWM output without modulating signal

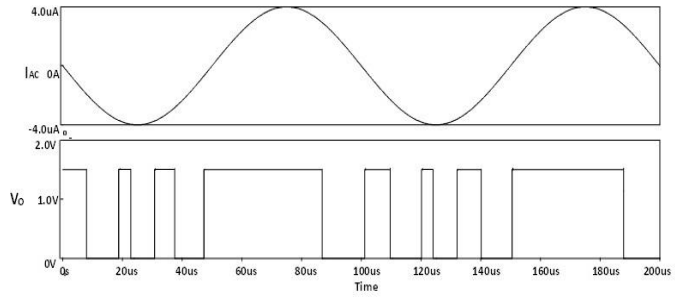


Fig.9. Output of PWM when modulating signal with 10KHz frequency is applied

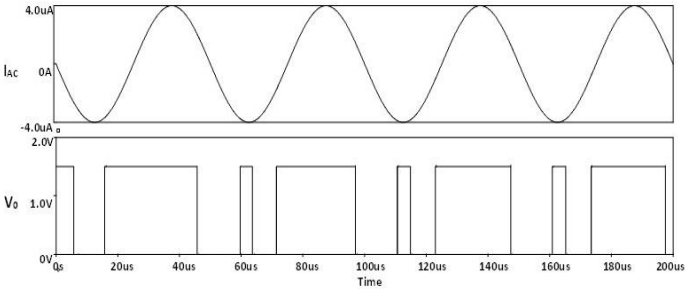


Fig.10. Output of PWM when modulating signal with 20KHz frequency is applied

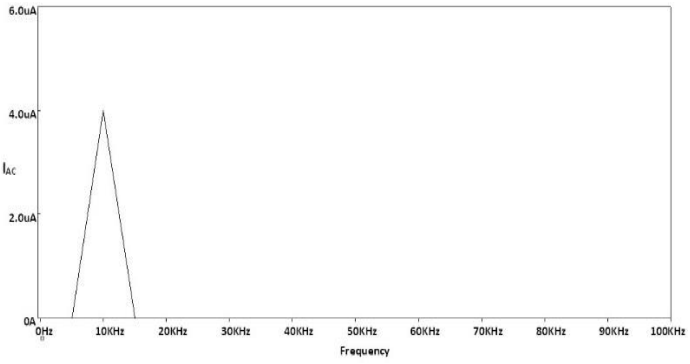


Fig.11. Frequency domain representation of modulating signal

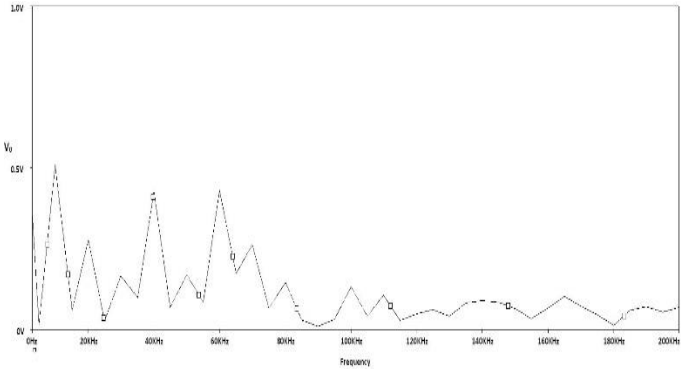


Fig.12. Frequency domain representation of output signal

## 4. COMPARISON

When the proposed work is compared with existing analog pulse width modulator circuits [22]-[26], it is observed that in existing circuits the PWM output is being generated by making a comparison between the reference sawtooth or triangular waveform and the modulating signal. It is also observed in [23] that PWM circuit is designed using op-amp, which is a voltage mode circuit. Voltage mode circuits have their own limitations as compared to current mode circuits. Voltage mode circuit generally has low slew rate and lower bandwidth as compared to current mode circuits.

The proposed circuit is based on current mode circuit, so that the performance does not get degraded for high frequency applications due to limited slew rate and gain-bandwidth product. A detailed comparison of the above fact is shown in Table 2. In addition to this OTRA input terminals are also virtually grounded due to which there are no parasitic effects on the proposed circuit.

## 5. CONCLUSION

This work presents a PWM generator using OTRA based timer circuit by utilizing the non-linear properties of OTRA. It is observed that the proposed circuit performs better as compared to the existing circuits for high frequency switching applications.

## REFERENCES

[1] C. Toumazou, "*Analog IC Design: the Current-Mode Approach*", Peter Peregrinus, 1990.

[2] Franco Sergio, "*Design with Opamp and Analog Integrated Circuits*", McGraw-Hill International, 1988.

[3] J.J. Chen, H.W. Tsao and C.C. Chen, "Operational Transresistance Amplifier using CMOS Technology", *Electronics Letters*, Vol. 28, No. 22, p. 2087-2088, 1992.

[4] Y.K.L.H.C. Chien, "Single OTRA-Based Current-Mode Monostable Multivibrator with Two Triggering Modes and a Reduced Recovery Time", *IET Circuits Devices Systems*, Vol. 1, No. 3, pp. 257-261, 2007.

[5] Yu-Kang Lo and Hung-Chun Chien, "Current-Mode Monostable Multivibrators Using OTRAs", *IEEE Transactions on circuits and Systems-II: Express Briefs*, Vol. 53, No. 11, pp. 1-12, 2006.

[6] J.W. Kolar, H. Ertl and F.C. Zach, "Influence of the Modulation Method on the Conduction and Switching Losses of a PWM Converter System", *IEEE Transactions on Industry Applications*, Vol. 27, No. 6, pp. 1063-1075, 1991.

[7] J.G. Cho, J.A. Sabate, G. Hua and F.C. Lee, "Zero-Voltage and Zero Current-Switching Full Bridge PWM Converter for High-Power Applications", *IEEE Transactions on Power Electronics*, Vol. 11, No. 4, pp. 622-628, 1996.

[8] R. Pongiannan, S. Paramasivam, and Y. Narri, "Dynamically Reconfigurable PWM Controller for Three-Phase Voltage-Source Inverters", *IEEE Transactions on Power Electronics*, Vol. 26, pp. 1790-1799, 2011.

[9] S.K. Sahoo, A. Ramulu, S. Batta and S. Duggal, "Performance Analysis and Simulation of Three Phase Voltage Source Inverter using Basic PWM Techniques", *Proceedings of International Conference on Sustainable Energy and Intelligent Systems*, pp. 1-7, 2012.

[10] C. Bassi, M. Filippo, D. Giulivo and A. Tessarolo, "Experimental Assessment of Medium-Voltage Induction Motor Performance under Multilevel PWM Inverter

Supply", *Proceedings of International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion*, pp. 253-258, 2012.

[11] Y. Lee and J. Kim, "A Novel Enhanced Inverted PWM Driving Scheme for Three-Phase BLDC Motor Drive", *Proceedings of IEEE International Conference on Consumer Electronics*, pp. 206-212, 2018.

[12] P. Colantonio, E. Cipriani, F. Giannini, L. Cabria, I.S. Gosh, U. Altmann, R. Follmann and N. Ayllon, "Development of a PWM based Transmitter for P-Band SAR Applications", *Proceedings of International Conference on Microwave, Radar and Wireless Communications*, pp. 1-4, 2016.

[13] K. Cheng, "Implementation of High Resolution Digital Pulse Width Modulator Based on FPGA", *Proceedings of IEEE International Conference on Signal, Information and Data Processing*, pp. 1-5, 2019.

[14] S. KılıncK. N. Salama and U.C Sam, "Realization of Fully Controllable Negative Inductance with Single Operational Transresistance Amplifier", *Circuits Systems Signal Processing*, Vol. 2, No. 1, pp. 47-57, 2006.

[15] C. Cakir, U. Cam and O. Cicekoglu, "Novel All Pass Filter Configuration Employing Single OTRA", *IEEE Transactions on Circuits and Systems-II*, Vol. 52, No. 3, pp. 122-125, 2005.

[16] A.K. Kafrawy and A.M. Soliman, "New CMOS Operational Transresistance Amplifier", *Proceedings of IEEE International Conference on Microelectronic*, pp. 31-34, 2006.

[17] K.N. Salamaa and A.M. Soliman, "CMOS Operational Transresistance Amplifier for Analog Signal Processing", *Microelectronics Journal*, Vol. 30, pp. 235–245, 1999.

[18] S. Banerjee, M. Ghosh and P. Mondal, "OTRA based Realization of Second Order Inverse Lowpass Filter and Inverse Bandpass Filter", *Proceedings of International Conference on Communication and Signal Processing*, pp. 148-152, 2019.

[19] H. Mostafa and A.M. Soliman, "A Modified CMOS Realization of the Operational Transresistance Amplifier (OTRA)", *Frequenz*, Vol. 60, No. 3-4, pp. 70-76, 2006.

[20] Olawale J. Omotosho and Samson O. Ogunlere, "Design Analysis and Circuit Enhancements of SR-Flip Flops", *Journal of Engineering Sciences and Research Technology*, Vol. 2, pp. 2433-2446, 2013.

[21] M. Siripruchyanun, P. Wardkein and W. Sangpisit, "Simple Pulse Width Modulator using Current Conveyor", *Proceedings of International Conference on Recent Technology*, pp. 452-457, 2000.

[22] PWM Basics, Pulse Width Modulator Amplifier, Available at https://www.electronics-tutorials.ws/blog/pulse-width-modulation.html, Accessed at 2021.

[23] H. Kim, H.J. Kim and W.S. Chung, "Pulse Width Modulation Circuits using CMOS OTAs", *IEEE Transactions on Circuits and Systems I*, Vol. 54, No. 9, pp. 1869-1878, 2007.

[24] M. Siripruchyanun and P. Wardkein, "A Fully Independently Adjustable, Integrable Simple Current Controlled Oscillator and Derivative PWM Signal Generator", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, Vol. 86, No. 12, pp. 3119-3126, 2003.

[25] R.K. Ranjan and K. Mazumdar, "Generation of Square and Triangular Wave with Independently Controllable Frequency and Amplitude using OTAs only and its Application in PWM", Analog Integrated Circuits and Signal Processing, Vol. 92, pp. 15-27, 2017.

[26] D.S. Rajput and R. Singh, "Timer Circuit using OTRA and its Application as Stable and Monostable Multivibrator", *Proceedings of International Conference on Electronics and Communication Systems*, pp. 1047-1050, 2015.