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CONTROLLING AMBIPOLAR CURRENT AND ENHANCEMENT OF ON-STATE CURRENT WITH HIGH AND LOW CONCENTRATION SOURCE POCKETS

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Abstract

This paper proposes and investigates a new architecture of PNPN TFET by using 2-D ATLAS Device Simulation Software TCAD Tool. The source pocket plays a crucial role in increasing the ON-state current through Tunnel FET. In order to enhance the source pocket characteristics, the source pocket is divided laterally into high and low concentration source pockets without modulating its width (LP). This modification results in a reduction of tunnelling width (λ), thereby increasing the significant amount of lateral electric field and suppressing the horizontal electric field, which in turn enhances the tunnelling probability as well as tunnelling rate. This proposed structure is a promising candidate for getting higher ON-state current (Ion), higher current ratio (Ion/Ioff), lower threshold voltage (VT) and reduced steepness sub-threshold slope (SS). These parameters are calculated with respect to conventional PNPN TFET and hetero-dielectric BOX (HDB) PNPN TFET, which enable the device to be operated efficiently with lower power consumption.

Keywords:

Band-to-Band Tunnelling (BTBT), Sub-Threshold Swing, Tunnelling Field-Effect Transistor (TFET), High-κ Dielectric, Hetero-Dielectric BOX (HDB)

1. INTRODUCTION

The Tunnel FET device is the best replacement for the conventional MOSFET devices because it has the ability to achieve lower values of sub-threshold swing (SS) than the thermal limit (60 mV/decade) of MOSFETs [1]. It can also achieve lower power consumption and higher scaling possibility than MOSFETs. The ambipolar behaviour of Tunnel FET may cause an increase in ambipolar conduction current [2]. However, its ON-state current (I_{on}) is too low to operate properly. In order to achieve the perfect transistor characteristics, it is needed to improve the existing conventional architecture or replace it with a new architecture, which has improved features and less fabrication complexity. Nowadays, the main reasons which degrade or limit the transistor performance, are ambipolar behaviour [3], an increase in standby power of the device [4], a higher sub-threshold swing which limits the transistor speed performance [5], lower ON-state current (I_{on}) which affects the operation and feasibility of the transistor [6]. Several approaches or techniques have been proposed to suppress the ambipolar behaviour of TFET. A number of device architectures have been proposed. Some of them are low drain doping, low-k spacers, gate-drain underlaps and lateral heterostructure with high bandgap material at the drain side [2]-[15]. The Tunnel FET suffers from low ON-state tunnelling current (I_{on}) because of the poor efficiency of band-to-band tunnelling (BTBT) [16].

Numerous factors like the higher effective mass of carriers, larger tunnelling width (λ), the indirect nature of bandgap, the high value of bandgap, and insufficient lateral electric field (E_x) (which is mainly responsible for tunnelling) are the reasons for this poor efficiency [8], [18], [19], [23]. Although the use of hetero-dielectric BOX below the source region reduces the ambipolar conduction it also reduces the ON-state current and increases the fabrication complexity. Hence, a new architecture is needed to improve the ON-state current.

Many solutions are available in the literature like using a PNPN TFET instead of the conventional p-i-n TFET structure [2], low drain doping [20], using lower bandgap material [6], [14], [25] and so on. These solutions are not adequate to achieve the higher ON-state current due to the presence of numerous drawbacks.

This paper proposes a new tunnel FET architecture which has split source pockets instead of a single source pocket. High and low concentration source pocket PNPN TFET structure is shown in Fig.1. This structure is capable of increasing the ON-state current significantly when compared to conventional PNPN TFET. It also incorporates a hetero-dielectric BOX (HDB) on the high concentration ground plane (P+) of n-channel PNPN TFET as shown in Fig.2. This high concentration ground plane is able to reduce the ambipolar conduction by increasing the depletion on the channel and the drain interface region [21]. Considering an optimal value of spacer length (L_S), i.e., 30 nm on both sides of the gate. The effective depletion in the interface region varies with the spacer length [21].

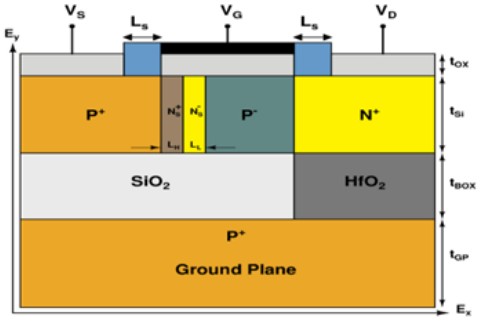


Fig.1. Schematic view of proposed architecture

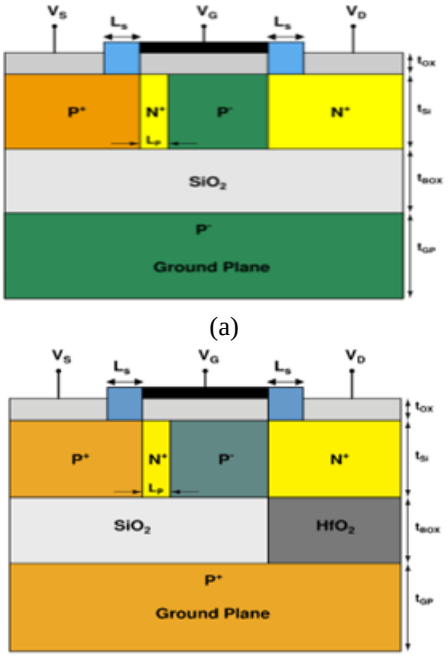
2. PROPOSED PNPN TFET ARCHITECTURE AND PARAMETERS

The schematic view of the conventional PNPN TFET and HDB PNPN TFET is shown in Fig.2 [21] and the proposed high and low concentration source pocket PNPN TFET is shown in

Fig.1. The details of device structure and parameters are given in Table.1. These parameters have been chosen in such a way that an optimal device performance is obtained [21]. The high and low concentration source pockets are the only difference in the proposed architecture when compared to conventional PNPN TFET and hetero-dielectric BOX (HDB) PNPN TFET.

2.1 QUANTUM TUNNELLING

Traditionally, free electrons are incapable of crossing the barrier due to insufficient energy. However, when these electrons tunnel through the barrier, it results in a tunnelling current. According to quantum mechanics, electrons exhibit wavelike nature. These waves do not end instantaneously at a surface or barrier, but die-out rapidly. For a thick barrier, a wave does not get past. If the barrier is thin enough, there is a higher probability of electrons penetrating the barrier to move into the next region. The probability that the electrons are present on the far side of the barrier is lower due to concentration gradient. As a result, only few electrons will penetrate the barrier. The movement of electrons through the barrier in this manner is called tunnelling.



(a)

(b)

Fig.2. The schematic view of (a) conventional PNPN TFET and (b) hetero-dielectric BOX (HDB) PNPN TFET [21]

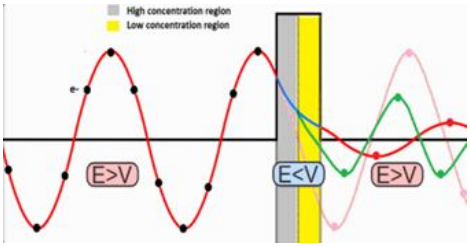


Fig.3. Quantum tunnelling through a barrier

The Fig.3 shows the scenario of the barrier being quite thin (about few nanometre). It is noticeable that a particle approaching from the left has insufficient energy to cross the barrier. However, once in a while, it can "tunnel" through the barrier to reach the far side.

Due to rapid fall in probability function through the barrier, the barrier thickness plays an important role in determining the number of electrons that will actually tunnel through the barrier. An increase in barrier thickness results in the current diminishing exponentially.

2.1.1 Drain Source Tunnelling Current (Idt):

The central expression in TFET model is an experimentally well-established equation for describing the fundamental transport mechanism in tunnel transistors [5], [6], i.e., band-to-band and Zener tunnelling in planar *p-n* junctions [3], [4]. The tunnelling phenomenon in a 2-terminal Zener diode can be transformed to a 3-terminal diode by employing the concepts of semiconductor physics.

In output characteristics, tunnelling window V_{tw} and the dimensionless factor f are responsible for the super linear onset current as per the following equation:

$$I_{dt}\left(V_{gs}V_{ds}\right) = a * f * E * V_{tw} * e^{-\frac{b}{E}} \tag{1}$$

where coefficients a and b are defined as:

$$a = \frac{Wt_{ch}q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_r^*}{E_g}} \tag{2}$$

$$b = \frac{4\sqrt{2m_r^* E_g^2}}{3q\hbar^2} \tag{3}$$

where $m_r^* = \left(\frac{1}{m_e^*} + \frac{1}{m_h^*}\right)^{-1}$ is the reduced effective mass, m_e^* and m_h^* are effective masses of electron and hole respectively, $\hbar$ is the reduced Planck's constant, E_g is the semiconductor band gap, W is channel width, t_{ch} is channel thickness and q is electron charge.

$$m_r^* = m_R m_0 \tag{4}$$

$$E_g = E_G q \tag{5}$$

The factor f is given by:

$$f = \frac{1 - e^{-V_{dse}/\Gamma}}{1 + e^{(V_{thds} - V_{dse})/\Gamma}} \tag{6}$$

where,

$$V_{dse} = V_{ds\min}\left(V_0 + V_1 - \sqrt{\delta^2 + 1}\right) \tag{7}$$

$$V_0 = \frac{V_{ds}}{2V_{ds\min}} \tag{8}$$

$$V_1 = \sqrt{\delta^2 + \left(V_0 - 1\right)^2} \tag{9}$$

$$V_{ds\min} = 10^{15} \tag{10}$$

$$V_{th} = \lambda \tanh(V_{gs}) \tag{11}$$

where δ is the transition width parameter. As V_{ds} becomes negative, the parameter V_{dse} tends to zero. The electric field in the tunnelling junction is given by:

$$E = \xi_0(1 + \gamma_1 V_{ds} + \gamma_2 V_{goe}) \tag{12}$$

where ξ_0 is the built-in electric field, γ_1 and γ_2 are electric field parameters.

V_{goe} also approaches zero as V_{go} becomes negative.

$$V_{goe} = V_{\min}\left(V_0 + \sqrt{\delta^2 + (V_0 - 1)^2}\right) \quad (13)$$

$$V_0 = \frac{V_{go}}{2V_{\min}} \quad (14)$$

$$V_{\min} = 0.0001 \quad (15)$$

The expression for the tunnelling window is given by:

$$V_{tw} = ln\left(1 + e^{\frac{V_{gt}}{U}}\right) \quad (16)$$

U is the Urbach factor, which is a linear function of the gate source voltage.

$$V_{gt} = V_{gs} - V_{th} \quad (17)$$

$$U = \gamma_0 U_0 + (1-\gamma_0) U_0 V_{goen} \quad (18)$$

$$U_0 = V_t\, n_1 \quad (19)$$

where γ_0 is the tunnel window parameter and n_1 is the sub-threshold identity factor.

$$V_t = (k_B(T + 273.15))/q \quad (20)$$

$$V_{goen} = V_{goe}/V_{th} \quad (21)$$

3. SIMULATION RESULTS AND ANALYSIS

All the simulations have been done by using Silvaco Atlas TCAD tool [22]. The proposed structure uses nonlocal band-to-band tunnelling (BTBT) model to study the forward tunnelling current in lateral direction of the electric field. Lombardi model has been included to account for high field mobility effects. Fermi-Dirac statistics model has been used for reduced carrier concentration in heavily doped region by using statistical approach and Shockley Read Hall (SRH) recombination model has also been considered for fixed minority carrier lifetime. Bandgap Narrowing (BGN) has been enabled to account for highly doped region. While the defects and the trap have been ignored at the interface, a defect-free interface has been considered in these simulations [9].

Table.1. Details of Device and Simulation Parameters.

Parameter	Conv. PNPN TFET	HDB PNPN TFET	Proposed PNPN TFET
Gate oxide thickness (t_{OX})	1 nm	1 nm	1 nm
Silicon layer thickness (t_{Si})	10 nm	10 nm	10 nm
BOX thickness (t_{BOX})	25 nm	25 nm	25 nm
Source doping (N_A)	$1e^{20}$ cm^{-3}	$1e^{20}$ cm^{-3}	$1e^{20}$ cm^{-3}
Drain doping (N_D)	$5e^{18}$ cm^{-3}	$5e^{18}$ cm^{-3}	$5e^{18}$ cm^{-3}
Channel doping (N_A)	$1e^{17}$ cm^{-3}	$1e^{17}$ cm^{-3}	$1e^{17}$ cm^{-3}
Source pocket doping (N_D)	$1e^{20}$ cm^{-3}	$1e^{20}$ cm^{-3}	$1e^{20}$-$1e^{19}$$cm^{-3}$
Ground plane doping (N_A)	$1e^{17}$ cm^{-3}	$1e^{20}$ cm^{-3}	$1e^{20}$ cm^{-3}
Source pocket length (L_P)	4 nm	4 nm	2nm-2nm split
Gate length (L_G)	50 nm	50 nm	50 nm
Spacer Length (L_S)	30 nm	30 nm	30 nm
Gate work function (Φ)	4.33 eV	4.33 eV	4.33 eV

The band diagrams shown in Fig.4 and Fig.5 reflect the similarity between the operation of the proposed PNPN TFET and the conventional PNPN TFET [13]. The modulation effect of tunnelling width (λ) due to a horizontal cut at 1 nm below the Si-SiO_2 interface has been analysed in the conventional PNPN TFET, HDB PNPN TFET and proposed PNPN TFET. The electrical characteristics of the proposed tunnel FET can be enhanced by introducing a source pocket between the source and the channel interface region. The reasons for this enhancement are as follows:

- The formation of a local minimum energy point below the conduction band and the valence band, which results in a sharper change in the conduction band and valence band, thus, reducing the tunnelling barrier width (λ).
- Strengthening of lateral electric field (E_x), which helps in getting a high ON-state current [6], [13], [14], [16]-[19].
- A reduction in the vertical electric field (E_y). This results in an increased reliability due to reduction in the rate of generation of the interface traps [9].

The tunnelling probability equation is given by:

$$T(E) \propto \exp\left(\frac{-4\sqrt{2m^* E_g^{0.5}}}{3|e|\hbar\left(E_g + \Delta\phi\right)}\varepsilon_t\right)\Delta\phi \quad (22)$$

$$\varepsilon_t = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}}} t_{ox} t_s \quad (23)$$

where m^* is the effective mass of the electron, E_g is the energy band gap, $\Delta\phi$ is the energy range over which the tunnelling occurs, t_{0x} is the oxide film thickness, t_{sis} the silicon film thickness, ε_{ox}, ε_s are the dielectric constants and $\hbar$ is the reduced Planck's constant.

Increasing the ON-state current in TFET without influencing other parameters is a challenging task. The ON-state current varies with the source pocket width. In fact, increasing the source pocket width results in an increase in the ON-state current (I_{on}). Simultaneously it also leads to an increase in the OFF-state current (I_{off}), thereby reducing the electrical characteristics performance [12]. There is a trade-off among the ON-state current (I_{on}), OFF-state current (I_{off}) and steepness of the sub-threshold slope [24], [26], [27].

This paper demonstrates an effective solution of increasing the ON-state current (I_{on}) without affecting the width of the source pocket and other parameters. In the proposed PNPN TFET structure, the entire source pocket width (L_P) is divided into two equal parts, high and low concentration source pockets from source to channel side with equal length (L_H=L_L=2 nm). The high concentration source pocket doping is N^+=1e20 cm^{-3} and low concentration source pocket doping is N^-=1e19 cm^{-3}. Both high and low concentration source pocket lengths are shown in Fig 1. The partition of source pocket (i.e., L_H and L_L) creates a grading change of doping concentration in the interface region, due to which a local minimum energy level is generated below the conduction band and valence band having subsided energy level. The generation of this local minimum energy level increases the band bending capability and reduces the tunnelling width (λ) as shown in Fig.4 and Fig.5. Consequently, lower amount of energy

is required by the electrons to tunnel through the junction. According to the tunnelling probability equation, this lower amount of energy requirement is also responsible for decreasing the tunnelling width (λ) and increasing the tunnelling rate.

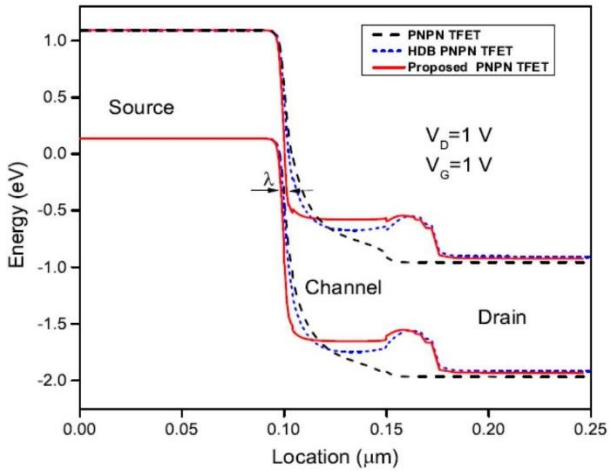


Fig.4. On-state energy band diagram comparison of conventional PNPN TFET, HDB PNPN TFET and proposed PNPN TFET

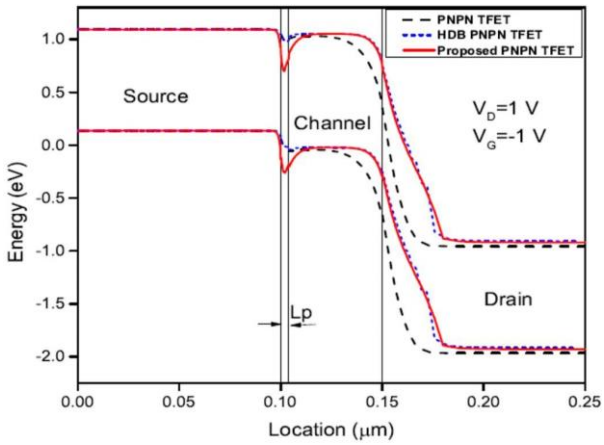


Fig.5. Off-state energy band diagram comparison of conventional PNPN TFET, HDB PNPN TFET and proposed PNPN TFET

A comparison of the conventional PNPN TFET, HDB PNPN TFET and proposed PNPN TFET band diagrams is shown in Fig.4 and Fig.5. Owing to a smaller tunnelling barrier thickness or effective electrostatic control over the channel surface, the current flowing in the vicinity of Si-SiO_2 interface is larger than the current through the inner part of the channel region. The source pocket length (L_P) and the source pocket doping concentration (N_D) play a crucial role in improving the electrical characteristics of the proposed PNPN TFET. The length at which the higher concentration source pocket (L_H) and the lower concentration source pocket (L_L) are completely depleted is considered as the maximum length for the source pocket. In the proposed architecture, the maximum length is 4 nm with higher source pocket doping concentration N^+=1e20 cm^{-3} and lower source pocket doping concentration N^-=1e19 cm^3. The gate-controlled band-to-band tunnelling (BTBT) at the source describes the sub-threshold conduction mechanism at this length.

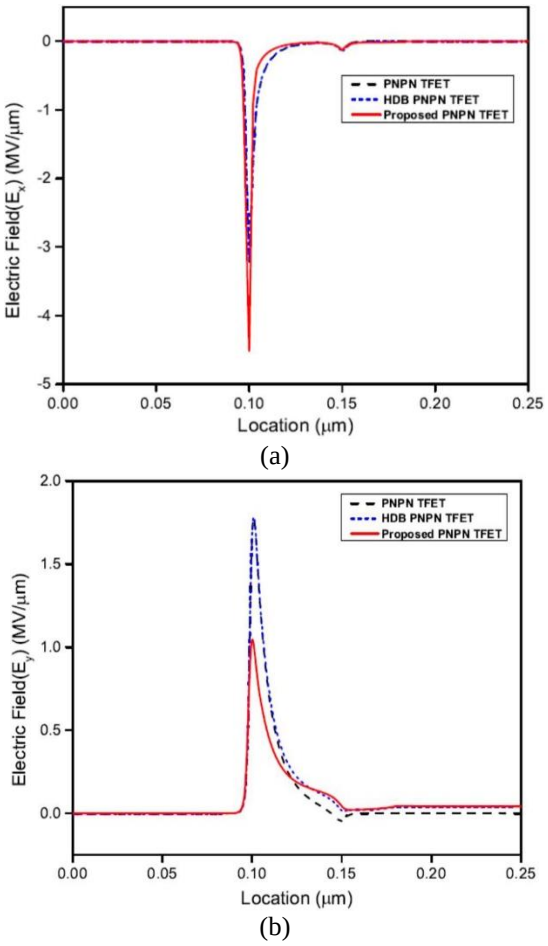


Fig.6. (a) Lateral electric field of conventional PNPN TFET, HDB PNPN TFET and proposed PNPN TFET, (b) Vertical electric field of conventional PNPN TFET, HDB PNPN TFET and proposed PNPN TFET

Rise in optimum length beyond 4 nm results in partial depletion of source pocket, thereby decreasing the concentration of electrons between the source and the channel interface region. A direct impact of this reduction can be observed in the form of declined conduction band profile. If the source pocket length is increased beyond the optimum length of 4 nm, the gate influence on the depletion region tends to decrease. This results in incomplete depletion and hence, the sub-threshold swing and the ambipolar current of the PNPN TFET begin to decline.

The reduction in the vertical electric field (approx. 27.85% with respect to conventional PNPN TFET) helps in decreasing the ambipolar conduction rate between the channel and the drain interface when V_D=1V and V_G=1 V is applied. It also reduces the interface trap charges in the device. On the other hand, enhancement in the lateral electric field (approx. 42.75% with respect to conventional PNPN TFET) improves the tunnelling probability and tunnelling rate.

The transfer characteristics of the conventional PNPN TFET, HDB PNPN and proposed PNPN TFET are shown in Fig.7 and 8. Due to accumulation of local charges near L_H and L_L split source pockets, the electric field is confined to a particular region and a particular direction, i.e., source pocket region and lateral electric field direction respectively. It has been observed that the electric field in TFET is very important for proper operation of the device.

The lateral component (E_x) is mainly responsible for higher tunnelling probability ($T(E)$) and higher tunnelling current. An improvement in the lateral electric field (E_x) peak in the proposed PNPN TFET is helpful in obtaining higher ON-state current and improving the transfer characteristics. On the other hand, the vertical component of the electric field (E_y) at the interface in the TFET device may cause reliability problems such as bias temperature instability stress, interface trap generation, and leakage current [3], [8], [9].

This paper aims at reducing the vertical electric field and increasing the lateral electric field as shown in Fig.6(a) and Fig.6(b). Tunnelling also depends on the velocity of the electrons. The lateral electric field induced near the source and the channel interface region is responsible for giving rise to high velocity electrons.

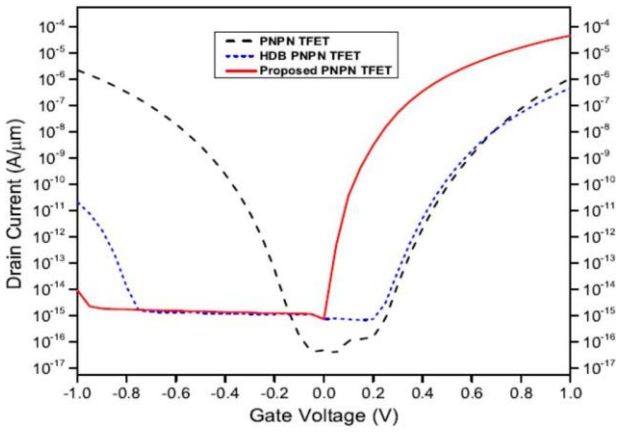


Fig.7. Transfer characteristics of conventional PNPN TFET, HDB PNPN TFET and proposed PNPN TFET

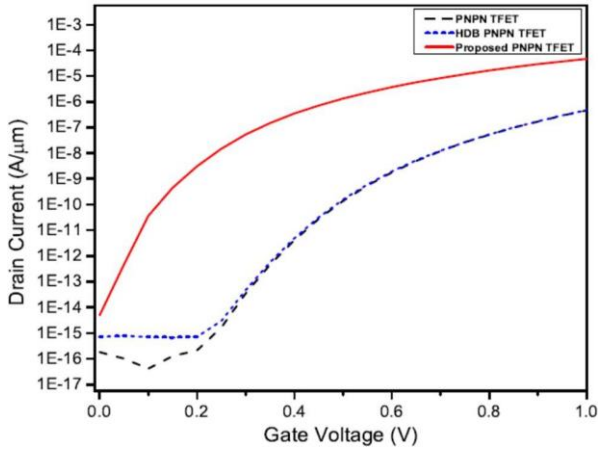


Fig.8. Forward transfer characteristics of conventional PNPN TFET, HDB PNPN TFET and proposed PNPN TFET

3.1 EFFECT OF VARIATION IN SOURCE POCKET LENGTH (L_P) ON VARIOUS PARAMETERS

The Fig.9 shows the variation of sub-threshold swing (SS) with source pocket length (L_P). It can be observed from the figure that initially the sub-threshold swing remains almost constant as the source pocket length is varied from 1 nm to 3 nm. Thereafter, it starts decreasing with the source pocket length and decreases to reach an optimal value of approx. 25 mV/decade for the source pocket length of 4nm. This is the optimal value sub-threshold swing for proposed TFET. As the source pocket length is increased beyond 4nm, the sub-threshold swing begins to increase again.

The Fig.10 shows the variation of threshold voltage (V_T) with source pocket length. It can be observed that the value of threshold voltage (V_T) is minimum (~0.23 V) at a source pocket length (L_P) of 4 nm. This shift in threshold voltage to a lower value is due to the creation of local minimum energy level below the conduction band and valence band which requires very low gate voltage to switch ON the TFET device.

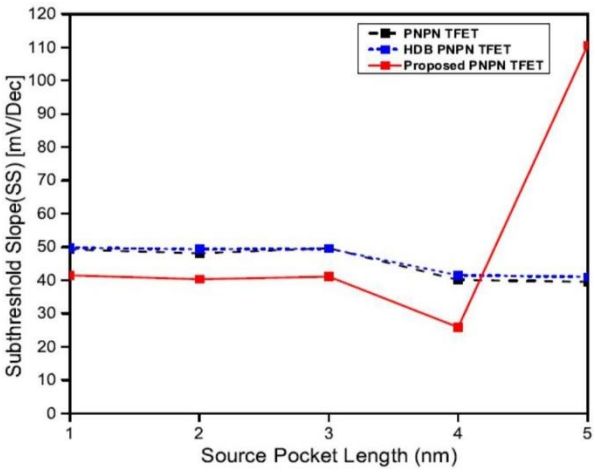


Fig.9. Effect of variation in source pocket length on Sub-threshold Swing (SS) of proposed high and low concentration source pocket PNPN TFET, HDB PNPN TFET and conventional PNPN TFET

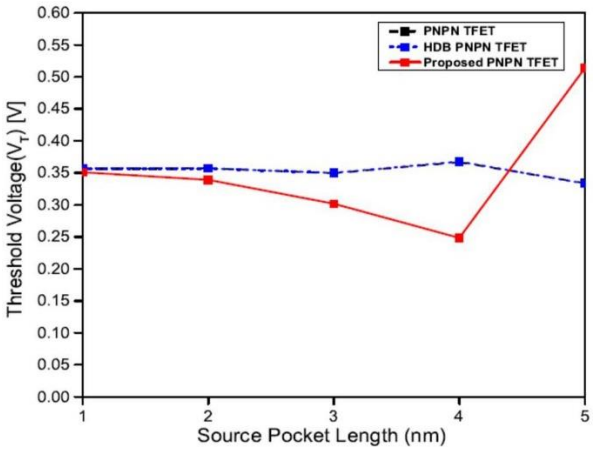


Fig.10. Effect of variation in source pocket length on threshold voltage of proposed high and low concentration source pocket PNPN TFET, HDB PNPN TFET and conventional PNPN TFET

The On-state and OFF-state current ratio I_{on}/I_{off} is an important parameter for the TFET to work as high-speed switching device with low power consumption. Typically, it should be greater than 10^6 [27]. Fig.11 shows the variation of the I_{on}/I_{off} current ratio with the source pocket length. It can be noticed that the optimum value of the I_{on}/I_{off} current ratio (~10^{10}) is obtained for the source pocket length of 4 nm. Increasing the source pocket length beyond the 4 nm results in degradation of the I_{on}/I_{off} current ratio.

4. COMPARISON OF DEVICE SIMULATION RESULTS

The Table.2 shows all the improved parameters of conventional, HDB and proposed PNPN TFET device. We have achieved the negligible amount ambipolar current when gate voltage decreases up to -1 volt.

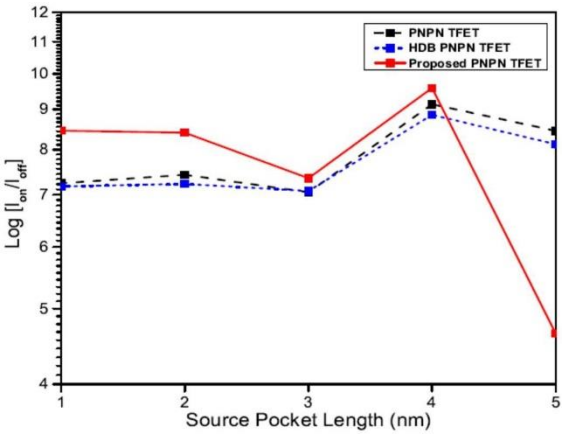


Fig.11. Effect of variation in source pocket length on I_{on}/I_{off} current ratio of proposed high and low concentration source pocket PNPN TFET, HDB PNPN TFET and conventional PNPN TFET

Table.2. Results Comparison Analysis of Conventional PNPN TFET, HDB PNPN TFET and Proposed PNPN TFET

Parameters	Conv. PNPN TFET	HDB PNPN TFET	Proposed PNPN TFET
Lateral Electric Field (E_x) (MV/µm)	~-3.26	~-3.58	~ -4.84
Vertical Electric Field (E_y) (MV/µm)	~1.85	~1.62	~1.05
Off-State Current (I_{OFF}) upto -1V_{GS} (A)	~1.26×10^{-5}	~6.28×10^{-10}	~1.92×10^{-14}
On-State Current (I_{ON}) (A)	~8.68×10^{-6}	~8.31 x10^{-6}	~ 4.78×10^{-4}
SS (mV/dec)	~ 40	~ 38	~ 24
V_T (Volt)	~ 0.38	~ 0.36	~ 0.23
I_{ON}/I_{OFF}	~ 8.58	~ 8.76	~ 9.38

It improved the study state power consumption and leakage current of the device, on-state current increased around 50 times of conventional PNPN TFET, steepness of device increased drastically up to 24mV/dec. This device also capable of low voltage application due to threshold voltage reaches as low as 0.23 volt. Here I_{ON}/I_{OFF} parameters increased around 9 to 10 times with respect of conventional and HDB PNPN TFET.

5. CONCLUSION

This paper proposes an improvised architecture for the conventional PNPN TFET and hetero-dielectric BOX PNPN TFET by bifurcating the source pocket into high and low concentration source pockets. This architecture shows promising simulation results in terms of significant high ON-state (I_{on}) current, minimum steepness sub-threshold slope threshold voltage (V_T) (~0.23V). All the simulation results have been demonstrated by using 2-D Silvaco ATLAS simulations TCAD tool.

The proposed architecture effectively reduces the tunnelling width (λ) to approximately 2.6 nm between source-channel interface region resulting in sufficient band bending. This leads to proper tunnelling even for a low gate biasing voltage and an increase in the lateral electric field (E_x) (~42.75%), which, in turn, increases the tunnelling rate as well as tunnelling probability. Due to this, the proposed device architecture can be used to increase the tunnelling conduction without increasing the OFF-state current (I_{off}) (in the range of femto Ampere/micron). It also diminishes the ambipolar conduction at the channel drain interface due to efficient depletion in the drain region by using high-k dielectric BOX below the drain region. Therefore, ambipolar conduction current is sustained at the minimum value even for V_G=-1V. The proposed PNPN TFET may serve as a better alternative of the conventional MOSFET devices for digital circuit applications with low power consumption.

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