ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2022.0210

LOW POWER DYNAMIC CMOS INVERTER AND SRAM CELL DESIGN USING LECTOR AND LECTOR-B TECHNIQUE

Vivek Harshey[1], Pankaj Kumar Das[2] and Shivani Sharma[3]

[1,2]Department of Electronics and Communication Engineering, Sant Longowal Institute of Engineering andTechnology, India
[3]Department of Electronics and Communication Engineering, Dr. B.R. Ambedkar National Institute of Technology, India

Abstract

At the current deep submicron and nanometer level, the leakage power is becoming the major contributor to overall power consumption in modern VLSI circuits. This research paper presents a novel approach to reducing leakage power by inserting two leakage transistors in the middle of pull-down and pull-up paths. Out of these two leakage transistors, one is the PMOS transistor, and another one is the NMOS transistor. This research work presents a dynamic CMOS inverter and 6T SRAM cell with and without transmission gate (TG) to reduce leakage power using the LECTOR and LECTOR-B techniques. The Cadence Virtuoso simulation tool is used to presents the results in terms of static power. Using the 45-nm technology node, the performance in terms of static power is analyzed. It is observed that using LECTOR and LECTOR-B techniques, the overall reduction in static power is 26% and 20%, respectively, compared to the conventional design for SRAM cell. Similar improvements are also noted for dynamic CMOS inverter and TG SRAM cell.

Keywords:

Dynamic CMOS Inverter, SRAM Cell, Leakage Power, LECTOR, LECTOR-B Technique

1. INTRODUCTION

In the recent past, power consumption is arguably the most critical challenge in modern-day VLSI design, pushing the performance to the secondary level. Most of the VLSI circuits demonstrated that, at technologies beyond 65nm, the dynamic power dissipation is higher than that of static power dissipation. At 65nm technology, both the dynamic and static power are the same [1]. If the technology is scaled down further, then the static power predominates over the dynamic power. Subthreshold leakage current is the dominating leakage current, and it increases exponentially as the threshold voltage V_t scales down. The threshold voltage is the primary parameter on which leakage power minimization is possible. The scaling down of threshold voltage hurts subthreshold leakage current.

As the threshold voltage scales down, there is a reduction in delay. So, from the performance point of view, a smaller threshold voltage is required, leading to faster operation and higher performance. With the reduction in threshold voltage the subthreshold current increases linearly. There is a tradeoff between higher performance and the subthreshold leakage current. We have the higher performance of CMOS circuits at low threshold voltage, but there is a dominating subthreshold leakage current. On the other side, the subthreshold leakage current reduces at a high threshold voltage, but there is a penalty of delay. In the CMOS circuits, threshold voltage must be kept in the range of $0.2V_{DD}$ to $0.5V_{DD}$ to get excellent performance and reasonable delay at the same time. As the supply voltage scales down, there is a reduction in dynamic power, but at the same time, their performance degrades. Therefore, to increase the device's operating speed, the downscaling of supply voltage along with threshold voltage should be carried out. However, scaling of these two parameters results in increased static power dissipation because of an exponential increase in the sub-threshold leakage current [2]–[4].

In this paper, we propose reducing the SRAM cell's static power using the LECTOR and LECTOR-B techniques. LECTOR technique uses the principle of transistor stacking. Additionally, the leakage power is also reduced using the LECTOR technique. In this approach, the pull-down and pull-up paths also consist of two transistors which act as a leakage control mechanism. The key concept behind this method was to slash leakage power by placing transistors in a stack in the path between supply to the ground. Hence, the gate of one leakage transistor is controlled by the source of other leakage transistors. To understand its effect, we note that supply voltage to the ground path is predominantly leakier when there is one OFF transistor as compared to many OFF transistors. Thus, effectively transistor stacking reduces leakage power [5]. In [5], the authors used a technique where two leakage control transistors (LCTs) are introduced in each CMOS gate so a cutoff region of operation was achieved for one of the LCTs. Nevertheless, the problem with the LECTOR technique was that it increases the delay, so to reduce the delay sizing of the transistor has been done, and also the substrates of leakage transistors are connected to their respective sources, this method is named as LECTOR-B technique [6]. Previously the static CMOS inverter has been analyzed using LECTOR technique [7].

Leakage power is a severe issue in dynamic CMOS when the clock is 1 and input is 0 at that time. The load capacitor starts discharging, but the requirement is it must charge up to maximum V_{DD}. So, this problem has been solved by introducing two leakage control transistors between pull-up and pull-down networks. The improvement of semiconductor process expertise has been the lashing strength behind the VLSI system design's speedy progress. In modern design, large on-chip memory or embedded memory must meet the growing demand for reduced power consumption and higher performance. Due to its higher speed and compatibility with process variations, the old six-transistor (6T) SRAM cell design plays an important part in many embedded memories and on-chip memories [7]. In CMOS VLSI circuits, power dissipation is deemed an important factor for the low power VLSI design by integrated circuit designers in the modern IC design process.

Nevertheless, the SRAM cell design faces straightforward challenges in maintaining enough cell stability due to scaling in technology. These difficulties stem from the increasing variability of process parameters as technology scales down and that embedded memory is particularly vulnerable to process variations. To address these issues, numerous advanced SRAM topologies and techniques have been discovered in recent years.

In this paper, a new SRAM cell design is analyzed using the stacking approach, which consumes less leakage power comparatively. The 6T SRAM cell has been analyzed by using the LECTOR and LECTOR-B technique. Then transmission gate SRAM cell analysis is presented for dynamic power, static power, and delay and finally for low delay purpose. Low power consumption circuit has been designed and named as single-ended transmission gate SRAM cell and analyzed using LECTOR and LECTOR-B technique [8] [9].

This paper is organized as follows: Section 1 introduces the different leakage power in VLSI circuits in the current research scenario. Section 2 provides the details about the dynamic CMOS inverter. Section 3 briefs about the SRAM cell. Section 4 describes the transistor stacking techniques. Section 5 presents the basics of the proposed lector technique. Finally, using the LECTOR and LECTOR-B techniques, low leakage power dynamic CMOS inverter and SRAM CELL designs are presented in section 5. Section 6 presents the result in terms of static power reduction of CMOS inverter and SRAM cell.

1.1 DYNAMIC CMOS INVERTER

The dynamic CMOS logic is presented as an alternative to static CMOS logic. There is no mechanism of pulling the output to a low or high level in dynamic logic, with the mode of operation determined by the clock signal CLK, i.e., either precharge or evaluation. This circuit only consumes dynamic power, and between V_{DD} and *GND* no static current path exists. The logic gates have faster switching speeds.

A clock signal is required in dynamic CMOS logic to estimate the combinational logic. There is no mechanism of pulling the output to a high or low level [10][11]. The circuits using dynamic MOS are realized using the parasitic capacitors to store information. In this case, when the clock is high the circuit dissipates power, and achieve low output. The high clock causes current to flow, by which power consumption reduces, ultimately depending on the ON time of the clock i.e., duty cycle.

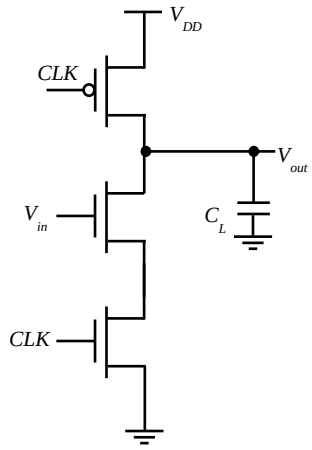

Fig.1. Conventional Dynamic CMOS inverter

To ensure faithful operation in dynamic logic a minimum clock rate is required so that output state of each dynamic gate is used or refreshed until the charge in the output capacitance leaks out enough to allow the digital state of the output to shift. Dynamic logic, in general, dramatically increases the number of transistors switching at any given time, resulting in higher dynamic power usage than static CMOS.

1.2 SRAM CELL

The primary memory block used in modern-day high-performance processors is the SRAM cell due to the design's compatibility. SRMA occupies a large amount of area in System on a Chip design. The low power designing of SRAM is itself a massive task. Additionally, process variations coupled with shrinking dimensions are significant challenges to designing an SRAM cell with low power dissipation. In the case of low power ICs, with the reduction in supply voltage, SRAM's main requirement is to be compatible with the functional conditions. Still, while considering the low voltage operation of SRAM as the critical point in designing the SRAM cell, designers must overcome several obstacles like bit cell stability, process variations, faithful sensing, and reliable operation of the whole memory chip. [12][13]

SRAM provides the advantage of low power consumption; SRAM designers must pay attention to the tradeoff between performance and area and maintain low power design.

The W/L ratio used in an SRAM cell's schematic plays a crucial role in deciding various output characteristics and features of the SRAM cell. The W/L ratio decides the output current, the transistor's gain, its trans-conductance, and other parameters. So, it becomes crucial to determine the optimum W/L ratio.

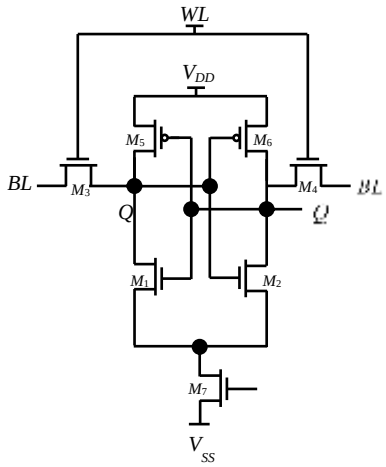

Fig.2. Conventional SRAM Cell

In a CMOS SRAM cell, to determine the W/L ratios of transistors, many design criteria are needed to be considered. Nevertheless, the two basic requirements which should be fulfilled to decide W/L ratios are:

1. The stored information in the SRAM cell should not get destroyed by the data-read operation.
2. Stored information modification should be allowed by the SRAM cell during the data-write phase [14] [15].

$$\frac{k_{n,3}}{k_{n,1}} = \frac{\left(W/L\right)_3}{\left(W/L\right)_1} < \frac{2\left(V_{DD} - 1.5V_{T,n}\right)V_{T,n}}{\left(V_{DD} - 2V_{T,n}\right)^2} \quad (1)$$

2. TRANSISTOR STACKING

The transistor stacking technique is used to reduce leakage power that works well in standby and an active mode of operation. The underlying principle is that series-connected transistors in off-state produce substantially less leakage than a single unit with comparable channel length. The off-current is reduced by a factor of two by channel length doubling. However, due to reverse short channel effects, the threshold voltage in modern-day devices of deep sub-micron regime can decrease for more extended channels hence making it less effective for, leakage reduction. The linear modeling of threshold voltage is given by [14].

$$V_{tn} = V_{tn}^{0} - mV_{DS} - gV_{BS} \quad (2)$$

where DIBL coefficient is modeled by m and the term gV_{BS} represents modeling of body effect in terms of linear approximation. The body effect is not experienced by the lower device because $V_{GS} = 0$.

2.1 LECTOR TECHNIQUE

The LECTOR technique is an efficient technique to reduce leakage power by inserting two leakage control transistors in the middle of pull-down and pull-up paths. These leakage transistors do not require any external control circuitry as the source of the NMOS transistor controls the PMOS transistor gate, and the source terminal of the PMOS leakage transistor controls the gate terminal of the NMOS leakage transistor. The substrate of PMOS is connected to power supply $V_{DD,}$ and the substrate of NMOS is connected to GND. These leakage transistors are arranged so that one transistor always works near the cutoff region out of these two. It works on the principle of stacking that is more than one-off transistor offers more resistance than a single off transistor, so with the increase in resistance, leakage power reduction is achieved. However, the drawback of technique is increased delay; as the resistance increases, there is an increase in RC delay. Here V_{th} is increased, and subthreshold leakage decreases due to reverse bias junction formation between source and substrate, and also, at the same time, it increases delay [16].

Moreover, the delay can be reduced by making the source and substrate junction less reverse bias, and this can be done by connecting the substrate of leakage transistors to the source of the leakage transistors. In other words, the substrate of NMOS leakage is connected to the source of the NMOS leakage transistor, and the substrate of the PMOS leakage transistor is connected to the source of the PMOS leakage transistor. This scheme is named the LECTOR-B approach. It will reduce delay compared to the LECTOR approach by making substrate source junction less reverse bias [17] [18].

When we go deeper into submicron technology, transistors are in the sub-threshold mode of operation, and the static current exponentially varies with gate-to-source voltage. Most CMOS-based logic circuits are composed of series-parallel combination of MOS transistors. Leakage current in parallelly connected MOS transistors is calculated by adding the sum of DC of the individual transistor connected in parallel. While in the case of series-connected transistors, the calculation of leakage current is done by considering nonlinear characteristics. When a transistor is in the sub-threshold region of operation, then the current analysis of the stack transistor arrangement is given by:

$$I_{S1} : I_{S2} : I_{S3} = 1.8\exp\left(\frac{\eta V_{DD}}{\eta V_T}\right) : 1.8 : 1 \quad (3)$$

where I_{si} (i=1,2,3) is the leakage current for stacked MOS transistors.

3. LOW LEAKAGE POWER DYNAMIC CMOS INVERTER AND SRAM CELL

Considering dynamic CMOS inverter, when input is '0' at that case, the output should remain at $V_{DD,}$ but charge leakage happens as shown in Fig.3, and the output voltage drops to $0.5V_{DD}$ for the simulated design.

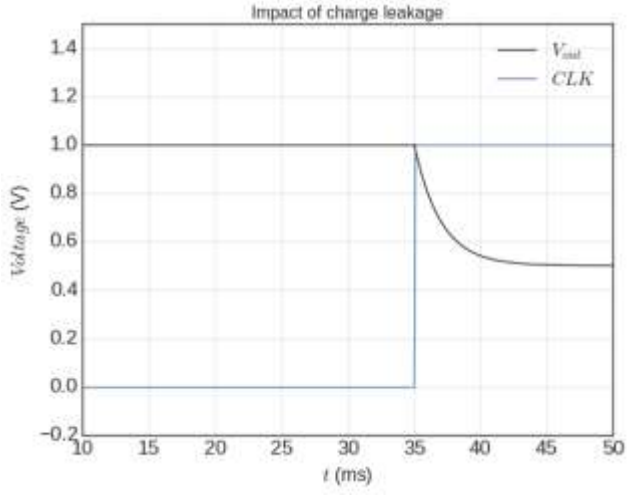

Fig.3. Impact of charge leakage

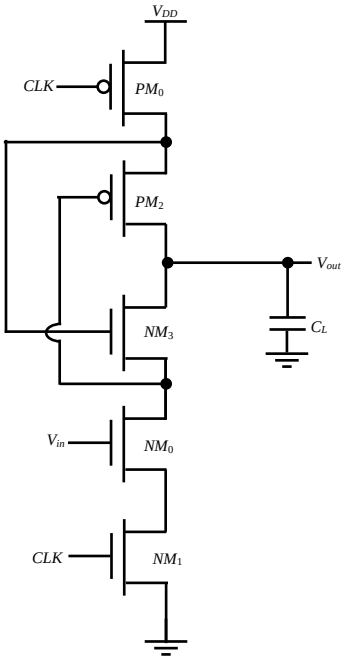

Fig.4. Schematic of dynamic CMOS inverter

The Fig.4 shows the design of a low-power dynamic CMOS inverter. In standby mode leakage power consumption of the circuit reduces—furthermore, the leakage offered by PMOS

transistor in the pull up path in the evaluation phase. Working can be understood by considering that the output is initially at $V_{DD.}$ When the circuit is in the precharge phase, the clock is '0' when PM0 is ON, and NM1 is OFF, irrespective of applied input capacitor will charge up to V_{DD} no discharge path from supply to ground.

3.1 LECTOR

Moreover, when the clock is $V_{DD,}$ that is logic '1'. In that case, the circuit is in the evaluation phase. The high clock turns off PM0 and turns on NM1. When applied input is logic '1' that will make NM0 turned on, PM2 (LCT1) is turned ON, and NM3(LCT2) is operated near cut off region. As it does not get a complete discharge path to the ground due to the OFF state of NM3, so it will give output nearly equal to V_{DD}. When the input is logic '0', it will turn off NM0 and turn on PM2. Again, it will not find the discharge path to the ground, so the output will nearly equal V_{DD}. The leakage introduced by pull-up PMOS (PM0) is reduced by making another transistor off simultaneously. As the resistance offered by two or more OFF transistors is more than a single OFF transistor, which will reduce the leakage current, this concept is known as forced stacking. [19]

The Fig.5 shows the schematic of the dynamic CMOS inverter using the LECTOR-B technique. The working is the same as the dynamic CMOS inverter using the LECTOR technique.

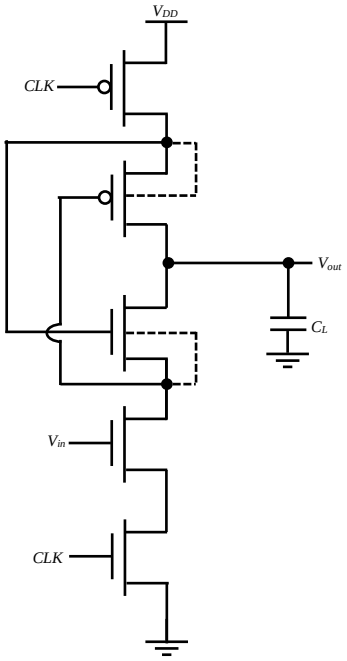

Fig.5. Schematic of dynamic CMOS inverter using LECTOR-B

Still, it offers less delay than the LECTOR approach, as the substrate of LCTs is connected to their sources, reducing the threshold voltage V_t and reducing the delay. Still, there is an increase in leakage current due to this V_t compared to the LECTOR technique.

The design of low-power SRAM cells has been analyzed, and results have been obtained in terms of static power, dynamic power, fall time and rise time. Firstly, these parameters have been obtained for conventional 6T SRAM cells, then SRAM has been analyzed using the LECTOR and LECTOR-B technique. And then, by using a transmission gate, the SRAM cell has been analyzed. Transmission gate SRAM cell reduces the leakage power but at the cost of an increase in delay. For that purpose, the single-ended transmission gate SRAM cell is analyzed [19].

Moreover, it reduces the leakage power as well as delay compared to conventional 6T SRAM cells. The Fig.6 shows the low-power single-ended transmission gate SRAM cell. Furthermore, the best results have been given by single-ended TG SRAM cell using the LECTOR-B technique.

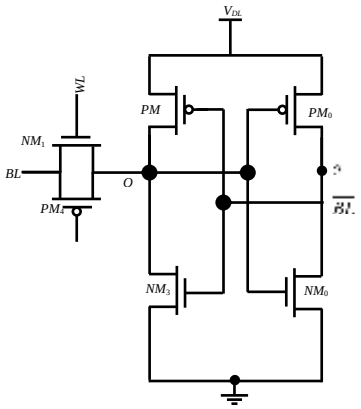

Fig.6. Schematic of single-ended transmission gate SRAM Cell

4. RESULTS AND DISCUSSION

This section analyzes the static and dynamic power loss of proposed circuits. The simulations have been carried out by the Cadence Virtuoso tool, and results have been evaluated for dynamic CMOS inverter, conventional SRAM cell, and SRAM cell with TG (transmission gate) at 45-nm technology node. The Table.1 shows the comparison that has been made for conventional dynamic CMOS inverter with LECTOR and LECTOR-B technique.

Table.1. Comparison of parameters of dynamic CMOS inverter using different approaches

Method	Dynamic Power	Static Power	Delay	PDP
LECTOR	20.5% ↑	19.2% ↓	52.8%↑	84%↑
LECTOR-B	10% ↓	17.88% ↓	0.7%↑	9.7% ↓

From Table.1, it has been concluded that the LECTOR technique reduces more static power compared to the LECTOR-B technique at the cost of an increase in delay. So, by transistor sizing, LECTOR-B is a good substitute for this problem, as mentioned above.

In SRAM cells, the calculations have been made for conventional SRAM cells with LECTOR and LECTOR-B technique.

Table 2. Summary of comparison of various SRAM cell parameters

Method	Static Power	Rise Time	Fall Time
LECTOR	26.5% ↓	381.9%↑	35.54%↑
LECTOR-B	19.15% ↓	253.8%↑	22.15%↑

Table.3. Comparison of various parameters of TG8T SRAM cell

Method	Static Power	Rise Time	Fall Time
LECTOR	26.43% ↓	71%↑	62.16%↑
LECTOR-B	25% ↓	34%↑	45.3%↑

Table.4. Summary of comparison of various single-ended TG SRAM cell parameters

Method	Static Power	Rise Time	Fall Time
LECTOR	0.983% ↓	0.0567%↑	0.304%↑
LECTOR-B	0.948% ↓	0.0118%↑	0.2077%↑

In the 6T SRAM cell case, static power is reduced by 26.5%, the rise time is increased by 381.9%, and the fall time is increased by 35.54% using the LECTOR technique. Using LECTOR-B, static power is reduced by 19.5%. Here, the rise time is increased by 253.80%, and the fall time is increased by 22.15%. So, to further reduce the static power transmission gate is used instead of the access transistor. Furthermore, to speed up the operation or reduce the delayed single-ended transmission gate is used, it gives the best result in terms of leakage power and the delay. In this static power is reduced by 98.3%, the rise time is increased by up to 5.67%, and the fall time is increased by 30.4% using the LECTOR approach. Moreover, by using the LECTOR-B approach, there is a 94.8% decrease in static power, the rise time is increased by 1.18%, and the fall time is increased by 20.77%.

5. CONCLUSIONS

With all the results mentioned above, it is best to use a single-ended TG SRAM cell using the LECTOR-B approach. Where the noise margin is an essential requirement, this can be used. However, there is a problem it will increase the transistor count compared to conventional 6T SRAM cells. Delay is also increased up to some extent by using LECTOR-B. Delay can be further reduced by using the inverter chain at the output. The same cell can be further analyzed at technology nodes other than 45nm like 32nm, 22nm, technology node.

REFERENCES

[1] A. Agarwal, S. Mukhopadhyay, A. Raychowdhury, K. Roy and C.H. Kim, "Leakage Power Analysis and Reduction for Nanoscale Circuits", *IEEE Micro*, Vol. 26, No. 2, pp. 68-80, 2006.

[2] Jian Hong Yang, Gui Fang Li and Hui Lan Liu, "Off-State Leakage Current in Nano-Scale MOSFET with Hf-based Gate Dielectrics", *Proceedings of IEEE International Conference on Nanoelectronics*, pp. 1189-1192, 2008.

[3] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits", *Proceedings of IEEE*, Vol. 91, No. 2, pp. 305-327, 2003.

[4] Dongwoo Lee, D. Blaauw and D. Sylvester, "Gate Oxide Leakage Current Analysis and Reduction for VLSI Circuits", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 2, pp. 155-166, 2004.

[5] A.P. Shah, V. Neema and S. Daulatabad, "Effect of Process, Voltage and Temperature (PVT) Variations In LECTOR-B (Leakage Reduction Technique) at 70 nm Technology Node", *Proceedings of IEEE International Conference on Computer, Communication and Control*, pp. 1-6, 2015.

[6] N. Hanchate and N. Ranganathan, "LECTOR: A Technique for Leakage Reduction in CMOS Circuits", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 2, pp. 196-205, 2004.

[7] M. Leela, S. Rooban and C. Joshitha, "Comparative Analysis on Low Power SRAMs", *Materials Today Proceedings*, Vol. 23, No. 2, pp. 1-13, 2020.

[8] P. Verma and R.A. Mishra, "Leakage Power and Delay Analysis of LECTOR based CMOS Circuits", *Proceedings of International Conference on Computer and Communication Technology*, pp. 260-264, 2011.

[9] M.C. Johnson, D. Somasekhar, Lih Yih Chiou and K. Roy, "Leakage Control with Efficient Use of Transistor Stacks in Single Threshold CMOS", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 1, pp. 1-5, 2002.

[10] R. Giterman, M. Vicentowski, I. Levi, Y. Weizman, O. Keren and A. Fish, "Leakage Power Attack-Resilient Symmetrical 8T SRAM Cell", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 26, No. 10, pp. 2180-2184, 2018.

[11] B. Kankanala, A. Srinivasulu and S. Musala, "7-T Single End and 8-T Differential Dual-Port SRAM Memory Cells", *Proceedings of IEEE International Conference on Information and Communication Technologies*, pp. 1243-1246, 2013.

[12] R. Gupta, S.S. Gill and N. Kaur, "A Novel Low Leakage and High Density 5T CMOS SRAM Cell in 45nm Technology", *Proceedings of IEEE International Conference on Recent Advances in Engineering and Computational Sciences*, pp. 1-6, 2014.

[13] N. Yadav, S. Dutt and G.K. Sharma, "A New Sensitivity-Driven Process Variation Aware Self-Repairing Low-Power SRAM Design", *Proceedings of IEEE International Conference on VLSI Design*, pp. 116-121, 2014.

[14] J.M. Rabaey, A. Chandrakasan and Nikolic Borivoje, "*Digital Integrated Circuits*", 2nd Edition, Pearson Education, 2003.

[15] S.M. Kang, C.W. Kim and Y. Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", 4th Edition, McGraw-Hill India, 2019.

[16] T.K. Gupta and K. Khare, "Lector with Footed-Diode Inverter: A Technique for Leakage Reduction in Domino Circuits", *Circuits, Systems, and Signal Processing*, Vol. 32, No. 6, pp. 2707-2722, 2013.

[17] G. Pasandi and S.M. Fakhraie, "A 256-kb 9T Near-Threshold SRAM With 1k Cells per Bitline and Enhanced Write and Read Operations", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, No. 11, pp. 2438-2446, 2015.

[18] V.S. Baghel and S. Akashe, "Low Power Memristor based 7T SRAM using MTCMOS Technique", *Proceedings of IEEE International Conference on Advance Computing and Communication Technology*, pp. 222-226, 2015.

[19] C.A. Kumar, B.K. Madhavi and K. Lalkishore, "Performance Analysis of Low Power 6T SRAM Cell in 180nm and 90nm", Proceedings of IEEE International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics, pp. 351-357, 2016.