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MEMRISTOR BASED 12T SRAM CIRCUIT USING SLEEPY STACK APPROACH IN 180NM TECHNOLOGY

Priyanka[1] and Omer Majeed Bhat[2]

[1]Department of Electronics and Communication Engineering, Indira Gandhi Delhi Technical University for Women, India
[2]Department of Electronics and Communication Engineering, Mewat Engineering College, India

Abstract

Leakage current has been a vital issue in system on-chip systems with the contemporary sub-micron advancements. It has consequently turned out to be vital to control the current and address the issue from the architectural level. This paper presents different models of Static Random Access Memory (SRAM) cells to diminish the leakage current. The types of leakage current considered in this paper are gate leakage and sub threshold leakage. Two traditional leakage reduction methods have been connected to 6T SRAM cell with memristor and results have been analysed. This is a non-volatile memory since it utilizes memristor. Non-volatile 6T SRAM cell with stack and sleep transistor indicates a significant decline in leakage current when compared with basic 6T SRAM cell. All the proposed work has been completed by utilizing Cadence Virtuoso at 180nm technology.

Keywords:

SRAM, Memristor, Sleepy Stack, Leakage Current

1. INTRODUCTION

As the VLSI technology is increasing, the memories are also increasing. Memory is nothing but it is a collection of storage cell with proper input and output and it is widely used to design computer, mobile phones and other similar devices [1].One type of these memories is SRAM. It is volatile in nature that implies information is put away, when power is plugged in, and as the power is plugged out information will get lost. The word static indicates that it does not need refreshing technique. It is type of semiconductor memory and it utilize quantities of transistors to store a single piece. It diminishes the delay between the processor and memories. These points of interest of SRAM are utilized to plan batteries for portable framework like mobile telephones, laptops and other electronic devices [2]. To design these devices from SRAM, low power and leakage parameters are crucial because in recent years' technology is scaling down rapidly. So we apply some techniques to design SRAM to achieve low power for high performance of the circuits. In this paper, sleep stack technique and memristor have been applied to design SRAM to reduce average power in comparison to the simple SRAM. In this paper, parameters like leakage power and delay has also been calculated.

A typical SRAM memory cell consists of four transistors that are arranged into two cross-coupled inverters[1] and have two stable states, "0" and "1". Two extra transistors are also required to control the memory cell during read and write operation which is known as the access transistors [2]. These extra transistors are used to implement the additional port's functionality in the register file of the SRAM.

The energy consumed by a circuit is divided into 3 different components [2], dynamic, static (or leak) and short circuit energy consumption. Dynamic energy is consumed when the signals that cross the CMOS circuits change its logical state of loading and unloading the output node capacitor. Leakage energy consumption is the energy consumed by sub-threshold currents and by inversely polarized diodes in a CMOS transistor. Short circuit power is the power consumed when both pull-up and pull-down networks are on simultaneously for some fraction of second.

2. LITERATURE REVIEW

Baghel and Akashe [1] proposed Multi Threshold CMOS (MTCMOS) based 6T and 7T Memristor Static Random Access Memory (SRAM) has been implemented and reduces parameters like delay, average power and leakage power. This is a non-volatile memory because it uses Memristor. Memristor is a forth missing non-linear resistor which acts as memory and it improves the power and speed. In this paper MTCMOS method is utilized, recently it is exceptionally popular in industry. It is a power lessening procedure that helps in decreasing leakage power in the SRAM by turning of the inactive circuit's areas.

Wasankar and Bhande [3] proposed MTCMOS (Multi Threshold CMOS) strategy is utilized recently it is extremely well known in the scholarly community and industry. It is a power decreasing procedure that helps in diminishing leakage power in the SRAM by turning of the idle circuit spaces. Outlining and calculation of parameters of simple SRAM, Memristor based SRAM and MTCMOS based Memristor SRAM has been finished with CMOS Design tool at 45 nm technology.

Almurib and Kumar [4] proposed a novel memristive SRAM cell is outlined utilizing seven transistors and one Memristor (7T1M). In this 7T1M SRAM cell, the non-volatile functionality is accomplished by including a single Memristor and a transistor to the plan of a volatile SRAM cell. The outlining of the 7T1M SRAM cell also presents VC-TRL which allows bidirectional current flowing through the Memristor, rather than relying on complementary info sources which would require more plan segments. In this article, memristive SRAM cells available from the literature are simulated utilizing a similar simulation condition for a reasonable examination. Simulations show that the 7T1M SRAM cell has the least power utilization against other memristive SRAM cells in the literature. The 7T1M SRAM cell works with a normal switching rate of 176.21ns and a normal power utilization of 2.9665μW. The 7T1M SRAM cell has a vitality delay-territory item value of 1.61, which is the lowest among the memristive SRAM cells available in the literature.

Pal and Islam [7] proposes a new SRAM cell that can work perfectly fine even below the subthreshold region and hence can be used in ultralow power applications. The robustness of this cell is measured by the Read SNM and the results obtained were compared with the traditional ones. The proposed cell has 1.83

times faster read operation and 1.47 times less PVT fluctuations compared to the traditional 6T SRAM cell it also has the high reliability as it has 1.40 times higher read SNM. If we talk about the write operation it has 3.86% faster write and the write operation is 18.4% less affected by the PVT fluctuations compared to the traditional 6T SRAM cell and has 2.33% higher write SNM compared to the traditional SRAM cell.

Zhu and Kursun, 2014 [8]: "A comprehensive comparison of superior triple-threshold-voltage 7-transistor, 8-transistor, and 9-transistor SRAM cells". In this paper, triple-threshold-voltage has been applied on three different architectures of SRAM cells which are 7T, 8T and 9T. The results are then compared on the basis of layout area, data stability, write voltage margin, idle mode leakage currents, data access speed, and active power consumption in a 65nm CMOS technology on Cadence Virtuoso tool. The single ended and differential read/write schemes are also compared for data access speed and power consumption in SRAM circuits.

3. LEAKAGE CURRENT

Leakage current is the unintended loss of electrical current or electrons. It is measured in amperes (A). An SRAM cell works in inactive state, when the word line is kept low and the bit line is kept at VDD. These inactive states come in between read and write operations. Even when the transistors are inactive, they dissipate some of the power which is known as the leakage power depending upon the value stored in the cell. This leakage current have primarily two dominant type of leakage mechanism viz., sub threshold leakage and gate leakage. Main contribution in the gate leakage current is because of carriers tunnelling through gate oxide and injection of hot carrier from substrate to the gate oxide.

Another important leakage mechanism is Gate-induced drain leakage (GIDL) which occur below the gate-drain overlap region because of the depletion at the drain surface. With increase in the leakage current, effective actions are need to be taken to reduce leakage power otherwise the static power consumption will affect the switching component of devices. To oppose SCEs, we cannot reduce the channel length randomly even if lithography permits it. The most unwanted SCE is the reduction of the threshold voltage which allows the device to turn on early especially at high drain voltages. Therefore new technologies, designs and device structures must be developed to keep balance between the small dimensions of the device and SCEs. In order to improve short-channel characteristics another technique apart from thickness scaling of gate oxide and scaling of junction is using engineering well. By varying the doping profile in the channel region, we can vary the spread of the electric field and potential curves. The goal of enhancing the channel profile is to reduce the leakage of off-state and maximize the currents in linear and saturation region. Super steep retrograde wells and halo implants are used as to reduce the channel length and improve the transistor's drive current with no triggering the leakage current in off-state. Till recent, the drain source sub-threshold current had been thought to be the dominant leakage mechanism. And there have been a number of techniques proposed to decrease drain to source sub-threshold leakage when the SRAM is in the inactive state.

4. MEMRISTOR

Memristor was created by Leon O. Chua in 1971 and as indicated by Chua, "Memristor is a fourth missing, two terminal passive elements with variable resistance also called as Memristance that give relation between flux (Φ) and charge (q)" [1]. This relation is represented in Fig.1.

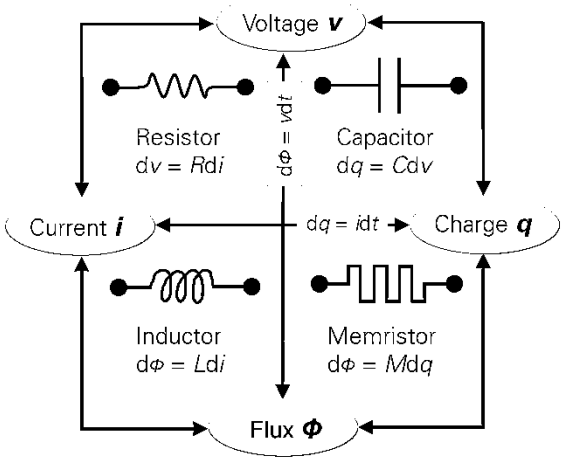

Fig.1. Memristor

Memristor is characterized as a two terminal non-volatile device in which the magnetic flux (Φ) between the terminals is an element of the measure of electric charge (q) that has gone through the device and it is indicated by M and its unit is ohm. Memristor has non-volatile, fast read/write time, good scalability and compatibility with CMOS technology over the simple SRAM. These advantages of Memristor help in the design of low power SRAM.

5. LEAKAGE REDUCTION TECHNIQUES

5.1 SLEEP APPROACH

Sleep transistors can be used in many ways, but mostly it is used to increase the resistance of V_{DD} to ground path and hence reduces the leakage current [2]. These sleep transistors turn on when circuit enters into active state and turns off when circuit enters into off or standby state. Sleep transistors are added between logic block and V_{DD} and between logic block and ground and hence break the connection of the logic block from the power supply and ground and results into reduction in leakage power in the standby mode.

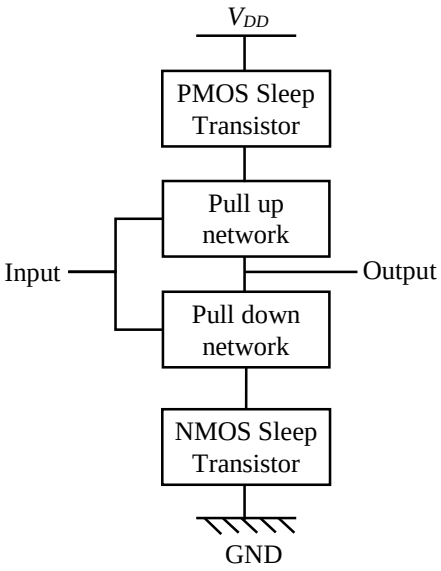

Fig.2. Sleep approach for leakage reduction

5.2 STACK APPROACH

In this technique, two extra PMOS and two extra NMOS transistors are associated with regular circuit block to control the leakage current. These leakage control transistors will work close to cutoff region. As a result, the resistance in conducting state will be lower than off state resistance. In this way very little conduction happens and total resistance from V_{DD} to ground increases because of which leakage current reduces.

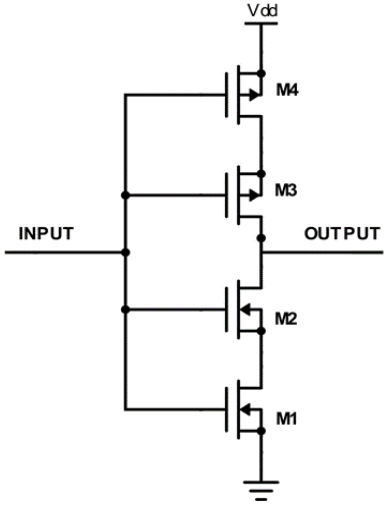

Fig.3. Stack approach for leakage reduction

5.3 SLEEPY-STACK APPROACH

In sleepy stack approach, both sleep and stack techniques are applied together [3]. Both sleep transistors turn off in standby mode and further leakage current is reduced by the stacking effect.

6. EXISTING SRAM CIRCUITS

6.1 6T SRAM CELL

A SRAM cell should have the capacity to read and write information and to hold the information till the power remains connected. A normal flip-flop could achieve this, but the size is very large. Fig.4. demonstrates a standard 6-transistor (6T) SRAM cell that can be in order of magnitude smaller than a flip-flop [6]. The 6T cell achieves its little size at the cost of more unpredictable hardware for read and write operation. 6T SRAM cell shows that it utilizes six transistors having two PMOS transistors and four NMOS transistors. Two PMOS and two NMOS transistors together make two cross coupled inverters in which one PMOS and one NMOS frame one inverter. Two different NMOS transistors are access transistors and these six transistors together structures one basic 6T SRAM cell. In 6T SRAM cell, there are two bit lines namely BL and BLB and one word line WL along-with two outputs Q and QBAR. BL and BLB are inverse of each other. Same goes for Q and QBAR.

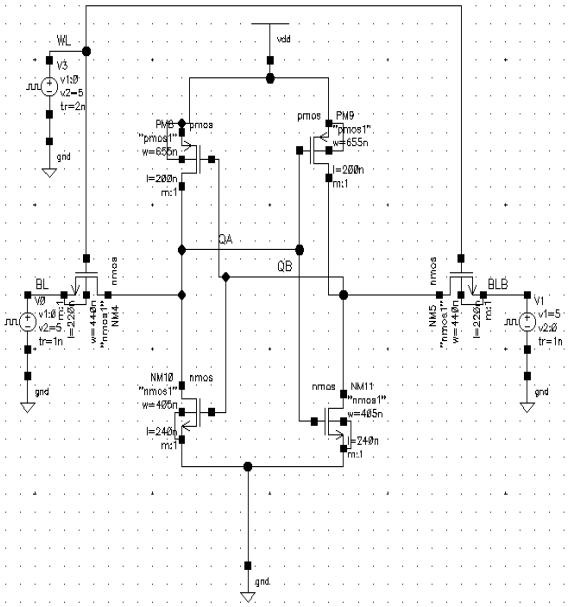

Fig.4. 6T SRAM Cell

6.2 8T SRAM CELL

8T SRAM cell is implemented by including NMOS and PMOS sleep transistors to basic 6T SRAM circuit. Sleep transistors are the two additional transistors associated with the SRAM circuit block [6].

As shown in Fig.5, PMOS M8 sleep transistor is associated between VDD and pull up system and NMOS M9 sleep transistor is associated between pull down system and ground. At the point when SRAM cell is in active state then both sleep transistors stay in on state. The voltage at source node of sleep NMOS transistor is the difference between the power supply and threshold voltage of NMOS. The voltage at source node of PMOS sleep transistor is equivalent to negative of threshold voltage of PMOS. With the reduction in voltage, the power also lessens.

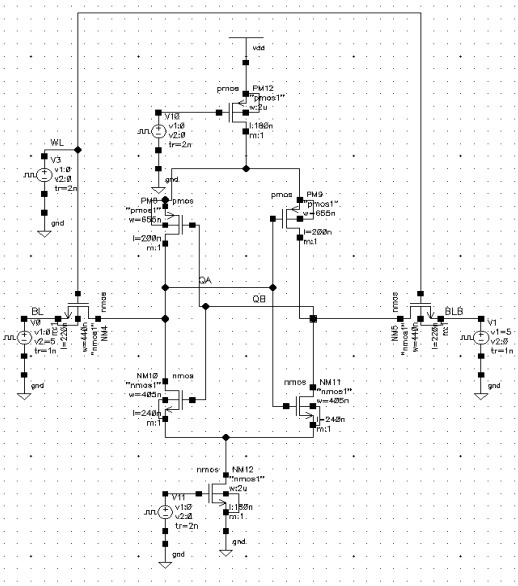

Fig.5. 8T SRAM Cell

6.3 MEMRISTOR BASED 8T SRAM CELL

Memristor based 8T SRAM cell is implemented by including two memristors to 8T SRAM circuit for leakage lowering. Here, memristor M1 is connected between PMOS P1 and PMOS P3 [1]. Similarly, memristor M2 is connected between PMOS P2 and PMOS P3.This configuration is used to lower the leakage current as well as leakage power [7].

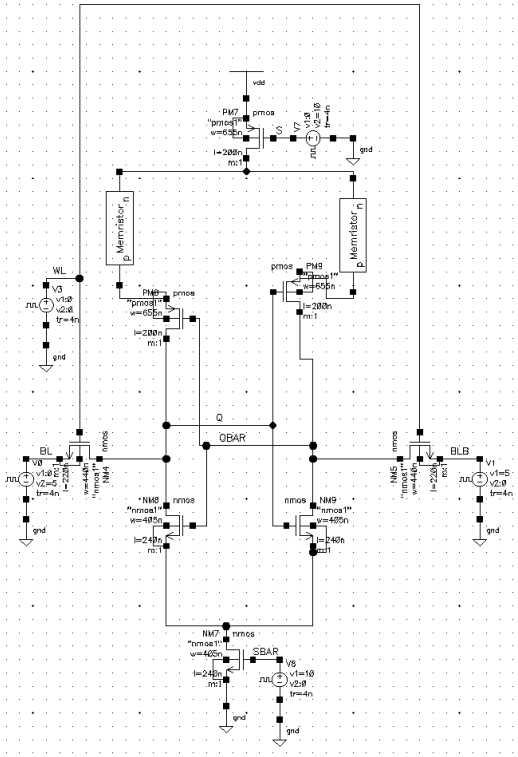

Fig.6. Memristor based 8T SRAM

7. PROPOSED SRAM CIRCUIT

7.1 MEMRISTOR BASED 12T SRAM CELL

12T memristor based SRAM cell is outlined by applying both stacking and sleep technique to deal with 6T SRAM cell to additionally lessen the leakage current as shown in Fig.7. The schematic of 12T SRAM cell with both stacking and sleep transistors is shown in Fig.7. Together these eight transistors form two cross coupled inverters. These are also known as leakage control transistors. At the point when SRAM cell is in standby mode then both the sleep transistors are in cut off state and because of stacking of transistors, there is significantly less leakage current. There is an increment in the area because of additional transistors and wires for sleep and stack transistors.

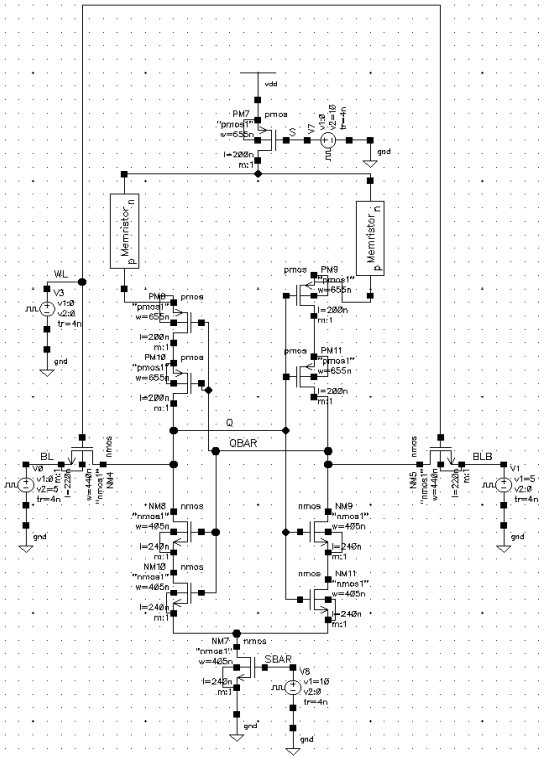

Fig.7. Memristor based 12T SRAM

8. RESULT

In this paper, we have designed Memristor based SRAM and have compared it with the existing SRAM SRAM models on the basis of leakage power and average power.

- **Average Power:** It is the average amount of energy transferred per unit time or work done per unit time. Unit of average power is watt (W).
- **Leakage Current:** Leakage current is the unintended loss of electrical current or electrons. It is measured in amperes (A). It decreases the capacity of the devices.

The Table.1 provides the leakage current and average power in different SRAM models after adopting various techniques.

Table.1. Different Parameters of nT SRAM Cells

Circuit	Technique Used	Leakage Current (pA)	Average Power (nW)
6t SRAM	Basic	418.739	52.32
8T SRAM	Sleep	11.61	40.24
Memristor based 8T SRAM	Sleep	6.89	12.48
Memristor based 12T SRAM	Sleepy-Stack	2.05	8.61

The Fig.8 shows the comparison of leakage current of various nT SRAM cells based on Memristor and shows a significant reduction in leakage current as we increase the number of transistors. Memristor based 12T SRAM shows the least leakage current. The leakage current of Memristor based 12T SRAM has been reduced by 70.2% as compared to Memristor based 8T SRAM cell.

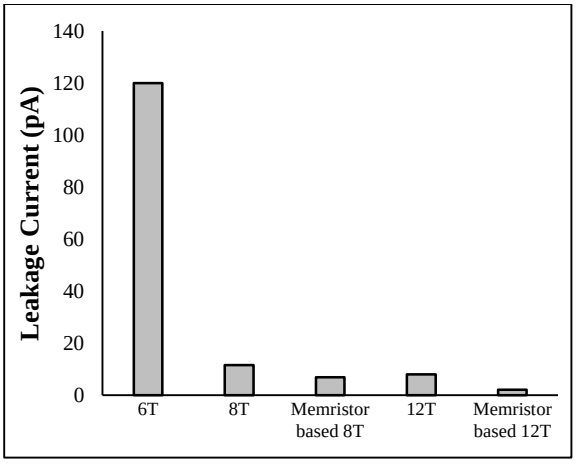

Fig.8. Comparison of leakage current of nT SRAM cells

9. CONCLUSION

The simulation of memristor based 12T SRAM cell has been carried out successfully with the help of cadence virtuoso on 180nm technology at 25 degree Celsius. The compared parameter is leakage current and average power. The relative analysis of the results demonstrates that, leakage reduction technique when combined with memristor based 6T SRAM (8T and 12T) indicates better performance when contrasted with traditional 6T SRAM. Memristor based 6T SRAM cell with sleep and stacking approach (12T model) is the better leakage reduction procedure and it yields better leakage current reduction and an increase in the area when contrasted with basic 6T SRAM cell.

REFERENCES

[1] V.S. Baghel and S. Akashe, "Low Power Memristor based 7T SRAM using MTCMOS Technique", *Proceedings of 5th International Conference on Advanced Computing and Communication Technologies*, pp. 222-226, 2015.

[2] M.R. Asati and N. Singh, "Leakage Power Optimization by Sleepy Keeper Gate Replacement Techniques", *International Journal of Scientific and Engineering Research*, Vol. 5, No. 2, pp. 866-873, 2014.

[3] M.R.S. Wasankar and A.E. Bhande, "Power Effective Memristor Based SRAM using MTCMOS", *International Journal of Engineering Research and General Science*, Vol. 4, No. 1, pp. 164-167, 2016.

[4] P.W. Ho, H.A.F. Almurib and T.N. Kumar, "Memristive SRAM Cell of Seven Transistors and One Memristor", *Journal of Semiconductors*, Vol. 37, No. 10, pp. 16-24, 2016.

[5] P.S. Aswale and S.S. Chopade, "Comparative Study of different Low Power Design Techniques for Reduction of Leakage Power in CMOS VLSI Circuits", *International Journal of Computer Applications*, Vol. 70, No. 11, pp. 1-7, 2013.

[6] R. Sharma, R. Antil and K. Kumar, "Comparative Study of 6T and 8T SRAM using Tanner Tool", *International Journal of Computer Science and Mobile Computing*, Vol. 4, No. 1, pp. 211-221, 2015.

[7] S. Pal and A. Islam, "Device Bias Technique to Improve Design Metrics of 6T SRAM Cell for Subthreshold Operation", *Proceedings of 2nd International Conference on In Signal Processing and Integrated Networks*, pp. 865-870, 2015.

[8] H. Zhu and V. Kursun, "A Comprehensive Comparison of Superior Triple-Threshold-Voltage 7-Transistor, 8-Transistor, and 9-Transistor SRAM Cells", *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 2185-2188, 2014.