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A LOW POWER PROGRAMMABLE BANDPASS FILTER FOR DIGITAL RADIO MONDIALE

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Abstract
In this paper, an inverter based transconductor using double CMOS pair is proposed for implementation of a programmable bandpass filter suitable for Digital Radio Mondiale (DRM). Major contributions of this paper are: proposal for operating the transconductance (G_m) stage in sub-threshold region in order to minimize the power dissipation, proposal for switching in different Gm cells with suitable dummy stages for varying the centre frequency (F-tuning) and filter pass band (Q-tuning), proposal for a digital tuning technique for the filter based on phase comparison method for PVT compensation. The filter circuit is based on a biquad G_m-C topology, which is designed and implemented on CMOS 0.18µm technology with 1.8V supply using gm/Id design methodology. The post layout simulation results demonstrate the tunability of the centre frequency from 2MHz to 11MHz with quality factor tunable up to 50, which meets the requirements of DRM (upto 30MHz). Post layout simulation results show that the filter exhibits an in-band dynamic range of 53dB at gain of 7dB. An input IP3 of up to 28dBVp is achieved for an input signal of 100mVp. The SFDR over the entire bandwidth is 57dB. These features are obtained for a total power consumption of less than 300 µW from a single 1.8 V power supply with an estimated silicon area of 0.3mm^2. The proposed approach guarantees the upper bound on THD to be -40dB for 300mV$_{pp}$ signal swing. The use of inverters with double CMOS pair results in 34dB higher PSRR compared to those using push pull inverter.

Keywords:
Continuous Time Filter, Sub-Threshold, Intermediate Frequency (IF) Bandpass Filter, Double CMOS Pair

1. INTRODUCTION

Transconductors have a wide range of applications in the area of analog signal processing [1], [2]. Continuous time filters implemented with transconductance amplifiers and capacitors are known as G_m-C or OTA-C filters and are very popular for a host of applications such as IF filters, hard disk drive filters, LC-oscillators and RF filters. A number of architectures have been proposed in the literature for the transconductor. The transconductor using double CMOS pair is proposed in [3] and it has been used to implement video frequency filter [4]. The scheme proposed by Nauta in [5] uses push pull inverters for realizing the transconductor and has the advantage of large bandwidth due to the absence of internal nodes. However, for realizing programmable filters using this scheme, the power supply voltage needs to be varied. This is not suitable for low voltage applications and it results in poor power supply rejection ratio (PSRR).

In this paper, we propose a band pass filter for Digital Radio Mondiale [21]. Some of the band pass filters proposed in the literature have a number of disadvantages. For example, for applications requiring low IF range, large values of capacitors are required to make use of the architecture in [5]. Similarly, the filter proposed in [6] which uses Nauta's architecture for bluetooth applications, requires large capacitors and consumes more silicon area. The schemes reported in [3]-[6] are not suited for low power applications. Log domain filtering with a tuning range of 30KHz - 10MHz is proposed in [7]. The accuracy of the above scheme relies on the matching between log and anti-log conversion circuits. To achieve wide bandwidth and also low power benefits, floating gate based techniques are used in [8] and [9]. The issue with the Floating Gate MOS (FGMOS) transistor is the trapped charge problem, which occurs during fabrication when an uncertain amount of charge is trapped on the floating gate and gives rise to large variations in threshold voltage. The implications of the trapped charge depend on the circuit in question, but often the design will not work unless the charge is removed. Field Programmable Analog Array (FPAA) based implementations are proposed in [10]. However, when used for high frequencies (MHz), parasitic resistances and capacitances of the switch introduce non linearity in frequency response, limiting the dynamic range of the filter. A CMOS bandpass filter for low IF bluetooth receiver based on current follower is reported in

This filter consumes considerable amount of power. Programmable monolithic G_m-C band-pass filter based on wide swing folded cascode architecture is achieved in [12], but with low quality factor. A digitally programmable biquad G_m-C band pass filter for FM application with independent centre frequency tuning and Q-tuning is proposed in [13]. The scheme in [13] requires two voltage sources, one for the filter core and the other for tuning circuitry. In this paper, separate voltage source for tuning circuit is dispensed with by using double CMOS pair operated in subthreshold region. In addition to this, the operation in subthreshold region can also result in lower power dissipation. Continuous time CMOS G_m-C filters with subthreshold operation has been already proposed for cochlea and other very low frequency applications.

In view of this, in this paper, a double CMOS pair operating in subthreshold region is proposed for the implementation of transconductor with the following features:

- To maintain the integrating capacitance constant over the entire programming range [15], a compact dummy-based switching scheme is proposed. This eliminates the switches in the signal path.
- DLL based digital tuning method using phase comparison method is implemented for PVT compensation.

The proposed bandpass filter has a wide tuning range suitable for low-IF receiver (see Fig.1) as depicted with gray shaded box.

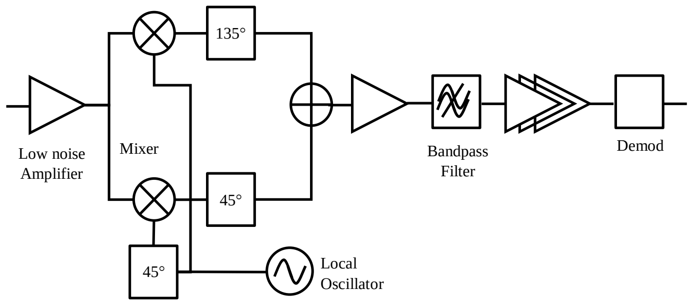

Fig.1. Low-IF Receiver Architecture

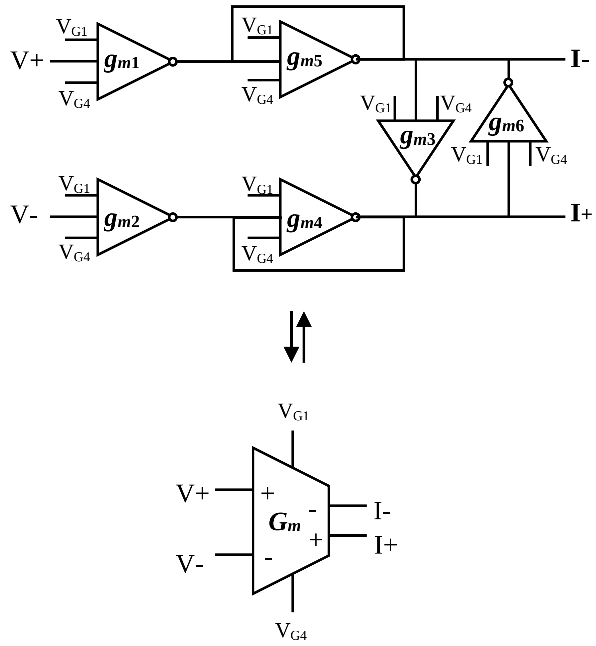

Fig.2. CMOS Pair based balanced G_m block

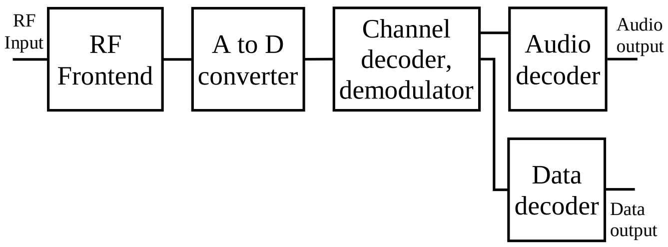

Fig.3. Functional Block Diagram of DRM Receiver

The following notation is used in this paper. The operational transconductance amplifier (OTA) shown in Fig.2, is denoted as G_m block. These G_m blocks are constructed using double CMOS pair [11] and is referred to as gm cell. The transconductance of the G_m block is referred to as G_m. The transconductance of the NMOS and PMOS devices forming the double CMOS pair is referred to as G_{mn} and G_{mp} respectively. Detailed analysis of G_m block operated in subthreshold region is given in [20].

This paper is organized as follows. Section 2 introduces the Digital Radio Mondiale. Section 3 presents the structure of the proposed digitally tunable band pass filter and its sub blocks including the F-tuning and Q-tuning schemes. The post layout simulation results are given in section 4 followed by the conclusions in section 5.

2. DIGITAL RADIO MONDIALE (DRM)

Digital Radio Mondiale (DRM; mondiale being Italian and French for “worldwide”) is a set of digital audio broadcasting technologies designed to work over the bands currently used for analogue radio broadcasting including AM broadcasting, particularly shortwave, and FM broadcasting. DRM is more spectrally efficient than AM and FM, allowing more stations, at higher quality, into a given amount of bandwidth, using various MPEG-4 audio coding formats. This section describes the DRM (Digital Radio Mondiale) receiver characteristics for consumer equipment intended for terrestrial reception operating in the frequency bands below 30 MHz (i.e. DRM robustness modes A to D, “DRM30”) and also those for the frequency bands above 30 MHz (i.e. DRM robustness mode E, “DRM+”). The specifications of this document, stresses the quality aspects of the RF frontend and baseband decoding [21].

The functional block diagram of DRM receiver is shown in Fig.3. In this work the first block, RF front end circuit is implemented using the subthreshold band pass filter.

3. DIGITALLY TUNABLE SECOND ORDER BANDPASS FILTER

The fully-differential G_m-C architecture of the digitally tunable second order bandpass filter based on double CMOS pair is shown in Fig.4. This uses digitally assisted centre frequency tuning (F-tuning) and the quality factor tuning (Q-tuning). In this circuit, G_{m1} is the V to I converter, the resistor is realized by G_{m2}, the inductor is realized by the Gyrator (G_{m3}, G_{m4} and C_2) and C_1 is the capacitor of resonant circuit. The transfer function of the bandpass filter with biquad structure is given by,

$$H(s) = sC_2G_{m1}/(s^2C_1C_2 + sC_2G_{m2} + G_{m3}G_{m4}) \tag{1}$$

From Eq.(1), the center frequency and the quality factor, Q, are given by,

$$\omega_0 = \frac{\sqrt{G_{m3}G_{m4}}}{\sqrt{C_1C_2}} \tag{2}$$

$$Q = \frac{\sqrt{G_{m3}G_{m4}C_1}}{G_{m2}\sqrt{C_2}} \tag{3}$$

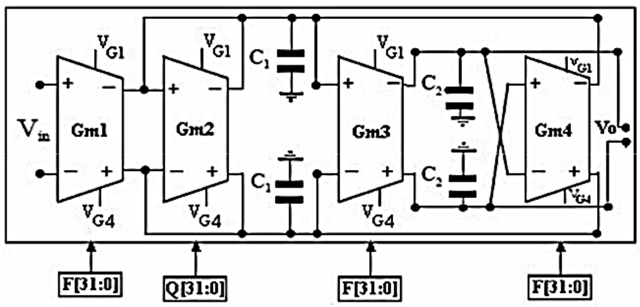

Fig.4. Schematic diagram of digitally tunable second order bandpass filter

In programmable continuous time filters, the center frequency and the quality factor of the filter can be tuned by varying G_m, which in turn is controlled by changing either the bias current or the device dimensions. From Eq.(2), the center frequency of the filter can be varied either by the constant-C or constant-G_m method. In constant-C technique, the load capacitance is maintained constant and the value of G_m is changed to alter the centre frequency of the filter. In constant-Gm technique, Gm is kept constant and the value of load capacitance is changed to alter the centre frequency of the filter. Detailed analysis of these two approaches is carried out in [15] based on noise, total capacitance required and power dissipation. It suggests that constant-C approach is suitable for tunable filter realizations. We follow the constant-C approach for both F-tuning and Q-tuning. To get Butterworth response (Q=0.707), the value of $G_{m2}=2G_{m1}$. In Fig.3, G_{m3} and G_{m4} are constructed by fully balanced architecture as in Fig.2 and they are identical. G_{m1} and G_{m2} blocks use only main transconductor cells g_{m1} and g_{m2} of Fig.2. The capacitors C_1 and C_2 of Fig.4 are realized by MOS capacitors. To obtain capacitors as linear as possible, we focus on the use of MOS structures available in digital CMOS processes in place of metal-metal structures. The regions of interest of the C-V characteristics are the "flat" parts where the two terminal MOS structure operates either in accumulation or in inversion. The source, drain and bulk terminal shorted together, forms one end of the capacitor (*Gnd*). The gate forms the other terminal of the capacitor. It can be shown that for certain gate to body bias voltages ($V_{gb}>V_t$) and for certain choice of process parameters, MOS accumulation capacitors tend to be more linear than inversion capacitors [15]. The distortion generated by a capacitor operating in inversion is higher than that generated by one operating in accumulation and, is a reason for considering accumulation capacitors. There is another advantage of operating in accumulation region: the capacitance is almost independent of the operation frequency.

3.1 TUNABILITY ISSUES

From Eq.(2), it is understood that G_{m3} and G_{m4} have to be varied for programmable centre frequency in constant C technique. G_{m3} and G_{m4} can be varied by varying the bias current or by combining the outputs of multiple transconductors. A number of CMOS linearized transconductors have been reported in the literature. Many of these cannot be optimally designed if their transconductance is to be variable. The transconductors exhibit varying excess phase shift and varying excess noise factor as their transconductance is varied [15]; each of these parameters attains its worst case value at opposite extremes of the programmable frequency range. This makes the design difficult and results in suboptimum performance. An alternative, which does not suffer from the above problems, is to construct transconductors using optimized unit transconductor cells and switching these in parallel to achieve the desired programmable transconductance values [15]. We follow the unit transconductor cell approach for both F-tuning and Q-tuning.

3.2 CONSTANT CAPACITANCE SCALING

If switchable unit cells are used to implement the programmable transconductance (G_m), then each time such cells are switched in and out, the total value of the parasitic capacitance at each node changes, in a manner that is very difficult to control. Programmability using a parallel connection of conventional cascoded differential pairs which satisfies constant capacitance scaling has been already reported in [15]; however, these structures are not suitable for low-voltage supply. To mitigate this problem, a compact dummy based switching scheme which maintains constant capacitance is proposed next. This scheme dispenses with the need for switches in the signal path. The transistors M_1 and M_4 of the double CMOS pair acts as switches to include or exclude the gm cell to achieve the desired programmable transconductance values. The Fig.5 shows the programmable transconductor cell with dummies. M_1-M_4 refers to the main transconductance cell of double CMOS pair and M_{1d} - M_{4d} correspond to the dummy cell, introduced to make the capacitance at the input nodes constant. The dimensions of dummies are same as that of main transistors. The input signal is given to both the gates of M_2, M_3 and M_{2d}, M_{3d} transistors. From Fig.5, it may be noted that when b_0=1 (1.8V) and b_0'=0 (0V), the main transconductor will be switched on (M_1 and M_4 operates in weak inversion), and the dummy will be in off state (M_{1d} and M_{4d} are in cut off region) and vice versa. A simple MUX is used to accomplish the switching in and out of main cell and dummy. In both the cases, all the nodal capacitances in the circuit remain the same, thus exhibiting true constant capacitance scaling. Notice that when the transistors M_1 and M_4 are turned off, transconductance and conductance in the network is removed, while parasitic capacitance remains the same. The output is taken only from the main transconductor cell and not from the dummy and hence the output capacitance will vary marginally, but since the load capacitance chosen is 1pF which is more dominant and hence the centre frequency will not vary much due to the variation in output capacitance.

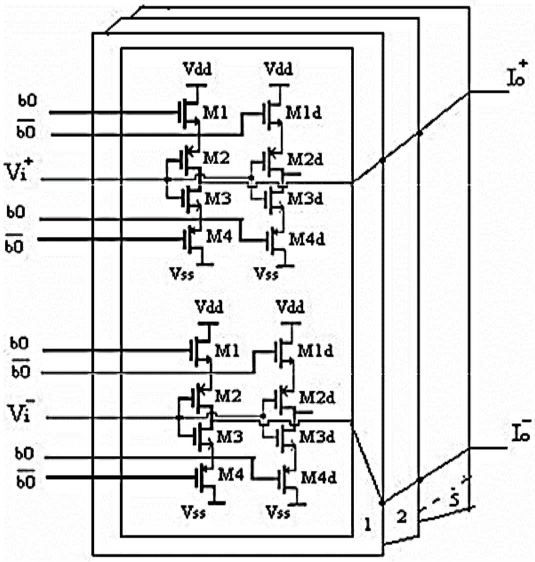

Fig.5. Programmable transconductor cell with dummies (G_{m1} block of Fig.4)

3.3 F-TUNING

The objective of this paper is to realize a bandpass filter with centre frequency tunable from 2MHz to 11MHz. The dimensions of unary gm cell consisting of M_1-M_4 transistors (N-MOS/P-MOS) in double CMOS pair are to be chosen such that the minimum centre frequency is 2MHz. The centre frequency is tuned by switching in suitable number of transconductance cells. The no. of unary cells to be switched in depends on the highest centre frequency required. Let N denote the total number of unary cells switched in. The digital tuning circuit generates the respective bit streams $F[N:0]$ depending on the cutoff frequency. This in turn decides the number of cells to be switched in. To make the filter work satisfactorily for all process corners, the number of unary gm cells should be chosen to be more than that required for the highest centre frequency at TT corner.

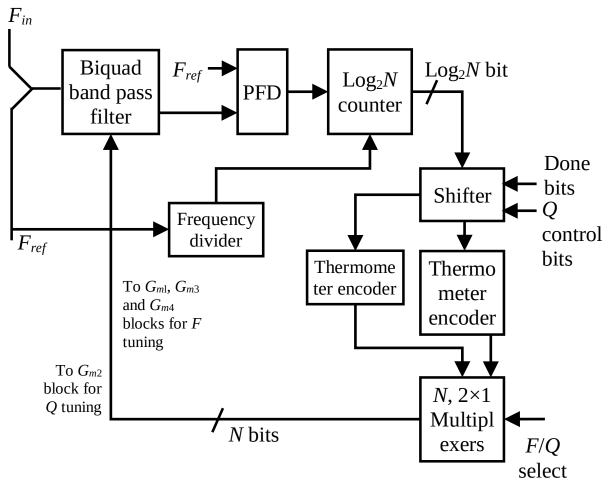

Fig.6. Block diagram of digital tuning circuit

3.4 Q-TUNING

The pass band of the band pass filter can be varied by varying the quality factor. From Eq.(3), if the product $G_{m3}G_{m4}C_1 / C_2$ is fixed, then the Q-factor is controlled by G_{m2} alone. To increase the Q-factor, the transconductance of the G_{m2} block has to be reduced. Once F-tuning is completed, the control bits $Q[N:0]$ from digital tuning circuit will decide the number of G_{m2} cells to be switched in.

3.5 DIGITAL TUNING BASED ON PHASE COMPARISON

The cut off frequency of the filter depends on the time constant C/G_m and may deviate by 35% of its nominal value due to the uncertainties in the fabrication process, temperature variations and aging. In order to obtain the required cut off frequency, there should be a provision to alter the parameters of the filters after fabrication. Any process variation and temperature dependencies can be compensated by tuning either the transconductance value or the MOS accumulation capacitor value or both. For higher order filters, a digital automatic tuning technique is proposed in [17] using phase comparison method. The above technique uses PLL based reference frequency source to tune the filter. In this paper, it is assumed that DLL based clock source [18] is available for tuning and it is an off-line tuning process. The Digital-Tuning method based on Phase Comparison (DTPC) uses phase information of the filter output signal to tune the cut off frequency. The tuning circuit proposed is shown in Fig.6. It consists of a Phase Frequency detector (PFD), a 5 bit counter, 5-31 thermometer decoder, 32 channel multiplexer, shifter and frequency divider.

3.5.1 Principle:

In biquad filter, both band pass and low pass outputs are available. From Eq.(4), band pass filter output will be in phase with the input signal, when a signal with frequency equal to the filter cutoff frequency is applied.

$$H_{BP(s)} = \frac{K_1 S}{S^2 + \frac{S^2}{Q} + \omega_0^2} \tag{4}$$

where K_1 is the gain of the band pass function, ω_0 is the cut off frequency of the filter and Q is the quality factor.

After fabrication, the filter may have arbitrary centre frequency. From DLL clock generator, the required frequency (F_{ref}) is applied to the tuning circuitry and also to the filter. The tuning circuit changes the filter parameters in such a way that the following condition is satisfied.

$$\varphi(F_{ref}) = 0^0 \text{ (or) } 360^0$$

where $\varphi(F_{ref})$ is the phase of the band pass output at cut off frequency. After tuning, the filter cutoff frequency becomes equal to F_{ref}. The filter design followed is based on g_m/I_d design methodology [13].

3.5.2 Circuit Implementation:

The filter cutoff frequency depends on the Gm value which in turn can be controlled by switching the required number of unary gm cells. The number of unary gm cells to be switched into the G_{m1} - G_{m4} blocks of Fig.6 is decided by the output of $\log_2 N$ bit counter. The binary counter output is converted to thermometer code F[N:0] before being applied to G_m blocks. The tuning circuitry uses the clock from the reference source in order to make the cutoff frequency to be equal to that of the reference source. On completion of tuning, the real time signals are applied to the filter. The phase difference between the reference signal and the band pass output can be detected by D-flip flop. Let N be assumed to be 32. Then, at reset or when the PFD output is 0, the 5 bit counter output is 00001, so that one of the 32 unary gm cells gets switched on respectively for the G_{m1}-G_{m4} blocks. This corresponds to minimum centre frequency (1.85MHz). If the binary output of the PFD is 0, then the phase is leading. In this case, the cut off frequency has to be increased and 5-bit counter counts up and decides the no. of unary gm cells to be switched on so as to meet the required cutoff frequency. If the phase detector output is 1, it implies that the output of the filter is lagging and the cutoff frequency of the filter needs to be decreased. This makes the 5-bit counter to count down till the filter tunes to the desired reference frequency. Once tuning process is completed, the counter will cease to count and thermometer decoder outputs are latched. The filter quality factor will be one at the completion of centre frequency tuning. To increase the quality factor of the filter, the number of unary gm cells to be switched in for Gm2 block has to be decreased and this is done by right shifting the counter outputs. The G_{m2} control is facilitated through 32 channel multiplexer, which allows F[31:0] when F-tuning process is active and Q[31:0] when quality factor control is required.

4. SIMULATION RESULTS

The second order programmable bandpass filter for DRM is implemented in TSMC 0.18µm CMOS technology with 1.8V supply voltage. The layout is drawn using Cadence Virtuoso XL(IC5141). Assura is used for DRC, LVS and parasitics extraction. The layout view with I/O pads is shown in Fig.7. The core area of the analog baseband block excluding digital tuning circuit occupies 0.3mm^2. The digital tuning circuitry for PVT compensation demands about 0.0275mm^2 silicon area and consumes 22µW. Dummies have been added to transconductor blocks to ensure matching. Simulated transconductance values versus differential input voltage (V_{id}) of the filter for various counter settings are shown in Fig.8. It can be observed from the results that transconductance value can be tuned from 18µS to 260µS, to cover the centre frequency range of 2 to 11MHz in TT corner. This bandwidth range is suitable for low IF applications. The DC bias current requirement varies between 16.6µA to 166µA. Switching of one unary gm cell yields 18µS. This corresponds to the centre frequency of 1.85MHz. Fifteen unary cells are required to obtain 11MHz in TT corner. However, 32 unary cells are implemented to account for PVT variations. The simulated magnitude responses of the filter at TT corner for counter settings of 1 to 15 are shown in Fig.9. The *Q*-tuning of band pass filter response for the centre frequencies 3MHz and 10.7MHz are shown in Fig.10. The *Q* values can be programmed between 0.707 and 50. To compensate for PVT variations, PVT tuning is also done. The Fig.11 shows the SFDR and total harmonic distortion (THD) versus input frequency for a 200mVpp signal. This gives about 53dB Dynamic Range for a -40 dB THD. From post layout simulation, it is estimated that the programmable bandpass filter dissipates a power of 30µW (2MHz) and 300µW (11MHz). This work is compared with other low-voltage continuous time filters by evaluating the figure-of-merit (FOM) and the results are reported in Table.1.

$$H_{BP(s)} = P_t/(8K\times T\times F_C\times N\times DR)$$

where P_t is the total power consumption, K is Boltzman's constant, T is absolute temperature in degree Kelvin, F_c is the centre frequency, N is the number of poles and DR is the dynamic range of the filter.

From Table.1, it may be noted that the proposed filter results in more than 10-fold reduction.

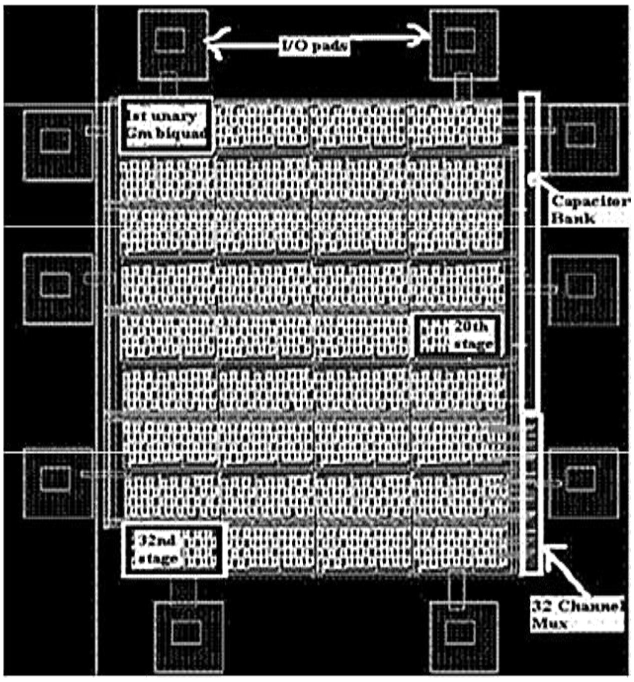

Fig.7. Layout view of Implemented Filter

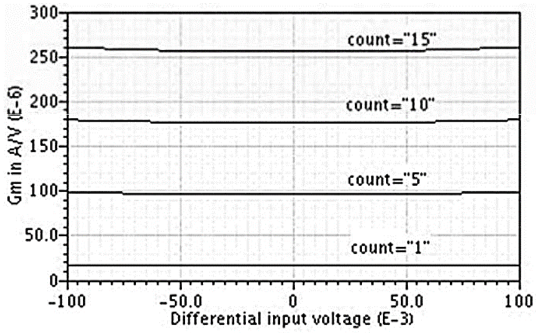

Fig.8. Simulated Transconductance for various Counter Settings

From Table.1, it may be noted that the proposed filter results in more than 10-fold reduction in power and two fold in area respectively than that of [11]. The performance of the programmable band pass filter is summarized in Table.2.

Table.1. Comparison with other filters

Parameters	[11]	[6]	[12]	This work
Technology	0.5µm CMOS	0.35µm CMOS	0.18µm CMOS	0.18µm CMOS
Filter order	12th order	14th order	2nd order	2nd order
Supply voltage	2.7V	2.3V	1.8V	1.8V
IIP3	10dBm @3MHz	28dB @3MHz	NA	28dBVp @3MHz
Total noise	52.3 µVrms	170µVrms	NA	105 µVrms
BW (Programmable)	2MHz to 4MHz	2.4MHz to 3.6 MHz	5.9MHz to 58MHz	2MHz to 11MHz
Active area	0.6mm^2	0.39mm^2	0.5mm^2	0.3mm^2
Power	3.5mW	7.3mW	10.5mW	300µW
Vinpp @ THD=-40dB	NA	NA	200mV	300mV
DR@THD ≤ -40dB	48dB	48dB	49dB	50dB
Figure of Merit (*fJ*)	790	1650	NA	630

Table.2. Performance summary

Parameters	Value
Technology	TSMC 0.18 m CMOS process
Supply voltage	1.8V
Order of the filter	2nd
Frequency tuning	2MHz -11MHz
Q–tuning	0.707 - 50
Pass band gain	7dB
Power consumption	30W to 300W
Total noise	105Vrms

THD @ 300mVpp IIP3 at 3MHz	-41dB 28dBVp (2.9 and 3.1MHz) 36dBVp (4 and 5MHz)
PSRR (1.8V and 0V) at 1MHz	46dB
Load capacitance	1pF

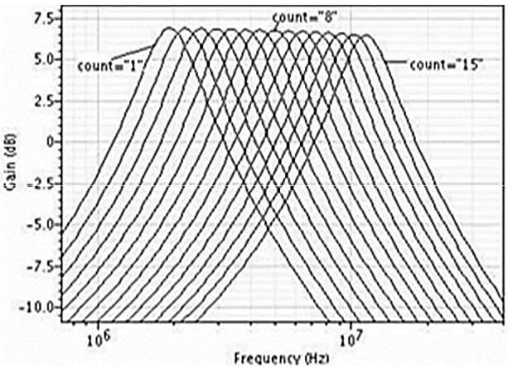

Fig.9. Band pass filter response for various frequency settings (Q=3)

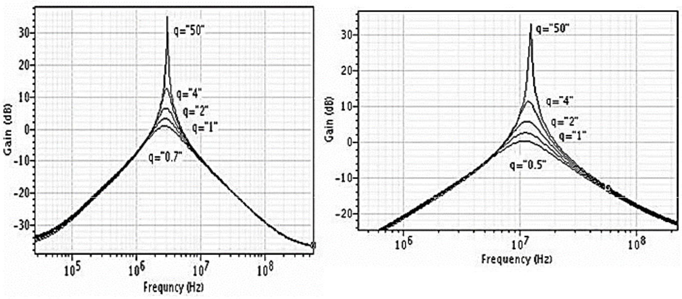

Fig.10. Q-tuning of BPF with centre frequencies of 3.6 and 10.7MHz

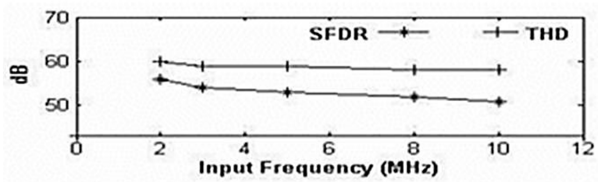

Fig.11. SFDR and THD versus input frequency for V_{in} = 200m V_{pp}

5. CONCLUSIONS

A low power programmable band pass filter targeted for DRM applications is implemented in TSMC 0.18m digital CMOS process using double CMOS pair. Thanks to the sub-threshold Gm stage and compact dummy based switching scheme, this filter performs both in lower power and area than that of the band pass filters proposed for low IF applications reported in the literature. The designed band pass filter features a good center frequency tuning from 2MHz to 11MHz and Q-factor programmable from 1 to 50. It has been shown that the transconductor is well suited for the robust implementation in typical submicron CMOS technologies of advanced low-voltage bandpass filters with center frequency in the lower megahertz region. The filter circuit not only requires lower area and power, but also has a good re-configurability feature and has become a strong candidate for utilizations as one of the building blocks for SDR transceivers.

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