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VERIFICATION AND COMPARISON OF PERFORMANCE PARAMETERS FOR FOLDED CASCODE OPAMP AT DEEP SUB-MICRON LEVELS

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Abstract

This paper presents the design and verification of folded cascode operational amplifier using conventional CMOS technology. The design specification has been decided and accordingly the aspect ratios are designed with the help of design equations. Design have been carried out on Mentor Graphics EDA tool using TSMC 180nm and 130nm, 32nm on HSPICE EDA tool using CMOS technology. Pyxis schematic and ELDO version 11.2 simulation tool is used for designing and Pyxis layout and Calibre tool for verification of the layout. For 180nm technology the pre-layout results are calculated and same are implemented in the EDA tool and gives output values as gain 67.6dB, Phase margin 63º, & Unity Gain Bandwidth 256MHz. The output swings up to 1.7266V with power dissipation of 649.7735µW. The post-layout simulations i.e. physical verification is done and verified using DRC checker, LVS report and PEX results. The performance parameters of folded cascode opamp are compared using 180nm, 130nm, and 32nm CMOS technology where the results show reduction in values but significant fall in power dissipation is observed which is an advantage. Other performance parameters can be improved by using FinFET, CNFET which can be an alternative for CMOS at deep sub-micron levels.

Keywords:

Moore Law, TSMC 180nm, 130nm, 32nm, Mentor Graphics, HSPICE, Physical Verification, DRC, LVS, PEX

1. INTRODUCTION

In this period of elite and small-scale gadgets, CMOS transistor scaling has nearly come to an end. There has been classical work conveyed by analysts for analog front end and back end designs. Still there is challenge for the folded cascode configuration in the present aggressive world. The Operational Amplifier is the most flexible analog device utilized as a part of simple and complex circuit applications [2]. Power scattering is a noteworthy test in the profound submicron innovation and is ending up more imperative in compact applications to enhance battery life traverse. In the meantime, it is likewise a test to keep up with the speed and territory necessities. In this way, it is a test to configuration low power operation amps with huge speed and other execution parameters like high yield swing, stage gain and adequate pick up data transfer capacity item. There are essential three sorts of OTA topologies, established two stage, folded cascode OTAs, and telescopic OTAs [3]. The reason for final selection of folded cascode opamp is power dissipation. Low speed, medium power dissipation of conventional two stage opamp and high speed and power dissipation of telescopic opamp makes the selection criteria imbalanced. So, as high speed and a scope of minimizing power dissipation is more suitable.

The outline of a superior Op-amp is a troublesome undertaking with the tireless scaling in the supply voltage and gadget length. The time and exertion required to plan simple format are generous, despite the fact that they involve a little piece of the format. Simple circuits are helpless against format parasitic and process varieties. The noteworthy elements that guarantee the coveted circuit execution are gadget floor-plan, symmetry and interconnect parasitic [4]. The main drivers of format parasitic are transistor source and deplete capacitances, capacitances in inter-connections, and coupling capacitances between interconnects.

This study is to address various trade-offs related to performance comparison of folded cascode op-amp between pre-layout and post layout simulation. Section 2 describes theory of folded cascode. Small signal analysis of folded cascode along with design specifications and equations are given in section 3. Layout checker tools and flow of work is mentioned in section 4 which ensures perfect match of schematic with the layout. Section 5 presents the simulation results for pre-layout and post layout simulation for conventional gate driven CMOS folded cascode op-amp operating at 1.8V, 1.2V, 1V supply voltage and 180nm, 130nm, 32nm process technology and some concluding remarks appear in section 6.

2. LITERATURE WORK

Gordon Moore, in 1970, anticipated that on account of the constant scaling down, transistor depend on a similar chip would twofold itself in every 18 months [5]. As by reducing the size of the transistor the speed of the device gets increased and the area gets reduced. Such a progression has let transistors to end up smaller and quicker, which in turns devour less power. As CMOS keeps on scaling further into the nanoscale, different gadget non-idealities cause the I-V attributes to be generously not quite the same as very much tempered MOSFETs. Research is now further extended to nanometer region for the search of novel devices such as CNFET which can be used in nanoscale devices.

As described in [6] the design of a folded cascode CMOS Operational Amplifier with a moderate gain, a larger phase margin and low power dissipation, where the circuit is designed using 180 nm technology and its performance parameters are measured using SPICE tool. In [7] is designed RFC OTA using 32nm CMOS technology by reusing the idle transistors in the signal path of FC OTA. Significant increase in performance parameters such as gain, phase margin, and bandwidth are obtained with different process corners and temperature simulations shows the robustness of the OTA design against process and environmental variations. As mentioned in [8] stated the main challenges and limitations of CMOS scaling, not only from physical and technological point of view, but also from material and economical point of view. A push pull configuration [9] is proposed at the initial stage of folded cascode opamp for

enhanced performance of gain and unity gain bandwidth. The results have increment of 3db gain with 100% in unity gain bandwidth over the conventional folded cascode OTA. This advancement in performance parameters is obtained by reducing the in input common mode range by one threshold voltage V_{th}. As in [10] presents a modified folded cascode OTA which is modified from conventional FC OTA by including an extra-large and compensation network. Trade-offs remains in the performance parameters such as gain, bandwidth, slew rate, phase margin and settling time using EDA tool using TSMC 180nm technology.

3. FOLDED CASCODE OP-AMP

Because of contracting in channel length of the transistors in nanometer, it ends up harder to achieve sensible operation amp increases because of different non-perfect impacts and parasitic [11]. Consequently, in simple and blended flag plans, wide swing cascode current mirrors are often utilized. Cradled operation amps are utilized to drive resistive burdens, however numerous contemporary incorporated CMOS operation amps needs to drive just capacitive burdens. Unbuffered operation amps or OTA's are favoured in such current rapid CMOS operation amps which are utilized as a part of low power hardware applications. Consequently, it ends up conceivable to actualize speedier operation amps with better flag swings thought about than those driving resistive burdens.

This can be accomplished by utilizing self-remunerating operation amps driving just capacitive burdens. The rule of this operation amp is to have just a solitary high-impedance hub at the yield of an operation amp. The impedance saw at all other hub is generally low [2]. Because of this, the speed of the operation amp is upgraded. As a consequence, voltage swing increments at the yield hub than voltage motion at all hubs. These kinds of operation amps are common called as folded cascode Op-amp, as appeared in Fig.1. These structures are likewise favoured over adjustable topologies for larger output swing, reasonable gain and stable phase margins.

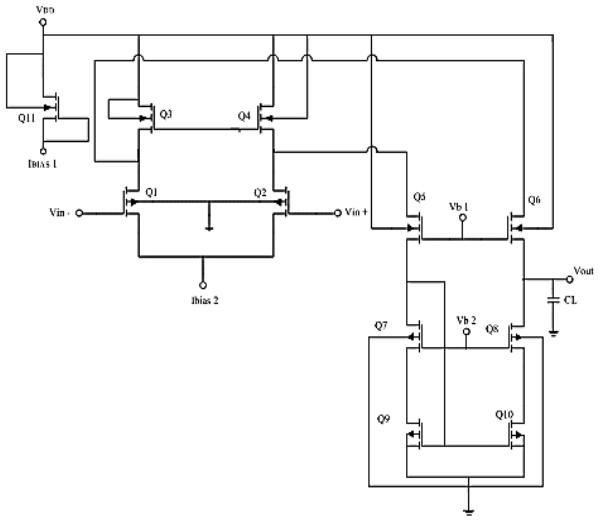


Fig.1. Folded Cascode Op Amp [2]

The circuit, appeared in Fig.1, is a folded cascode operation amp with wide swing cascode current mirrors rather than simple current mirrors [3]. The motivation behind utilizing such mirrors is to build yield impedance, for boosting the dc gain of the operation amp. In folded cascode operation amp, input differential transistors and cascode transistors are of various kinds. Such folded structures are easy to design and helps in getting wider output swing with improve common mode voltage range [8]. This information normal mode scope of the op-amp outlined in this paper is around 1.8V, and yield swing is dependent upon 1.7266V for TSMC 180nm technology. Wide swing current mirror is utilized for differential-to-single finished change and is acknowledged by the transistors M7, M8, M9, and M10. The dominant-pole compensation is achieved by the load capacitor.

4. SMALL SIGNAL ANALYSIS

In this investigation not at all like regular op-amp, it is assumed that the current from M1 straight forwardly moves through the drain of M6 and along these lines to the load capacitance and the current from M2 goes by indirectly through M5 and the present mirror comprising of M7 to M10 [2]. Additionally, it is accepted that most extreme measure of current moves through M1 and henceforth these two ways have slightly different transfer functions. The high frequency poles and zeros are non-predominant and can be disregarded, on the grounds that they are situated at high frequency compared to unity gain frequency. An approximate small-signal transfer function for the folded-cascode op amp is given by:

$$A_V = \frac{V_{OUT}(s)}{V_{IN}(s)} = g_{m1} \cdot Z_L(s) \tag{1}$$

where, g_{m1} is the amplifier's transconductance gain and $Z_L(s)$ is the output impedance.

The open loop gain of op amp is further calculated as:

$$A_V = \frac{g_{m1} \cdot r_{out}}{1 + s \cdot r_{out} C_L} \tag{2}$$

where, r_{out} is the output impedance of the op amp and C_L is the load capacitance.

For high frequencies, the load capacitance dominates, and hence,

$$A_V = \frac{g_{m1}}{sC_L} \tag{3}$$

The gain bandwidth product of the op amp is given as,

$$UGB = \frac{g_{m1}}{sC_L} \tag{4}$$

The input transconductance can be expanded by utilizing long channel transistors and guaranteeing that the input transistor combine's predisposition current is fundamentally bigger than the cascode transistors inclination current. This will likewise bring about change of bandwidth. To amplify the DC gain of the outlined op-amp, it is viewed as that the present moving through every one of the transistors associated with yield hub is at little levels. This won't just augment the input transconductance yet in addition amplifies yield impedance.

Slew rate of the op amp is given by

$$SR = \frac{I_{D4}}{C_L} \quad (5)$$

Power Dissipation in the op amp is given by

$$P_{DD} = V_{DD} \cdot 2(I_{D1} + I_{D6}) \quad (6)$$

5. DESIGN FLOW AND LAYOUT CHECKER TOOLS

In this section the flowchart for the design and verification of op-amp is introduced that is carried out on Mentor Graphics EDA tool. The flowchart is shown in the Fig.2 that starts from design specifications which are selected according to technology.

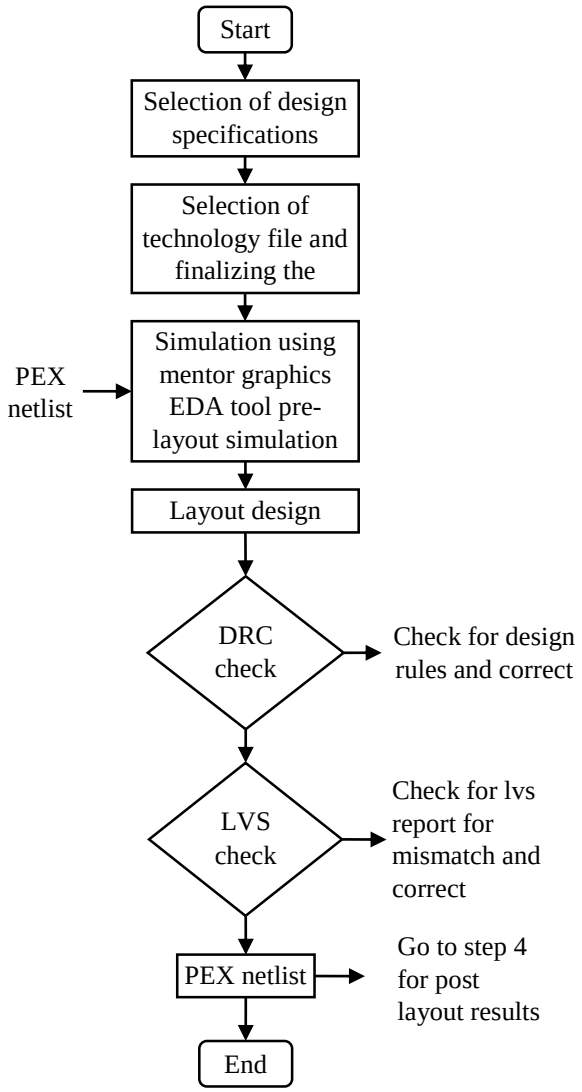


Fig.2. Design flowchart for the proposed work

After specifications are finalized the schematic design simulation is carried out in Pyxis Schematic and ELDO simulation tool using TSMC 180nm technology. Pre-layout results are noted down for comparison with post layout simulation results. The layout is designed for obtaining the post layout results and PCB mask. The port used while designing the op-amp for the simulation have to be deleted for proceeding to layout design. Layout is designed using left-right tiling which facilitates for the engineer for better design. Pyxis Layout for designing the layout and Calibre tool for verification of op-amp. The EDA tool flow carries out the physical verification flow with the common checks steps to verify and post layout simulation results. All the three checks have to be cleared with the last check generating the parasitic file containing R+C combination of parasitics. Any errors in any of the check files generated have to be removed for smooth flow of the tool. This PEX file is used for obtaining the post layout results which on comparison with pre-layout results gives the robust nature of the op-amp.

The following specifications is given for 180nm CMOS technology and is designed in Mentor Graphics EDA tool. Comparison of performance parameters is done for 180nm, 130nm, 32nm CMOS technology have the same specifications but only supply voltage, oxide thickness, mobility and threshold voltage values are different due to the different technology used.

Circuit Specifications:

- Supply Voltage, V_{DD} = 1.8V
- Open loop gain, AV =1000 = 60dB
- Phase Margin = 60°
- Load Capacitance, C_L= 2.5pf
- Maximum Input Common Mode Range, ICMR (+) = 1V
- Minimum Input Common Mode Range, ICMR (-) = 0.8V
- Slew rate = 20V/µsec
- Gain Bandwidth Product, GBW = 256MHz

EDA Tool Specifications for CMOS design:

- $\mu_n C_{ox}$ = 218.58µA/V^2
- Vth_n = 0.37V
- $\mu_p C_{ox}$ = 92.62µA/ V^2
- Vth_p = - 0.39V

Designing has been conceived on the basis of fundamental equations which are used for the calculations of aspect ratios and device dimensions.

6. SIMULATION RESULTS

The folded cascode op-amp shown in Fig.1 is designed in Mentor Graphics EDA tool in Pyxis Schematic and simulated using ELDO simulation tool which are integrated in the EDA tool using BSIM3v3.3 level 53 model at 180nm CMOS technology. The schematic is show in Fig.3 which is designed in the tool.

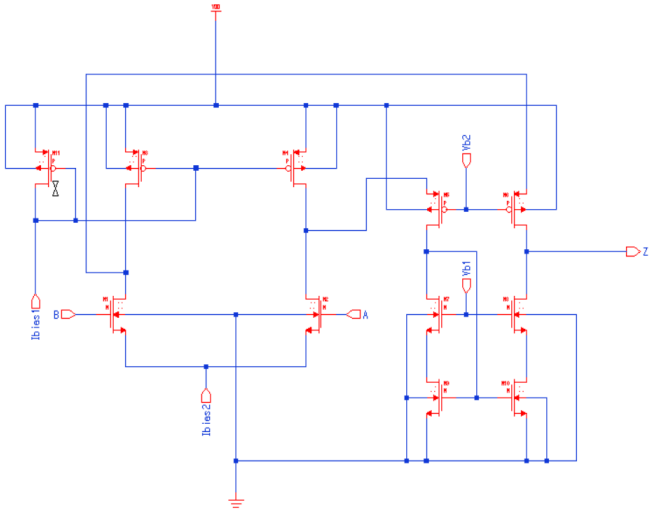
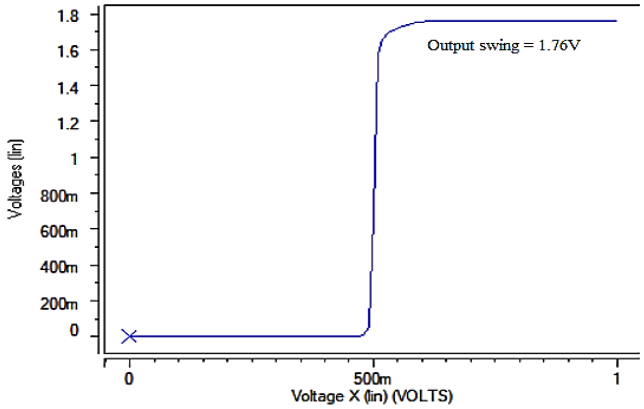
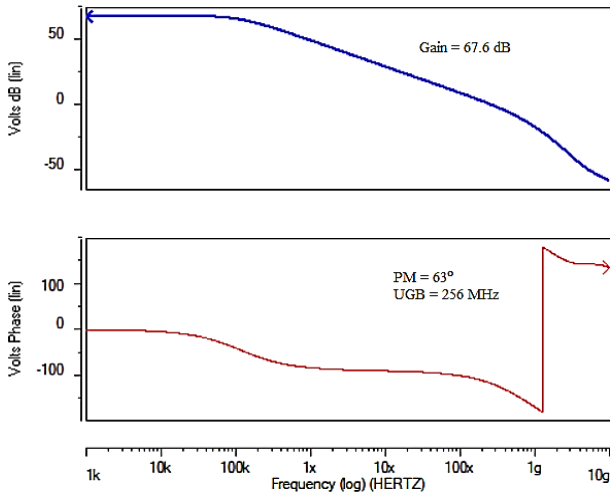


Fig.3. Schematic of folded cascode op-amp

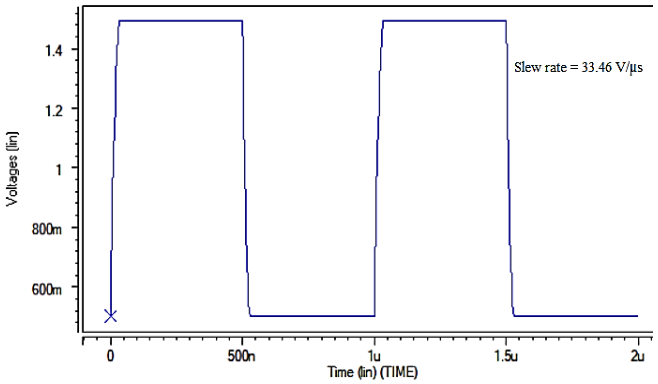
The op-amp operates with the 1.8V power supply and dissipates only µW power. Simulations results for DC, AC and transient analysis are carried out and are shown below in Fig.4.



(a)



(b)



(c)

Fig.4. Output waveforms (a) Output Swing (b) AC (c) Slew rate

The summary of 180nm, 130nm, 32nm CMOS technology is given in Table.1 which depicts the performance parameters values along with power dissipation. The values obtained are approximately equal to the theoretical specification values and the variations for each of the technology is caused due to the different oxide thickness, threshold voltage and other small and large signal values given in the technology files. Low power dissipation is obtained for 32nm CMOS technology which is 11% less than the specification value.

Table.1. Comparison of performance parameters for folded cascode opamp at 180nm, 130nm and 32nm technology

Technology	Gain (dB)	UGB (MHz)	PM (°)	OS (V)	SR (V/µS)	ST (ns)	PD (µW)
FC-CMOS 180	67.6	256	63	1.76	33.46	10.9	649.77
FC-CMOS 130	60.1	224	48	1.07	14.41	9.95	416.17
FC-CMOS 32	30.2	93.5	86.7	0.99	29.48	18.6	356.14

Layout is designed from the schematic in Pyxis layout and physical verification is carried by Calibre tool. The layout shown in Fig.5 is processed for common checks such as DRC (Design Rule Check), LVS (Layout VS Schematic), and PEX (Parasitic Extraction File).

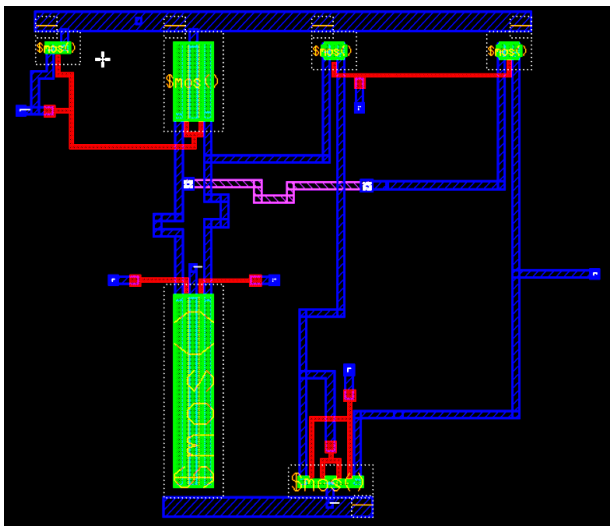


Fig 5. Layout of folded cascode op-amp

6.1 DRC (DESIGN RULE CHECK)

Every explanation has an identical particular system coded in an interior database which relates to the physical check "DRC rule" that relates to this comment. This particular methodology is called at whatever point this explanation is recognized. This methodology acknowledges the data produced in the past advances "content gds layer number, text coordinates and layer coordinates" [1]. A time later it creates the required DRC checker file as drc.summary file. The technology file i.e. (.mod) file is only required for DRC checker tool to carry out the checks.

```
--------------------------------------------------------------------------------
------RULE CHECK RESULTS STATISTICS (BY CELL)
------
--------------------------------------------------------------------------------
------SUMMARY
------
TOTAL CPU Time: 0
TOTAL REAL Time: 0
TOTAL Original Layer Geometries: 255 (282)
TOTAL DRC RuleChecks Executed: 91
TOTAL DRC Results Generated: 0 (0)
```

Fig.6. DRC summary file

6.2 LVS (LAYOUT VS SCHEMATIC)

The second step interfaces the parsed gadget or net to its relating mate in the format. The primary connection between the schematic netlist and the format is the Layout versus Schematic (LVS) that is utilized to play out the LVS correlation. Once the design is LVS-clean, LVS database is produced [1]. This database contains finish data that determines the gadget and net properties on both the schematic and the format databases. Furthermore, data about the availability and the layer properties of each layer on the design is accessible in this database. Technology file, GDSII (Graphic Database System), and schematic netlist that is developed when start the check process. Two files are generated one is. EXT and other is the report file for LVS which gives one to one mapping of all cells between layout and source netlist file.

6.3 PEX (PARASITIC EXTRACTION FILE)

In electronic design automation, parasitic extraction is count of the parasitic impacts in both the composed gadgets and the required wiring interconnects of an electronic circuit, parasitic capacitances, parasitic protections and parasitic inductances, regularly called parasitics. Parasitic extraction is computation of the parasitic impacts in both the composed gadgets and the required wiring interconnects of an electronic circuit, parasitic capacitances, parasitic protections and parasitic inductances, regularly called parasitics [12]. Re-reproduction of schematic with inferring PEX netlist again is performed for post layout simulation results. Technology file, GDSII, simulated netlist, DSPF/R+C selection files are required to carry out simulation.

```
CELL COMPARISON RESULTS (TOP LEVEL)
            ##############
            ##CORRECT###
            ##############

LAYOUT CELL NAME: newDRCsimloriginalnewlayoutsim
SOURCE CELL NAME: NEWMALOCDESION_APP
--------------------------------------------------------------------------------
INITIAL NUMBERS OF OBJECTS
----------------------------------------
                    Layout    Source      Component Type
                    ---------  ---------  ----------------------
Ports:                9          9
Nets:                 14         14
Instances:            6          6          MN (4 pins)
                      5          5          HP  (4 pins)
                    ---------  ---------
Total Inst:           11         11

NUMBERS OP OBJECTS AFTER TRANSFORMATION
--------------------------------------------------------------------
                    Layout    Source      Component Type
                    ---------  ---------  ----------------------
Ports:                9          9
Nets:                 12         12
Instances:            2          2          MN        (4 pins)
                      5          5          HP        (4 pins)
                      2          2          _smn2v (4 pins)
                    ---------  ---------
Total Inst:           9          9
```

Fig.7. LVS summary file

Table.2. Comparison of pre and post layout simulation results

Simulation	Gain (dB)	PM (°)	UGB (MHz)	OS (V)
Pre-Layout	76.31	47.701	271.22	1.7266
Post Layout	57.76	47.704	278.86	1.7265

7. CONCLUSIONS

A folded cascode CMOS operational amplifier is implemented using 180nm, 130nm and 32nm CMOS technology. The results for performance parameters for folded cascode opamp give an indication of reduction of performance of the opamp at deep sub-micron levels which can be improved using new beyond CMOS technology devices such as CNFET, FinFET which replaces CMOS technology which can be an alternative to provide better performance than CMOS technology in nanometer region. Significant phase margin, bandwidth and output swing with acceptable range of gain is provided for pre and post layout simulation results. As compared to pre-layout results the performance parameters such as gain is reduced from 67.6dB to 30.2dB and UGB from 256MHz to 93.5MHz with corresponding 55.33% & 63.48%. With power dissipation being an important factor of design, it is reduced from 649.77μW to 356.14μW with 45.19%. In physical verification results, the parasitics are applied using DSPF (Detailed Parasitic Extracted Format) configuration which causes 14.5% decrease in gain and approximately small reduction in UGB, and output swing. As a part of future scope, the proposed FC OTA can be used for designing analog signal processing applications, RF, Wide band applications etc. CNFET technology will come out to be better alternative for CMOS at

deep sub-micron levels for better performance parameter values for the applications.

REFERENCES

[1] V. Bendre and A.K. Kureshi, "Performance Analysis of Operational Transconductance Amplifier at 180nm Technology", *Proceedings of 2nd International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity*, pp. 271-276, 2016.

[2] Arafa et al., "Schematic-Driven Physical Verification: Fully Automated Solution for Analog IC Design", *Proceedings of IEEE International SOC Conference*, pp. 260-264, 2012.

[3] P.E. Allen and D.R. Holberg, "*CMOS Analog Circuit Design*", Oxford University Press, 2002.

[4] David A. Johns and Ken Martin, "*Analog Integrated Circuit Design*", John Wiley and Sons, 2008.

[5] Nur Hidayah Binti Mansor, "Layout Design of Folded Cascode Operational Amplifier", Technical Report, Department of Electronics Engineering, Universiti Teknikal Malaysia, 2011.

[6] Prasad Guru, "A Low Power, 54dB Open Loop Gain, Folded Cascode CMOS Operational Amplifier using 180nm Technology", Available at: https://www.researchgate.net/publication/317050196_A_Low_Power_54_dB_Open_loop_Gain_Folded_Cascode_CMOS_Operational_Amplifier_using_180_nm_Technology.

[7] T.V. Prasula and D. Meganathan, "Design and Simulation of Low Power, High Gain and High Bandwidth Recycling Folded Cascode OTA", *Proceedings of 4th International Conference on Signal Processing, Communication and Networking*, pp. 1-6, 2017.

[8] Nor Zaidi Haron, "Why is CMOS Scaling Coming to an END?", *Proceedings of 3rd International Design and Test Workshop*, pp. 98-103, 2008.

[9] S. Kumaravel, B. Venkataramani, S. Rishi, V.S. Vijay and B. Shailendra, "An Enhanced Folded Cascode OTA with Push Pull Input Stage", *Proceedings of International Multi-Conference on Systems, Signals and Devices*, pp. 1-6, 2012.

[10] Priyanka Soni, B.P. Singh and Monika Bhardwaj, "Design of Enhanced Performance Folded Cascoded Operational Transconductance Amplifier", *AIP Conference Proceedings*, Vol. 1324, No. 1, pp. 360-364, 2010.

[11] S. Rathore and A.D. Darji, "Minimum Area Layout of High Bandwidth Folded Cascode Operational Amplifier using SCL 180nm CMOS Technology", *Proceedings of International Conference on Information, Communication, Instrumentation and Control*, pp. 1-6, 2017.

[12] Z. Kun and D. Wu Di, "A High-performance Folded Cascode Amplifier", *Proceedings of International Conference on Computer and Automation Engineering*, pp. 41-44, 2011.