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DESIGN OF A CARBON NANOTUBE BASED QUARTERNARY ADDER FOR HIGH SPEED AND LOW POWER APPLICATION

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Abstract

Quarternary logic is the suitable and yet efficient alternate to the binary logic due to its simple design and limited power consumption. The reduction in power consumption is possible because of its narrow circuit overheads. From existing binary circuits, quaternary signals and binary signals are produced through Quaternary(four-valued) logic. The area has been reduced by Quaternary radix on MVL(multi-valued logic). In terms of normalization, short channel effects, impact ionization and surface scattering are among the failures encountered. Resistive-load CNTFET based logic design and a novel Quarternary logic based on CNTFET adder for signal processing application will be designed and compared with existing design. A novel circuit architecture consists of the combination of new device and logic will be proposed. This novel design will be high speed and low power. SPICE simulation is used to verify the proposed design. Comparisons are done with existing design and found an increase in performance of the overall design. In existing work FinFET was done. For implementation Stanford University Nanoelectronics Group CNT model files will be used in Synopsis HSPICE.

Keywords:

Multi-Valued Logic (MVL), Quaternary Logic (QTL), FinFET

1. INTRODUCTION

The VLSI circuit has advanced Integrated Circuits (IC). The VLSI chips have external issues on chip. The MVL circuits are realized by 2 methods namely, 1) Current-mode and 2) Voltage mode. Current-mode circuits, power consumption is high because of poor current flow. Reduction of noise is crucial task. The Quaternary numeral system has base as 4. The Digits 0, 1, 2 and 3 was used for representing any real numbers. In Quaternary numeral system '4' is denoted as maximum number. The Quaternary logic are denoted as {0, 1, 2, 3}. The Cost of input/output (I/O) pins should be taken into account. Every extra bus line has overall system was crucial. FinFETis known as Fin Field Effect Transistor. The FinFET word was derived from set of fins. A multi-gate transistor has wide variety of gates. In FinFET, thin silicon film wrapped around the conducting channel. The Thickness of device depends upon channel length. FinFET device provides better performances than MOSFET technology.

2. LITERATURE SURVEY

Hajare et al. [1] designed FinFET based full adders. MOSFET suffers with short channel effects. The FinFET based 28T and 16T 1-bit full adders was carried out in HSPICE software. The FinFET based full adder design was more effective than MOSFET. A. Raghunandan and D. R. Shilpa [2] innovated High-Speed Hybrid Full Adders using FinFET 18nm Technology. The Hybrid full-adder circuits based on novel full-swing XOR-XNOR gates. This Experiment was carried out using Cadence virtuoso tool with 18nm FinFET technology. The HFA NB 26T achieved a smallest delay.

V.M Senthilkumar and S. Sowmiya [3] used FinFET based 4-2 compressor with FinFET 32nm technology. The Two new approximate 4:2 compressors and full adder were designed using 10 transistors to evaluate 4 bit Dadda multiplier. This Experiment was carried out using HSPICE tool. M. Yang and E. Oruklu et al. [4] applied full adder circuit design using Lateral Gate-All-Around (LGAA) FETs. Full-adder data path circuits using Lateral GAA FETs (LGAA FETs) based on BSIMCMG model are analyzed.

W. X. You et al. [5] evaluated NC-FinFET based subsystem-level logic circuits. The NC-FinFET aspect on performance was discussed. H. Thapliyal et al. (2018) [6] simulated MTJ/CMOS design. This Design are simulated with 45 nm CMOS technology.

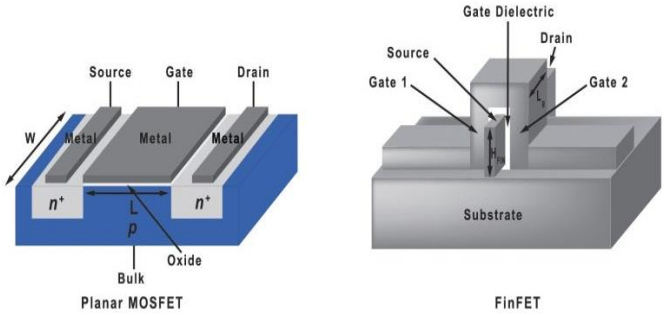

Fig.1. Internal design of FinFET and MOSFET

The MTJ/CMOS OR, AND, XOR, MUX and full adder designs had low power. H. Naseri and S. Timarchi et al. [7] designed XOR/XNOR for low-power and fast full adder. The Experiment carried out using HSPICE and Cadence Virtuoso. The 65-nm CMOS process technology was utilized. Particle swarm optimization algorithm was utilized.

A. Chauhan et al. [8] analyzed low power quaternary adder using CNFET. Multi-valued logic (MVL) such as Quaternary Logic (QTL) was utilized. Carbon Nano-tube Field Effect Transistor (CNFET) was utilized to design QFA. The Experiment was carried out using Cadence Virtuoso.

Roosta et al. [9] designed multiplexer-based quaternary full adder. The Quaternary multiplexer 4:1 was designed with carbon nanotube field-effect transistors (CNFETs) 32-nm technology. The Experiment was carried out using HSPICE simulator.

Takbiri et al. [10] used multiple-valued logic (MVL) at Noise margin (NM) calculations. In MVL NM calculations are used to execute the equations with higher radixes.

A. K. Pandaet al. [11] used 3 operand binary adder. FPGA with 32nm CMOS technology. Dimitrakopoulos et al. [12] discussed Sum Propagate Adders.

3. EXISTING METHODOLOGY

3.1 BINARY ADDERS

Binary Adders is used to add two binary digits. Combinational logic circuit was designed with logic gates. Binary adder is basic combinational logic circuits. It doesn't have any memory unit.

Table.1. Binary to quaternary conversion

Binary	Quaternary
00	0
01	1
10	2
11	3

3.2 CMOS TECHNOLOGY

CMOS (complementary metal-oxide semiconductor) devices are faster and low power. Its complementary with a pair NMOS and PMOS, transistor is turned vice versa. The Main advantages of CMOS are lower power consumption, non-saturating driver, and end to end complementary logic. CMOS in VLSI (very-large-scale integration) design has enabled massive scaling in a variety of semiconductor devices. Combining the CMOS process with VLSI has helped push packages to smaller levels while keeping costs reasonable. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

These advances led to superior performance and dramatically reduced cost per function. Currently, 65 nm CMOS technology is being used in the manufacturing of memory and 3GHz microprocessors. Meanwhile, CMOS devices recently have been fabricated in 65 nm suffer from second order effects. The power optimization was challenging and to optimize the same power supply voltage (Vdd), threshold voltage (Vt), gate oxide thickness (tox), channel length (L) are to be considered.

3.3 FINFET TECHNOLOGY

In recent times, from mobile devices to biomedical applications several microprocessors are designed. These processors should have low power and highly efficient. Compared to BJT and CMOS, FinFET uses fins like structures to control the current flowing through the Gate or channel. The fins formed around the diffusion area is in the Silicon on Insulator (SoI) structure. The device structure is shown in Fig.1. The FinFET performance addressed in literature for designing various circuits are found to be better [12]-[15].

3.4 DISADVANTAGES OF EXISTING METHOD

The Main disadvantage of CMOS logic family is that runs slow speed than BJT. Propagation delay time for CMOS family was 50ns.The CMOS technology below 22nm suffers with short channel effects. Ripple Carry Adder (RCA), Carry Look Ahead (CLA) and Carry Save Adder (CSA) are analyzed in this paper. The Transition of output suffers with propagation delays. So that existing method suffers at computation process. Hence CMOS technology with binary or quaternary logic lags at latency, average power and area requirement (i.e. pin counts).

4. PROPOSED METHODOLOGY

The short-channel behavior and channel doping are improved by using Fin field-effect transistor (FinFET) shown in Fig.2. The FinFET is a multi-gate device which is different from MOSFET (metal-oxide-semiconductor field-effect transistor). Thenovel double gate Silicon on insulator (SOI) like FinFET eliminates short channel and drain induced barrier lowering (DIBL). The Fin is between source and drain, it surrounds gate. The double gate is fabricated on SOI FinFET's top. In triple gate FinFETs, the fins are on sides. When compare with MOSFET's, the dual gate structure in FinFET's produce double the ON current. The feature of FinFET's are the channel control, energy harvesting applications. Using FinFET the Scaling to ultra-low gate dimensions is possible.

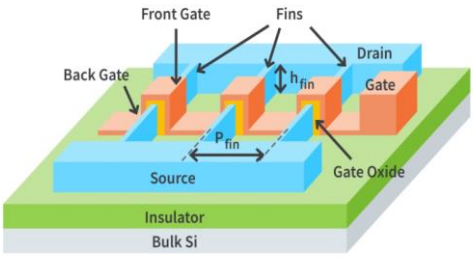

Fig.2. Internal design of FinFET

5. CARBON NANOTUBE FIELD-EFFECT TRANSISTOR

Instead of bulk silicon in the traditional MOSFET structure, A carbon nanotube field-effect transistor (CNTFET) is a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material.

These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional bulk MOSFET structure with a single carbon nanotube or an array of carbon nanotubes.

Fig.3. Top and side view of a silicon back gated CNTFET

The different types of CNTFET devices are top-gated CNTFET, Wrap-around gate CNTFETs, Sheathed CNT and Gate all-around CNT Device (Fig.3). For low biases applied at source/drain, the single-walled carbon nanotubes device can be fully switched off. The metallic tubes are difficult to fully switched off.

5.1 ADVANTAGES OF CNTFET

Carbon nanotubes (CNT) a better conducting material is advantages than the conventional silicon devices.Furthermore, due to their dual characteristics of metallic and semiconducting properties, carbon nanotubes(CNTs) offer the potential to fabricate circuits solely composed of CNTs by utilizing metallic CNTs for interconnect purposes.

5.2 QUATERNARY LOGIC

Using a single wire, 4 logic values can be transmitted in quaternary logic**.** So information is passed using minimum wires (Fig.4). When wires count is minimized, critical path delay, area, total power and energy gets reduced. Compared to binary logic, Quaternary logic has more advantages. For storing any information, it requires half the number of digits. It reduces the storage space when compared with binary system.

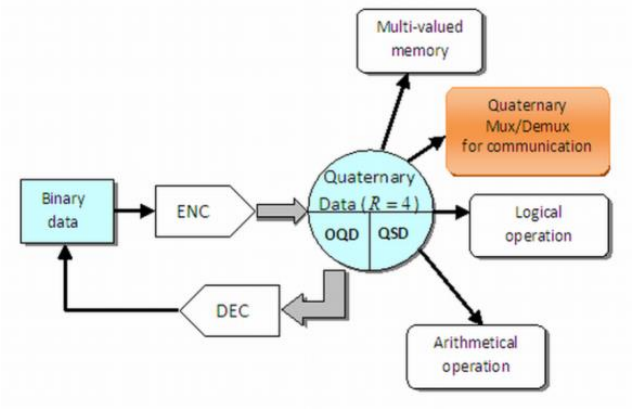

Fig.4. Quaternary logic computation

Quaternary logic is utilized to design Ripple Carry Adder (RCA), Carry Look ahead Adder CLA and Carry Save Adder (CSA) with16nm FinFET Technology. The Average power is measured and compared with other adders. A Quaternary system completely executes its circuits with quaternary logic only. A mixed system is formed using the standard binary system and quaternary logic system. The potential for the logics '0,' '1,' '2,' and '3' and are 0, 1/3 VDD, 2/3 VDD, and VDD respectively. The QNOT, QNAND, and QNOR logics design are implemented using the logic. The QSD number system whose range is -3 to 3 digit can be used to design subtraction without borrow and addition without carry. The complexity, interconnections and transistor counts were reduced in QSD number system. This Logic can be used for implementing multipliers and adder with effective area and speed. The Quaternary system base is about 4. Digits 0, 1, 2 and 3 are utilized for representing number for a system. The QSD number system minimizes the interconnections and transistor counts. Hence the complexity of system gets minimizes. Hence this logic was utilized in adder for an effective area and speed. The Main quaternary logic functions are QNOT, QNAND, and QNOR. The Conversion binary logic and quaternary logic are discussed detailed in the introduction section. The Main quaternary logic functions are QNOT, QNAND, and QNOR was designed. The Adders such as QCLA, QRCA, and CSA was designed and their performance was analyzed. The proposal of FinFET aimed to address the issues associated with short channel effects.

6. RESULTS AND DISCUSSION

The computational building blocks are the Logic circuits such as Inverter, NAND, XOR were designed using quaternary logic and simulated. The adders such as half adder and full adder are designed using quaternary logic and simulated. LTspice IV is used here for the simulation of all logic circuits. The netlist were designed and executed for CNTFET devices. The CMOS counterpart of the Quaternary Inverter Transistor Level Implementation. In LTspice are shown in Fig.below. The CNTFET results are obtained using model file. Using SPICE netlist conversion the nodes and circuit components are replaced with short gated FinFET and CNTFET model. The model parameters are given below table.2

Table.2. PTM Technology parameters for CNTFET

Parameter	Description	Value
Lch	Physical channel length	32.0 nm
Tox	The thickness of high-k top gate dielectric material	4.0 nm
L_channel	Physical gate length	32.0 nm
Pitch	The distance between the centers of two adjacent CNTs	20.0 nm
Leff	The mean free path inp+/n+ doped CNT	15.0 nm
phi_M	The work function of Source/Drain metal contact	4.6eV
phi_S	CNT work function	4.5eV

The proposed CNTFET based circuits provides enhanced performance in terms of current, power and energy. The performance exhibits variations across different frequencies are presented. The CNTFET has shown improved power consumption at high input GHz range. When compared to CMOS the CNTFET will be better in all aspects. At higher frequencies the circuit has increased current and power in the order of 10. But compared to CMOS and FinFET the power consumed was very less at higher frequencies.

Table.3. Implementation of the proposed CNTFET based Full adder in different frequency of operation

Parameters	10 MHz	100 MHz	1 GHz
Average Current (A)	18.54µ	12.3538µ	13.092µ
Average Power (W)	5.6828p	54.182p	14.4132n
Average Energy (J)	0.36468f	5.5036f	5.6548a
Delay (s)	115.98p	0.99512p	20.044p
PDP	63.614y	269.588y	1444.4y

10^{-12}, *pico*, p. 10^{-15}, femto, f. 10^{-18}, atto, a. 10^{-21}, zepto, z. 10^{-24}, yocto, y

The building block of the quaternary adder -the inverter is shown in Fig.5. The circuit is of three stages with 3 PMOS and 3

NMOS for better driving capability. The stage provides the same logic but with better current. The voltage applied for logic 1 is 1V.

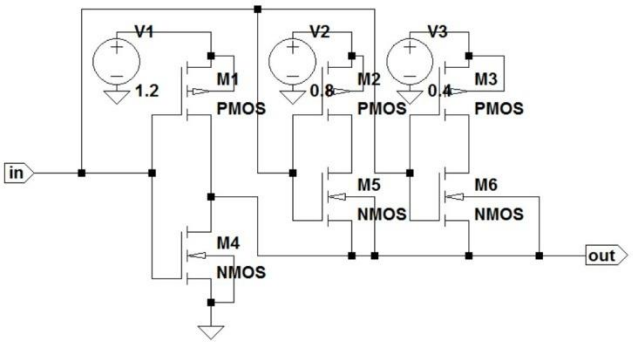

Fig.5. Building block of the quaternary adder

6.1 QUATERNARY NAND TRANSISTOR LEVEL IMPLEMENTATION IN LTSPICE

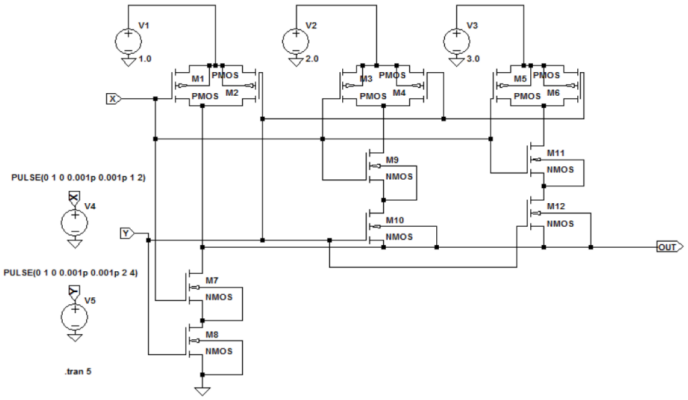

Fig.6. Building block of the quaternary adder -the quaternary NAND

The building block of the quaternary adder -the quaternary NAND is shown in Fig.6 above. The circuit is of three stages with 3 PMOS and 6 NMOS for better driving capability. The stage provides the same logic but with better current. The building block of the quaternary adder -the NAND is shown in Fig.6. The voltage applied for logic 1 is 1V, and zero for logic zero.

6.2 QUATERNARY XOR TRANSISTOR LEVEL IMPLEMENTATION IN LTSPICE

The building block of the quaternary adder -the quaternary XOR is shown in Fig.7 above. The circuit is of three stages implemented using 6 NAND gates. The complete circuit is implemented and executed. The stage provides the same logic but with better current. The Fig.7 shows the circuit of quaternary half adder using NAND gates. The complete circuit is implemented and executed. The sum and carry is obtained as per the quaternary logic. The inputs x and y with sum and carry are shown. The voltage levels are nearer to 1V for logic 1 and few mV for logic zero.

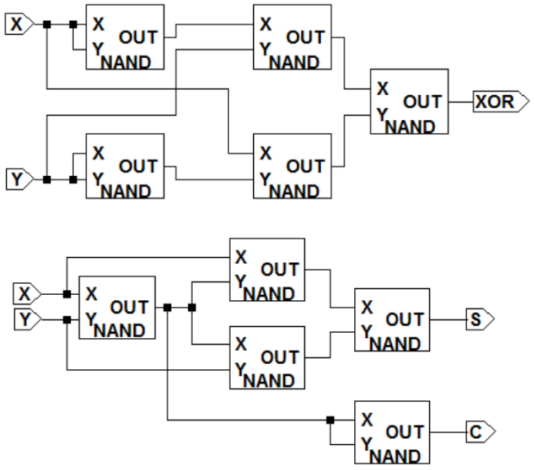

Fig.7. Proposed Quaternary XOR Transistor and half adder circuit

The Quaternary Full Adder Transistor Level Implementation In LTspice is shown below. The simulations are carried out using model files and netlist. The circuits are executed.

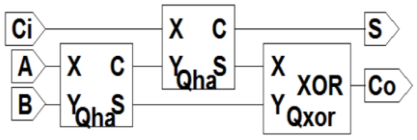

Fig.8. Quaternary full adder

The Fig.8 shows the circuit of quaternary full adder using quaternary full adder and quaternary XOR gates. The complete circuit is implemented and executed. The sum and carry are obtained as per the quaternary logic . The voltage levels are nearer to 1V for logic 1 and few mV for logic zero.

7. CONCLUSION

This paper proposes a quaternary adder with FinFET and CNTFET Technology. The Quaternary RCA, Quaternary CLA and Quaternary CSA performance were analyzed. The Average power is measured and compared with existing adders. The Proposed paper provides effective results power consumption. Multiplication process reduced due to a low power consumption and rapid computation. In terms of power, delay and area consumption the proposed quaternary adder with CNTFET technology is more efficient when compared with other adders.

In future, Application specific integrated circuits will be designed based on the logic and adder designed using CNTFET. The ASIC for medical wearable device will be designed using the adder and multiplier of quaternary logic which will enhance the computing performance. The power minimization will be further improved using gating methods. Input signal and power gating will reduce the battery power in wearable devices.

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