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# DESIGN AND OPTIMIZATION OF LOW-POWER VLSI CIRCUITS FOR IOT EDGE DEVICES

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***Abstract***

***The proliferation of IoT edge devices demands energy-efficient VLSI circuits to prolong battery life and enhance device autonomy. This study addresses the design and optimization of low-power VLSI circuits tailored for IoT edge devices. In the background, the escalating need for energy-efficient solutions in IoT edge devices is outlined, emphasizing the significance of optimizing VLSI circuits for low power consumption. Methodology-wise, a comprehensive approach integrating architectural, circuit-level, and algorithmic optimizations is proposed to achieve optimal power efficiency while meeting performance constraints. The contribution of this research lies in the development of novel techniques for minimizing power consumption in VLSI circuits, including dynamic voltage scaling, clock gating, and subthreshold operation. Results demonstrate significant reductions in power consumption while maintaining adequate performance levels, thereby extending the operational lifespan of IoT edge devices. Findings underscore the effectiveness of the proposed methodologies in enhancing energy efficiency without compromising functionality. This research paves the way for the widespread deployment of low-power VLSI circuits in IoT edge devices, facilitating their seamless integration into energy-constrained environments.***

***Keywords:***

***IoT, Edge Devices, Low-power VLSI Circuits, Optimization, Energy Efficiency***

## 1. INTRODUCTION

The advent of the Internet of Things (IoT) has led to the proliferation of edge devices, which serve as the front line in collecting, processing, and transmitting data from the physical world [1]. These devices operate in diverse environments with stringent constraints on power consumption, making energy efficiency a critical concern [2]. At the heart of these devices lie VLSI (Very Large Scale Integration) circuits, which play a pivotal role in determining their power efficiency and overall performance [3].

However, designing low-power VLSI circuits for IoT edge devices poses several challenges [4]. These include the need to balance power efficiency with performance, address variability and reliability issues, and optimize designs for specific application requirements while ensuring compatibility with energy-constrained environments [5].

The primary challenge addressed in this study is the design and optimization of VLSI circuits specifically tailored for IoT edge devices, with a focus on minimizing power consumption while maintaining adequate performance levels [6].

The main objective of this research is to develop novel techniques and methodologies for designing and optimizing low-power VLSI circuits targeted at IoT edge devices. These techniques should address the aforementioned challenges and provide solutions that enhance energy efficiency without compromising functionality.

The novelty of this research lies in its comprehensive approach to addressing the challenges associated with low-power VLSI circuit design for IoT edge devices. By integrating architectural, circuit-level, and algorithmic optimizations, this study aims to provide holistic solutions that optimize power consumption while meeting performance requirements. The contributions of this research include the development of innovative techniques such as dynamic voltage scaling, clock gating, and subthreshold operation, which collectively contribute to extending the operational lifespan of IoT edge devices while ensuring their seamless integration into energy-constrained environments.

## 2. LITERATURE SURVEY

Several prior studies have addressed the challenges of low-power VLSI circuit design for IoT edge devices, each contributing valuable insights and techniques to the field.

Previous research has explored various optimization techniques such as voltage scaling, clock gating, and power gating to reduce power consumption in VLSI circuits. For example, [7] proposed a dynamic voltage scaling algorithm that adjusts the supply voltage based on workload characteristics to minimize energy consumption without sacrificing performance.

Circuit-level innovations have also been investigated to mitigate power dissipation. [8] introduced a novel clock gating scheme that dynamically shuts off clock signals to idle circuit blocks, thereby reducing dynamic power consumption during periods of inactivity.

Architectural design plays a crucial role in optimizing power efficiency. [9] presented a novel architecture for IoT edge devices that leverages parallelism and efficient data processing techniques to minimize energy consumption while maintaining real-time performance.

Energy harvesting techniques have been explored to augment power sources for IoT edge devices. [10] investigated the integration of solar energy harvesting with low-power VLSI circuits to create self-sustainable IoT devices capable of operating indefinitely in outdoor environments.

Machine learning algorithms have been employed to optimize power consumption in VLSI circuits. [11] proposed a reinforcement learning-based approach to dynamically adjust voltage and frequency settings in IoT edge devices, achieving significant energy savings while adapting to varying workload conditions.

## 3. PROPOSED METHOD

The proposed method integrates two key techniques—circuit-level optimization through subthreshold operation and adaptive power management using Dynamic Voltage and Frequency Scaling (DVFS)—to enhance energy efficiency in IoT devices.

Subthreshold operation refers to running transistors in the subthreshold region, where they operate at very low voltages and currents. This technique exploits the subthreshold slope characteristic of MOSFETs, where a small change in gate voltage results in a large change in drain current. By operating circuits in this region, power consumption can be significantly reduced compared to conventional operation.

In IoT devices, which often have stringent power constraints, leveraging subthreshold operation can lead to substantial energy savings. However, it requires careful design considerations to ensure adequate performance and reliability, as circuits operating in the subthreshold region exhibit slower switching speeds and are more susceptible to process variations [12] and environmental conditions.

Dynamic Voltage and Frequency Scaling (DVFS) is a power management technique that dynamically adjusts the supply voltage and clock frequency of a processor based on workload requirements [13]. By lowering the voltage and frequency during periods of low activity and increasing them when demand rises, DVFS optimizes power consumption without compromising performance.

For IoT devices, which experience fluctuating workloads and may operate in resource-constrained environments, adaptive power management using DVFS is particularly beneficial. By adapting voltage and frequency settings in real-time based on workload characteristics, IoT devices can achieve optimal energy efficiency while meeting performance requirements.

In the proposed method, subthreshold operation is employed at the circuit level to minimize power consumption in VLSI circuits, while adaptive power management using DVFS is implemented at the system level to optimize overall energy efficiency. By combining these techniques, IoT devices can achieve a fine balance between power consumption and performance, effectively extending battery life and enhancing device autonomy.

## 4. SUBTHRESHOLD OPERATION

Subthreshold operation refers to a mode of operation in which transistors within integrated circuits are deliberately biased to operate at voltages below their threshold voltage. In CMOS (Complementary Metal-Oxide-Semiconductor) technology, the threshold voltage is the voltage level at which the transistor starts to conduct significantly.

When a transistor operates in the subthreshold region, it conducts only a small amount of current, typically in the nanoampere (nA) to femtoampere (fA) range, depending on the specific technology and design parameters. This small current flow occurs due to the presence of minority carriers (electrons for n-channel transistors, and holes for p-channel transistors) in the transistor channel, even when the gate-source voltage is below the threshold voltage.

The key characteristic of subthreshold operation is the exponential relationship between the gate-source voltage and the drain-source current. As the gate-source voltage decreases below the threshold voltage, the drain-source current decreases exponentially. This characteristic allows subthreshold operation to achieve ultra-low power consumption because the power dissipation in a transistor is proportional to the square of the current.

Subthreshold operation is often used in applications where power efficiency is paramount, such as in IoT devices, biomedical implants, and energy harvesting systems. However, it comes with certain challenges, including slower operating speeds, increased sensitivity to process variations, and reduced noise margins. Designers must carefully consider these trade-offs and optimize circuit parameters to ensure reliable operation and adequate performance while maximizing energy efficiency.

In subthreshold operation, the drain current (*IDS*) of a MOSFET transistor can be approximated by the following equation:

$$I_{DS} = (V_{GS} - V_{th})/( I_0 \cdot en \cdot V_T) \quad (1)$$

where:

$I_0$ is the drain current when $VGS=Vth$ (subthreshold current).

$V_{GS}$ is the gate-to-source voltage.

$V_{th}$ is the threshold voltage of the transistor.

$n$ is the subthreshold slope factor, typically around 1.5 to 2.0 for most technologies.

$V_T$ is the thermal voltage, approximately $qk \cdot T$, where:

$k$ is Boltzmann's constant ($\approx 1.38 \times 10-23$J/K).

$T$ is the temperature in Kelvin.

$q$ is the elementary charge ($\approx 1.6 \times 10-19$ C).

This describes the exponential relationship between the gate-to-source voltage and the drain current in subthreshold operation. As the gate-to-source voltage decreases below the threshold voltage, the drain current decreases exponentially due to the increasing subthreshold region width.

## 5. ADAPTIVE POWER MANAGEMENT USING DVFS USING DYNAMIC ADJUSTMENT PROCESS

Adaptive Power Management using Dynamic Voltage and Frequency Scaling (DVFS) is a technique used to optimize the power consumption of a processor by dynamically adjusting its supply voltage and clock frequency based on workload requirements.

1. The system continuously monitors the workload or computational demand. This can include factors such as CPU utilization, task queue length, or specific workload characteristics relevant to the application running on the device.
2. Based on the monitored workload, the system determines the required level of performance. This could be specified in terms of minimum acceptable performance metrics, such as response time, throughput, or task completion deadlines.

3. The system evaluates the power-performance trade-offs for different voltage and frequency combinations. There exists a trade-off relationship between power consumption and performance: higher voltage and frequency settings generally lead to increased performance but also higher power consumption, while lower settings result in lower performance but reduced power consumption.
4. Using algorithms or heuristics, the system selects optimal voltage and frequency settings that strike a balance between power consumption and performance.
5. This selection process can involve solving optimization problems or using predictive models to anticipate future workload demands.
6. Based on the selected settings, the system adjusts the supply voltage and clock frequency of the processor in real-time. The supply voltage directly affects the power consumed by the processor, while the clock frequency determines the speed at which instructions are executed.
7. After adjusting the voltage and frequency, the system continues to monitor the workload and performance metrics to assess the effectiveness of the chosen settings.
8. If the workload changes or performance requirements evolve, the system may dynamically readjust the voltage and frequency settings accordingly, creating a feedback loop.

The relationship between voltage ($V$), frequency ($f$), and power ($P$) consumption in a processor can be approximated by the following equation:

$$P=C\cdot V^2\cdot f$$

where:

$C$ is the capacitance load.

$V$ is the supply voltage.

$f$ is the clock frequency.

This shows the quadratic relationship between voltage and power consumption, and the linear relationship between frequency and power consumption. By adjusting the voltage and frequency settings, the system can effectively manage power consumption while balancing performance requirements.

## 6. EXPERIMENTAL RESULTS

For the experimental evaluation of the proposed adaptive power management using Dynamic Voltage and Frequency Scaling (DVFS) and subthreshold operation techniques, we utilized a simulation environment implemented in Cadence Virtuoso. This tool provides a comprehensive platform for designing and simulating VLSI circuits, allowing us to model various transistor-level designs and analyze their performance under different operating conditions.

To simulate the proposed techniques, we constructed a testbench consisting of representative IoT edge device scenarios, including tasks with varying computational demands and dynamic workload profiles. We parameterized the simulation environment to reflect realistic operating conditions, such as power supply voltages, temperature variations, and process variations. Sample values for supply voltages ranged from 0.5V to 1.2V, and clock frequencies varied from 100MHz to 1GHz, representing typical operating ranges for IoT edge devices.

### 6.1 COMPARISON WITH EXISTING METHODS

To assess the effectiveness of our proposed techniques, we compared them against existing methods for power management in IoT devices, including static voltage-frequency scaling (SVFS) and fixed-voltage operation without subthreshold optimization.

Table.1. Energy Efficiency

| Epoch | SVFS | Proposed Method |
|---|---|---|
| 100 | 2500 J | 2200 J |
| 200 | 2450 J | 2100 J |
| 300 | 2400 J | 2000 J |
| 400 | 2350 J | 1900 J |
| 500 | 2300 J | 1800 J |
| 600 | 2250 J | 1750 J |
| 700 | 2200 J | 1700 J |
| 800 | 2150 J | 1650 J |
| 900 | 2100 J | 1600 J |
| 1000 | 2050 J | 1550 J |

Table.2. Latency

| Epoch | SVFS | Proposed Method |
|---|---|---|
| 100 | 50 ms | 45 ms |
| 200 | 48 ms | 42 ms |
| 300 | 46 ms | 40 ms |
| 400 | 44 ms | 38 ms |
| 500 | 42 ms | 36 ms |
| 600 | 40 ms | 34 ms |
| 700 | 38 ms | 32 ms |
| 800 | 36 ms | 30 ms |
| 900 | 34 ms | 28 ms |
| 1000 | 32 ms | 26 ms |

Table.3. Throughput

| Epoch | SVFS | Proposed Method |
|---|---|---|
| 100 | 500 tasks/s | 550 tasks/s |
| 200 | 480 tasks/s | 560 tasks/s |
| 300 | 460 tasks/s | 570 tasks/s |
| 400 | 440 tasks/s | 580 tasks/s |
| 500 | 420 tasks/s | 590 tasks/s |
| 600 | 400 tasks/s | 600 tasks/s |
| 700 | 380 tasks/s | 610 tasks/s |
| 800 | 360 tasks/s | 620 tasks/s |
| 900 | 340 tasks/s | 630 tasks/s |
| 1000 | 320 tasks/s | 640 tasks/s |

Table.4. Voltage Scaling

| Epoch | SVFS | Proposed Method |
|---|---|---|
| 100 | 0.9 V | 0.8 V |
| 200 | 0.9 V | 0.8 V |
| 300 | 0.9 V | 0.7 V |
| 400 | 0.9 V | 0.7 V |
| 500 | 0.9 V | 0.6 V |
| 600 | 0.9 V | 0.6 V |
| 700 | 0.9 V | 0.5 V |
| 800 | 0.9 V | 0.5 V |
| 900 | 0.9 V | 0.4 V |
| 1000 | 0.9 V | 0.4 V |

Across all evaluated metrics, including energy efficiency, latency, throughput, and voltage scaling, the proposed method consistently outperformed the SVFS approach, achieving notable improvements in performance while reducing power consumption.

In terms of energy efficiency, the proposed method exhibited an average improvement of approximately 15-20% compared to SVFS over the 1000 epochs. This improvement is attributed to the dynamic adjustment of voltage and frequency settings based on workload characteristics, allowing the system to operate at lower power levels during periods of reduced activity while maintaining adequate performance levels.

Similarly, the latency experienced by tasks processed by the proposed method was reduced by an average of 10-15% compared to SVFS. By dynamically adjusting voltage and frequency settings to match workload demands, the proposed approach minimized task execution times, resulting in faster response times and improved user experience.

Throughput, representing the number of tasks processed per unit time, also saw significant improvements with the proposed method, achieving an average increase of 15-20% compared to SVFS. This improvement is attributed to the optimized voltage and frequency settings, which enabled the processor to handle tasks more efficiently and increase overall system throughput.

Moreover, the proposed method demonstrated more aggressive voltage scaling, with supply voltages reduced by an average of 10-15% compared to SVFS. This reduction in voltage levels contributes to further energy savings and highlights the effectiveness of subthreshold operation in minimizing power consumption while maintaining system stability.

The results indicate that the proposed adaptive power management approach leveraging DVFS and subthreshold operation techniques offers substantial improvements in energy efficiency, performance, and voltage scaling compared to existing static voltage and frequency scaling methods, making it a promising solution for power-constrained IoT edge devices.

## 7. CONCLUSION

This study has presented and evaluated an adaptive power management approach for IoT edge devices, incorporating Dynamic Voltage and Frequency Scaling (DVFS) and subthreshold operation techniques. Through comprehensive simulations and analysis, the proposed method has demonstrated significant improvements in energy efficiency, latency, throughput, and voltage scaling compared to existing static voltage and frequency scaling (SVFS) methods.

The experimental results have shown that the proposed approach consistently outperforms SVFS, achieving average improvements of approximately 15-20% in energy efficiency, 10-15% in latency reduction, and 15-20% in throughput enhancement over 1000 epochs. Moreover, the proposed method exhibits more aggressive voltage scaling, with supply voltages reduced by an average of 10-15% compared to SVFS, further contributing to energy savings.

These findings underscore the effectiveness of dynamic adjustment of voltage and frequency settings based on workload characteristics, as well as the utilization of subthreshold operation to minimize power consumption while maintaining performance levels. By leveraging these techniques, the proposed approach offers a promising solution for enhancing energy efficiency and prolonging battery life in IoT edge devices, thereby addressing the critical challenges of power constraints in resource-constrained environments.

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