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CMOS REALIZATION OF CFOA BASED ON CLASS AB SUBTHRESHOLD CURRENT MIRROR OTA AND APPLICATIONS

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Abstract

This paper presents a low-voltage low-power current feedback operational amplifier using bulk driven class AB subthreshold current mirror OTA followed by second generation CCII+ cell having wide input common mode range and an output buffer. The CCII+ cell uses two conventional CMOS inverters connected at the output of the OTA. This OTA circuit permits closely rail-to-rail input common mode range, high output current drive capability with low dual power supply of ± 0.25 V. This CFOA cell produces low input referred noise of 0.8 µV/sqrt Hz, dissipates ultra-low power of 485.3 nW and is suitable of low-frequency applications, such as bio-signal processing. This CFOA cells are utilized to design a SIMO type voltage mode biquadratic filter and current mode instrumentation amplifier to validate its workability. The circuit is simulated using tanner EDA tool in 180 nm n-tub CMOS process technology with low bias current of 20 nA.

Keywords:

Current Feedback Operational Amplifier (CFOA), Bulk-Driven (BD), Second Generation Current Conveyor (CCII), SIMO Biquadratic Filter, Instrumentation Amplifier (IA)

1. INTRODUCTION

In the recent years, there has been great interest for the analog circuit designer to design portable analog circuits operating successfully with low-voltage and low-power (LV-LP) budget. So, the research devoted for such type of analog circuits like CCII and CFOA which have their own advantages due to better performances, high speed and better bandwidth than voltage-mode operational amplifier (op-amp) and operational transconductance amplifier (OTA) counterparts. The CFOA cell provides constant bandwidth irrespective of its closed loop gain as long as its feedback resistance remains constant and is much greater than its inverting input resistance [1]. The slew rates of CFOA is very high as compared to op-amp and OTA cells [2].

Basically, the bipolar junction transistor (BJT) based CFOA cell was more popular because of its high current driving capability and high transconductance gain which favoured current mode design. The circuit implementation with CMOS devices offers benefits of offset compensation, compact area design and high frequency operations.

Indeed, the CFOA circuit implemented by using CMOS operates with low-power budget and minimum supply voltage (V_{TH}+3$V_{DS,Sat}$) where V_{TH} is device threshold voltage and $V_{DS,Sat}$ is its saturation voltage [3], [4]. The integrated circuit implementation of CFOA is commercially available in the form of AD844 which provides an accessible compensation terminal. It is an important analog building block for analog circuit design because various functional units can be designed with least possible number of components and without requiring any component matching conditions [5].

Nowadays, current mode circuits are more popular when compared to voltage mode circuits. The voltage-mode cell such as the op-amp has limited slew rate and gain-bandwidth. The second-generation positive and negative current conveyer (CCII) has also been used for many analog systems designs in both voltage and current-mode aspects. The CFOA cell relatively offers maximum bandwidth and slew rate [6]-[7]. Hence, the CCII+ and CFOA are mostly used for LV-LP design with enhanced slew rate with constant gain independent of its bandwidth. The CCII+ and CFOA cells operate well at low-supply voltage and reduced power dissipation and are suitable design cells for both voltage and current-mode design approaches [8].

The analog mixed-signal circuits and systems utilizes some of the active cells like op-amp, OTA, CCII, and CFOA cells. Among these active cells, the CFOA came into picture in 1985 which offers a constant bandwidth of 100 MHz which is independent of closed-loop gain and a very high slew rate of 2 kV/µs and suitable for high frequency applications [9].

The CCII+ cell followed by output buffer are most common topology to realize the CFOA cell available in literature. A lot of applications such as voltage and current amplifiers, integrators, differentiators, multipliers, impedance simulators, analog to digital and digital to analog converters, instrumentation amplifiers, oscillators, biquadratic filters etc. are realized by CFOA cells in past literature. In last decade, several circuits have been implemented using CFOA cell. Analysis of the noise characteristics of current-feedback operational amplifier has been presented in [10], in this research article authors have implemented CFOA cell using BJT based design topology and analyse the circuit to calculate voltage and current noise power spectral densities as 2.8 nV/sqrt Hz, 1.7 pA/sqrt Hz determined at 1 MHz frequency. A research paper titled, "A New Configuration for Current Feedback Operational Amplifiers," has been presented in [11], in this article the authors have implemented an inverting amplifier/attenuator using CCII+ cell followed by op-amp with three resistors and one capacitor. The authors reported that in the non-inverting mode, the circuit produced the DC attenuation of −6.3 dB and unity gain of 0 dB. A research paper, titled, "Alternative Realizations of CMOS Current Feedback Amplifiers for Low Voltage Applications," in [12] has implemented a CMOS CFA (Current feedback amplifiers) by using CCII+ cell followed by output voltage buffer for Circuit-1 and obtained their performances in terms of input resistance, $r_{in,x}$ at low frequency as 15.11 Ω, r_z as 47.9 kΩ, output resistance of CFA R_0 < 0.2 Ω and power consumption of 2.2 mW at 1.8 V and 45 mW at 3.3 V, respectively. High-performance CMOS Current Feedback Operational Amplifier is addressed in [2] has implemented high performance CFOA cell which produced the loop gain of 74 dB, gain-bandwidth product (GBW) of 58 MHz, high slew-rate of 300 V/µs, the input noise voltage spectral

density of 10.9 nV/sqrt Hz and power dissipation of 5.36 mW. The paper titled, "Low-Voltage High-Drive CMOS Current Feedback Op-Amp," in [4] has implemented the low voltage CFOA cell using two CCII+ cell by cascading and obtained high current drive capability of ± 1mA using a power supply of 1.5 V. The DC gain and the GBW were found 53 dB and 390 kHz, respectively. The phase margin was 57° and almost independent of the load capacitor. The r_x, r_z and slew-rate have been reported as 150 Ω, 300 kΩ and 1 V/μs, respectively for single CCII+ cell. The paper titled, "Two CMOS Current Feedback Operational Amplifiers, in [13] has reported the performances of the CFOA cell as slew-rate of 35 V/μs, settling time of 60 ns, closed loop bandwidth of 2 MHz and current dissipation of 1.63 mA using a supply voltage of 3.3 V. The research paper titled, "A new 90 nm CMOS current feedback operational amplifier," in [14] has reported the performances of low bandwidth (LBW) and high bandwidth (HBW) of 32 MHz and 107 MHz using 1.2 V power supply. The output impedance is as low as 8 Ω, for HBW circuit, and increases to 110 Ω at 120 MHz for LBW circuit. Its output impedance starts with 20 Ω and reaches 300 Ω at 33 MHz. The paper titled, "Multiphase Sinusoidal Oscillators Using Current Feedback Operational Amplifiers," in [15] has implemented three phase sinusoidal oscillators using 3-CFOA cells, 3-RC networks and 3-resistors and six phase sinusoidal oscillator using 6-CFOA cells, 6-RC networks and 6-resistors and found frequency of oscillation of 106 kHz. The research article titled, "Multiple Input Single Output Universal Biquad Filter with Current Feedback Operational Amplifiers," in [16] has implemented MISO (Multiple input single output) type biquadratic filter using 4-CFOA cells, 5-resistors and two capacitors. The authors have addressed the resonance frequency, ω_0 and quality factor, Q of 94.5 kHz and 1.1, respectively. A Novel Equi-amplitude Quadrature Oscillator Based on CFOA in [17] has presented quadrature oscillator using 3-CFOA cells, 4-resistors and two capacitors which offered the oscillation frequency of 15.6 kHz with dual power supply of ± 12 V. The research paper titled, "Three-mode controllable master-slave monostable multivibrators using current-feedback operational amplifiers," in [18] has addressed the multivibrator using three CFOAs, four resistors, a capacitor, an analogue switch, a single-pole single-throw (SPST) switch, a single-pole double-throw (SPDT) switch and three supply sources (V_A, V_B and I_B) and found the measured waveforms with master pulse width, T_m = 100 μs and slave pulse width T_s = 50 μs for various circuit. A novel full-wave rectifier/sinusoidal frequency doubler topology based on CFOAs presented in [19] has addressed full wave rectifier using two CFOA cells and three MOS switches and sinusoidal frequency doubler using two CFOA cells, two MOS switches and one resistor. The impedances R_x, R_z and R_y are found as 4 Ω, 54 kΩ, and ∞, respectively while voltage and current gain frequency are found as 592 MHz and 335 MHz, respectively using dual power supply of ± 1.25 V for this CFOA cell. A CFOA-based voltage-mode multifunction biquadratic filter and a quadrature oscillator using the CFOA cells is addressed in [20], in which the authors have implemented SIMO type biquadratic filter using 3-CFOA cells, 3-resistors and two capacitors and found angular frequency of 39.79 kHz and quality factor of 0.71 for band-pass (BP) response. The authors have also implemented voltage mode quadrature sinusoidal oscillator using 3-CFOA cells, 4-resistors and two capacitors and found frequency of oscillation of 38.84 kHz. The paper titled, "CMOS CFOA based Quadrature Oscillator," in [21] has implemented a CFOA cell by using CCII+ cell followed by an op-amp buffer and presented a quadrature oscillator as an application using two CFOA cells, resistors and capacitors and found current-mode oscillator with a frequency of 66.7 MHz. The paper titled, "Analytical Synthesis of High-Pass, Band-Pass and Low-Pass Biquadratic Filters and Its Quadrature Oscillator Application Using Current-Feedback Operational Amplifiers," in [22] has addressed voltage mode biquadratic filter and quadrature oscillator using 3-CFOA cells, 4-resistors and two capacitors and found center frequency of 757.88 kHz. The power consumption of the filter chip cell was addressed as 5.4 mW with a power supply of ±0.9 V.

In this paper, a LV-LP bulk-driven CFOA cell has been designed using new high gain OTA based CCII+ cell followed by an output buffer. The section 2 presents basic principle of CFOA and detailed discussion of circuit schematic, section 3 presents simulation result. To validate the workability of CFOA cell, SIMO type biquadratic filter and instrumentation amplifier have been implemented and described in section 4 and finally, section 5 concludes the various results related to the paper.

2. THE BASIC PRINCIPLE OF CFOA

The CFOA is a 4-terminals (Y, X, Z, and W) analog building block in which node voltages and corresponding node currents are expressed as V_Y, V_X, V_Z, V_W and I_Y, I_X, I_Z, I_W, respectively. The CFOA can be realized by cascade connection of CCII+ cell followed by a voltage buffer as shown in Fig.1(a) and its symbol in Fig.1(b).

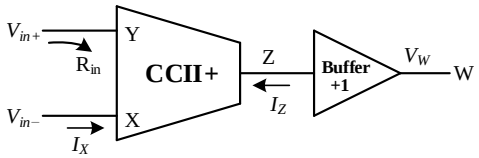

Fig.1(a). CFOA Topology

The voltage input node Y and current node Z offers very high impedance, ideally ∞, and practically very high. The X node and W node offers very low impedance, ideally 0, practically very low. There exists voltage buffer action between Y and X nodes which ensures $V_Y = V_X$ and between Z and W nodes which ensures $V_W = V_Z$. There lies current buffer action between Z and X nodes which ensures $I_Z = I_X$.

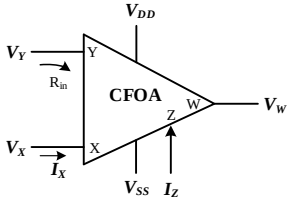

Fig.1(b). CFOA Symbol

The relationship between input and output variables are shown in matrix form and is given by Eq.(1)

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_W \end{bmatrix} \quad (1)$$

Which states that $I_Y = 0$, $V_X = V_Y$, $I_Z = I_X$ and $V_W = V_Z$ [20]. The voltage gain (α) is given by $V_X/V_Y = 1$ and $V_W/V_Z = 1$ and current gain (β) is given by $I_Z/I_X = 1$. Under the mismatch condition during fabrication process due to mismatch of threshold voltages of nMOS and pMOS transistors, the α and β values may slightly differ and may be less than unity, say 0.997 [19]. The X node has very low input impedance as 100% negative feedback is applied. The CFOA cell shows a very high slew rate and their bandwidth is independent of closed loop gain.

2.1 THE PROPOSED CIRCUIT SCHEMATICS

The proposed LV-LP CFOA cell is realized by a new high gain OTA introduced by J. Roh in his research paper, 'High-Gain Class-AB OTA with Low Quiescent Current' in 2006 which is the input core of analog and mixed signal circuit design [23]. In his research paper, the conventional current mirror OTA has been replaced by new high gain OTA by introducing two voltage controlled current source required in quiescent condition to enhance the gain operating in strong inversion region and suitable for high frequency applications. The proposed bulk-driven CFOA cell uses new high gain OTA in their input core operating in weak inversion region as shown in Fig.2.

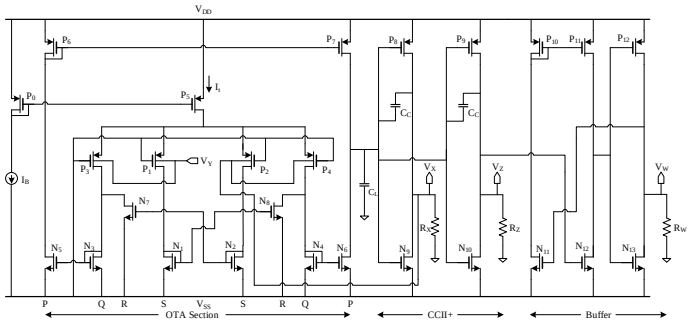

Fig.2. LV-LP CMOS CFOA cell

In Fig.2, *P*, *Q*, *R* and *S* shows the respective aspect ratios of nMOS loads N_5, N_3, N_7, a*N*d N_1, respectively. The transconductance and output impedance [23] of conventional current mirror OTA is given by

$$G_m = g_{m_{p3,4}} \times \frac{P}{Q} = \frac{I_t}{V_{od}} \times \frac{P}{Q} \quad (2)$$

$$R_{out} = r_{0_{N_6}} \left\| r_{0_{P_7}} \right. = \left(\frac{1}{\lambda_{N_6} I_{0,Q}} \left\| \frac{1}{\lambda_{P_7} I_{0,Q}} \right. \right) = \frac{2}{\left(\lambda_{N_6} + \lambda_{P_7}\right) I_t} \times \frac{Q}{P} \quad (3)$$

$$A_v = G_m R_{out} = \frac{2}{V_{od}} \times \frac{1}{\left(\lambda_{N_6} + \lambda_{P_7}\right)} \quad (4)$$

where V_{od} is the overdrive voltage, I_t is the tail transistor current, λ is channel length modulation coefficient and $I_{0,Q}$ is the drain current of output transistors in quiescent condition. The open loop gain of the conventional current mirror OTA is given by:

The slew rate of conventional current mirror OTA is limited to maximum output current $I_{0,max}$ and is given by

$$SR = \frac{I_{0,\max}}{C_L} = \frac{I_t \times \frac{P}{Q}}{C_L} \quad (5)$$

For increase of the quiescent current, the I_t or current mirror ratio P/Q must be increased for higher slew rate.

The open loop gain may be increased either by increasing the output impedance, R_{out} or by using the cascode device in the circuit. The use of cascode device limits the output voltage swing. It's one solution is to increase the R_{out} by decreasing the output current which proportionally decreases the G_m of conventional current mirror OTA [24].

The new high gain OTA shown in Fig.2 can be realized by adding two extra voltage controlled current source N_7 and N_8 to decrease the quiescent current at output stage and increase the output current of conventional current mirror OTA during large signal operation. In the quiescent condition, some noticeable amount of current drawn by the current source N_8 from the drain of P_4 thereby reducing the output current. The transistors P_1, P_2, N_1, N_2 senses the differential input voltage and control N_7 and N_8. If the current in P_4 is increased by $g_{mP4} \times V_{in}/2$, then the current in N_8 is decreased by $g_{mP1} \times V_{in}/2 \times (R/S)$, proportionally; where V_{in} is differential input voltage of transistors pairs (P_2, P_4) and (P_1, P_3). Hence, amount of current decrease in N_8 causes proportional increase in current of N_4 and the total current change in N_4 is equal to sum of the current change in P_4 and N_8.

The overall transconductance of new high gain OTA circuit is given by:

$$G_{m,new} = \frac{Q+R}{Q+R+S} \times G_m \times \frac{P}{Q} + \frac{S}{Q+R+S} \times G_m \times \frac{R}{S} \times \frac{P}{Q} \quad (6)$$

$$G_{m,new} = G_m \times \frac{P}{Q} + \frac{Q+2R}{Q+R+S} \quad (7)$$

The quiescent output current is reduced as

$$I_{0,Q} = \frac{I_t}{2} \times \frac{Q}{Q+R+S} \times \frac{P}{Q} = \frac{I_t}{2} \times \frac{P}{Q+R+S} \quad (6)$$

As a result, the output impedance of new high gain OTA increased to

$$R'_{out} = r_{0_{N_6}} \left\| r_{0_{P_7}} \right. = \frac{2}{\left(\lambda_{N_6} + \lambda_{P_7}\right) I_t} \times \frac{Q+R+S}{P} \quad (9)$$

The open loop gain of new high gain OTA is given by

$$A'_v = G_{m,new} \times R'_{out} \quad (10)$$

Since, the overall transconductance and output impedance have been increased by using Eq.(6) and Eq.(9), hence open loop gain has been increased.

Now, two CMOS inverter have been connected at the output of new high gain OTA in order to realize CCII+ cell. If the 100% negative feedback is applied from the output of first inverter to inverting terminal of OTA cell, then it becomes X terminal of CCII+ cell. Due to this feedback, impedance of X terminal is greatly reduced and ideally impedance should be zero and other input terminal of OTA do not have such negative feedback, hence

its impedance is very high, ideally infinite and becomes Y terminal of CCII+ cell. The output of second CMOS inverter becomes Z terminal and its impedance is very high. Two compensation capacitors C_C of equal value have been used between input and output of CMOS inverters in order to set better phase margin.

Using routine analysis, the voltage gain (α) of the CCII+ cell is obtained by the Eq.(11),

$$\alpha = \frac{V_X}{V_Y} = \frac{\left(g_{m_{P8}} + g_{m_{P9}}\right)\cdot\left(R_{0_{P8}} \left\| R_{0_{N9}}\right.\right)\cdot A_v'}{\left\{1+\left(g_{m_{P8}} + g_{m_{P9}}\right)\cdot\left(R_{0_{P8}} \left\| R_{0_{N9}}\right.\right)\cdot A_v'\right\}} \tag{11}$$

The current gain (β) can be obtained by

$$\beta = \alpha = \frac{I_Z}{I_X} \cong \frac{g_{m_{P8}} + g_{m_{N10}}}{g_{m_{P8}} + g_{m_{N9}}} \tag{12}$$

where, R_{0P8} and R_{0N9} are the output impedances of P_8 and N_9, g_{mP8} and g_{mN9} are the transconductances of P_8 and N_9, respectively and the open loop gain of new high gain OTA is A'_v [25].

In the output section of CCII+ cell, there exists a class AB unity gain voltage buffer comprised of the transistors $P_{10\text{-}12}$ and $N_{11\text{-}13}$ which was adapted from [12]. The common drain of transistors P_{12} and N_{13} form the buffered output node W of the CFOA cell which have low impedance output node. The *X*, *Z* and W nodes of the CFOA cell use the load resistors of 100 kΩ. The impedances at node *X*, *Y*, *Z* and *W* can be obtained by Eq.(13)-Eq.(16), respectively.

$$R_X = \frac{V_X}{V_Y} = \frac{\left(R_{0_{p9}} \,\|\, R_{0_{N9}}\right)}{\left\{1+\left(g_{m_{P8}} + g_{m_{N9}}\right)\cdot\left(R_{0_{P8}} \left\| R_{0_{N9}}\right.\right)\cdot A_v'\right\}} \tag{13}$$

$$R_Y = \frac{1}{2\pi f C_Y} \tag{14}$$

$$R_Z = R_{0_{p9}} \,\|\, R_{0_{N10}} \tag{15}$$

$$R_W \approx R_{0_{p12}} \,\|\, R_{0_{N13}} \tag{16}$$

where C_Y is the total capacitance at Y node, According to equation (13), R_X tends to be very small due to high value of closed loop gain $\{1+(g_{mP8}+g_{mN9})(R_{0P8}\|R_{0N9})A'_v\}$. R_Y is very large as *Y* node is input terminal and output impedance at *Z* node is large if the output resistor of second CMOS inverter comprising of transistors P_9 and N_{10} is large [25].

3. SIMULATION RESULTS

The proposed CFOA cell is simulated using 180 nm n-tub CMOS process technology and utilizing dual power supply of ±0.25 V with the bias current (I_B) of 20 nA at room temperature, i.e., at 27°C. The common mode voltage (V_{CM}) is equal to zero for dual power supply-based design. The proposed CFOA cell utilizes two compensation capacitors (C_C = 3pF) of equal values between input and output of two-CMOS inverters that are connected at the output of new high gain OTA. The circuit also uses three equal value of load resistors (R_X = R_Z = R_W =100 kΩ) at *X*, *Z* and *W* terminals. The aspect ratios of the CMOS devices used for the design of the proposed CFOA cell is shown in Table.1.

Table.1. Dimensions of the components used in proposed CFOA cell.

Device	W/L (μm/μm)	Device	W/L (μm/μm)
P_0	2/1	N_7, N_8	6/1.2
P_1, P_2	5.4/0.6	N_9, N_{10}	40/0.18
P_3, P_4, P_6, P_7	10.8/0.6	N_{11}, N_{12}, N_{13}	10/1
P_5	8/1	C_C	3 pF
P_8, P_9	50/0.18, M=2	C_L	15 pF
P_{10}, P_{11}	50/1, M=2	R_X	100 kΩ
P_{12}	50/1	R_Z	100 kΩ
N_1, N_2	3.6/1.2	R_W	100 kΩ
N_3, N_4	1.2/1.2	I_B	20 nA
N_5, N_6	7.2/1.2	Power Supply	±0.25 V

In CFOA structure there lies 100 % negative feedback between X terminal and one terminal of input pair which offers voltage buffering action between Y and X nodes. This CFOA cell has utilized OTA cum two inverters-based design topologies, so current buffering is expected for both of X and Z nodes. The DC input voltage is applied on the V_Y node and swept between ±0.25 V while the output is determined at X, Z and W nodes. The output responses in Fig.3 shows a very good linearity in the rail-to-rail operation between –250 mV to 250 mV for X, Z nodes.

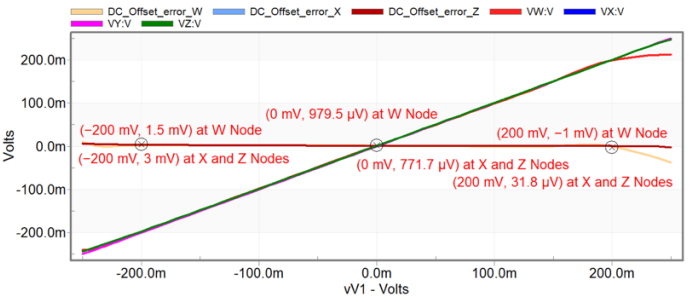

Fig.3. DC Sweep response

A very good linearity is obtained for W node between –250 mV to 200 mV. The DC offset error when no signal is applied on Y terminal i.e. at 0 mV are determined as 979.5 μV at W node, 771.7 μV at X and Z nodes. The errors at –200 mV are found to be 1.5 mV at W node, 3 mV at X and Z nodes. The errors at +200 mV are found to be –1 mV at W node, 31.8 μV at X and Z nodes.

The slew rate determines the speed of the proposed circuit that how the output voltage changes per second and simulated in pulse transient mode. The input pulse of 250 mV with 1 kHz of frequency is applied on Y terminal and slew rates are determined at X, Z and W nodes. The Fig.4 depicted the positive slew rate (SR+) of 27.2 V/ms at X and Z node for the rising edge of the square-wave and negative slew rate (SR–) of 16.3 V/ms at the X and Z node for the falling edge of the square wave while for the W node SR+ of 63.3 V/ms and SR– of 33 V/ms for loads R_X = R_Z = R_W = 100 kΩ.

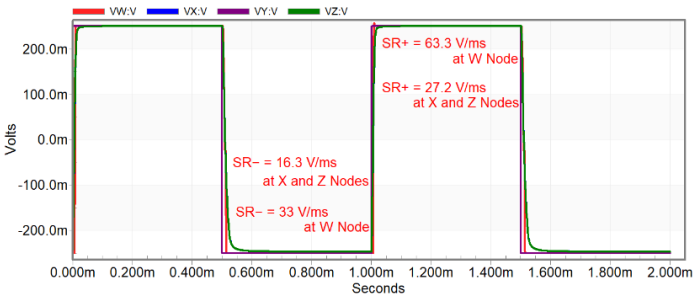

Fig.4. Pulse transient response

The Fig.5 shows the total harmonic distortion (THD) when a sinusoidal signal of 100 mV amplitude with 250 Hz frequency is applied on Y terminal and simulated in transient response mode whereas THD will be determined at X, Z and W nodes and found to be −50.2 dB at X and Z nodes and −42.5 dB at W node which shows a very good linearity between input and outputs since the THD should be less than 1% or −40 dB.

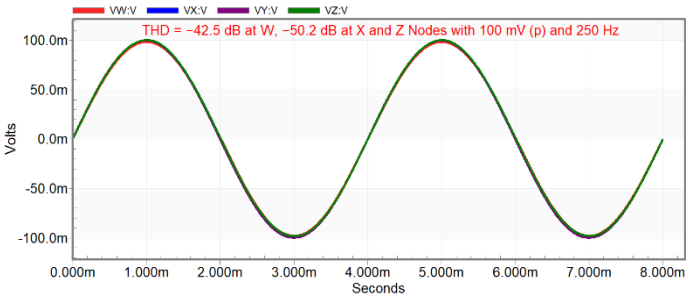

Fig.5. THD of proposed CFOA cell

When V_{ac} signal is applied on Y terminal of proposed CFOA cell and output response to be considered at X, Z and W nodes, then it is expected to be 0 dB gain obtained at individual nodes at certain frequency of interest. It is considered as strong voltage buffering action between X, Y and Z, W nodes and strong current buffering action between X and Z nodes. The load resistances at X node, say R_X, Z node, say R_Z and W node, say R_W have been set to 100 kΩ in this AC simulation set up.

The Fig.6 shows the ac analysis result when ac signal is applied at the Y terminal. This figure depicted the −3dB bandwidth of 22.3 kHz with C_L of 15 pF with R_X = R_Z = R_W = 100 kΩ for both of X and Z nodes as output terminal nodes and 18.7 kHz for W node. The power dissipation of proposed CFOA cell is 485.3 nW.

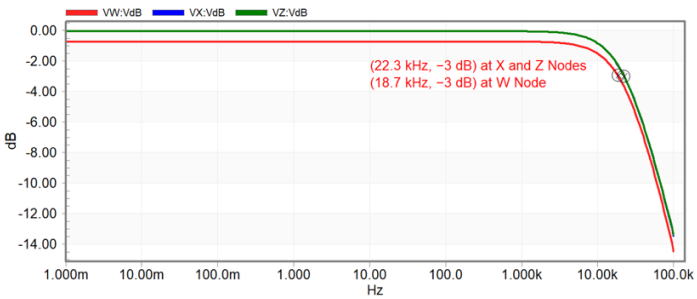

Fig.6. AC response with −3 dB bandwidth with load resistances

The Fig.7 shows the ac response when load resistances have been removed. It shows a −3 dB bandwidth of 104.6 kHz, 107.5 kHz and 113 kHz for X, Z and W nodes, respectively as output nodes.

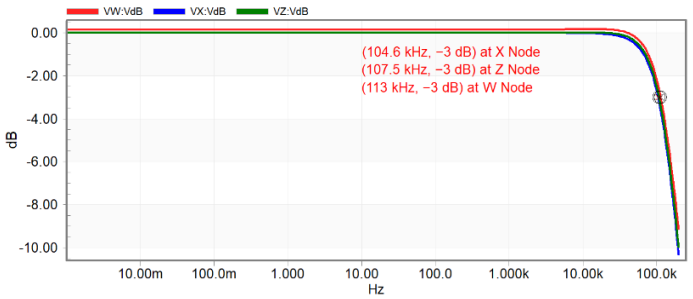

Fig.7. AC response with −3 dB bandwidth without load resistances

When V_{ac} input voltage is applied at Y terminal under ac analysis in simulation setup, then it is expected as unity gain at X and W nodes and there is a good voltage buffering action between X, Y and W, Z nodes and a good current buffering action between X and Z nodes. The Fig.8, 9 and 10 shows the voltage gains X, W nodes and current gain at Z node of the proposed CFOA cell, respectively.

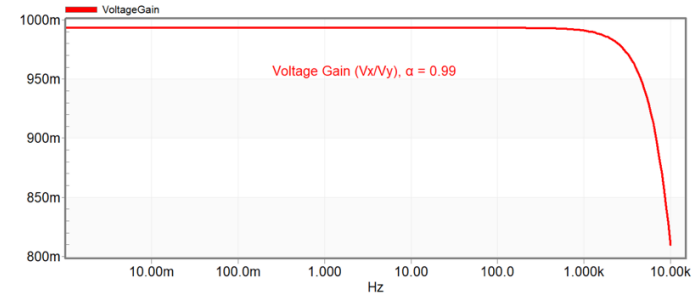

Fig.8. Voltage Gain response at X Node

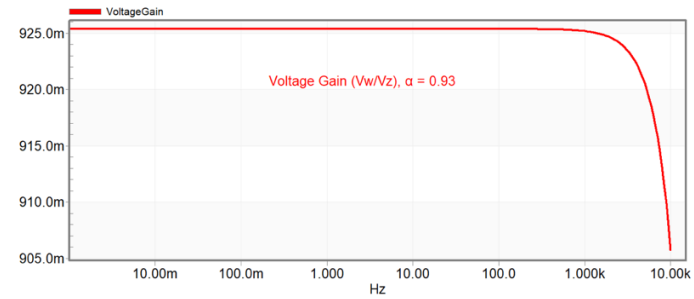

Fig.9. Voltage Gain response at W Node

The Eq.(11) and (12) shows the voltage gain (α) and current gain (β) of CFOA cell. The mean of voltage gain (α) at X, W nodes and current gain (β) (for 1 mHz to 10 kHz range) are found to be 0.99, 0.93 and 1.0000045, respectively.

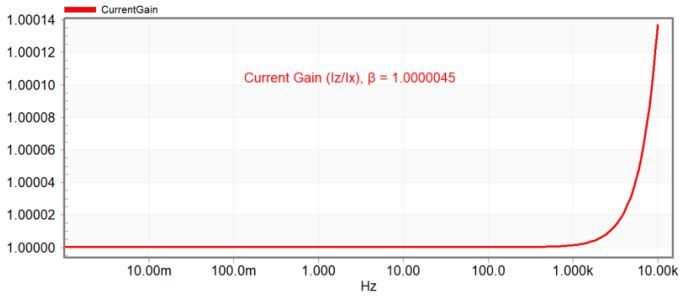

Fig.10. Current Gain response at Z Node

The noise is an unwanted signal present in the circuit due to fluctuations of the voltage or current received at the output along with the original which severely affect the proper operation and the circuit becomes noisy. It may be internal or external interferences like fluctuations of the supply voltage, electromagnetic waves from external sources. The internal noises are like thermal and flicker noises, due to vibrations of devices, heat produced from resistors which can be minimised by using proper transistor sizes.

The total input thermal and flicker noise power spectral density (*PSD)* in weak inversion operation at gate-terminal $\bar{V}_{sn}^2$ could be expressed as:

$$\bar{V}_{sn}^2 = \bar{V}_{sn,th}^2 = \bar{V}_{sn,\left(\frac{1}{f}\right)}^2 = 2\frac{q_{i_{D_i}}}{g_m^2} + \frac{1}{g_m^2}\frac{K'_{FP}g_{m_i}^2}{g_m^2\left(\frac{W}{L}\right)_i f} \quad (17)$$

The total input thermal and flicker noise power spectral density (*PSD)* in weak inversion operation at bulk-terminal $\bar{V}_{snB}^2$ could be expressed as:

$$\bar{V}_{snB}^2 = \bar{V}_{snB,th}^2 + \bar{V}_{snB,\left(\frac{1}{f}\right)}^2 = \frac{2q_{i_{D_i}}}{g_{m_{b_i}}^2} + \frac{1}{g_{m_{b_i}}^2}\frac{K'_{FP}g_{m_i}^2}{g_{m_{b_i}}^2\left(\frac{W}{L}\right)_i f} \quad (18)$$

where g_m and g_{mbi} are the gate and bulk-transconductances of the input pair.

If V_{ac} input is applied at Y terminal, the output noise may be observed at X, Z and W nodes of CFOA cell. The output noise associated at X, Z and W nodes when referred to input terminal is called input referred noise which is found to be 0.8 µV/sqrt Hz (same for both X and Z nodes) and for W node, 0.9 µV/sqrt Hz at 1 kHz frequency. A comparison of proposed CFOA cell performances with references [19] [26] [27] [28] is presented in Table.2.

Table.2. Comparison of the proposed CFOA cell performance to that of [19] [26] [27] [28]

Parameters	**This Work**	**[19]**	**[26]**	**[27] Fig.1**	**[27] Fig.2**	**[28]**
Process (µm)	0.18	0.25	0.18	0.35	0.35	0.25
I_B (nA)	20	-	70	50000	50000	-
Power Supply (V)	±0.25	±1.25	0.5	1.5	1.5	±0.75
C_L (pF)	15	-	-	-	-	-
Power dissipation (nW)	485.3	-	4700	552000	544000	456000
3-dB bandwidth with R_L (kHz)	22.3 @ X, Z, 18.7 @ W	592000, 335000, 574000	160	264700, 806800, 335300	134600, 149900, 291100	120000
3-dB bandwidth without R_L (kHz)	104.6 @ X, 107.5 @ Z, 113 @ W	-	300	-	-	-
Impedance at Y (TΩ)	1.8	∞	0.145	∞	∞	∞
Impedance at X, W nodes (kΩ)	6, 4.8	0.004	6.18, 2.48	0.0254, 0.0254	0.0394, 0.0394	< 0.036
Impedance at Z (MΩ)	1.7	0.054	132	0.1925	0.1836	0.001-0.008
Voltage gain α, (V_X/V_Y)	0.99	0.989	0.999	0.9948	1.018	1
Voltage gain α, (V_W/V_Z)	0.93	0.989	0.999	0.9948	1.027	-
Current gain β, (I_Z/I_X))	1.0000045	1.024	0.998	1	1.073	-
DC offset error (µV)	979.5 @ W, 771.7 @ X, Z	-	-	171.2, 85.8	30500 @ W, 6900 @ X, 4.6 @ Z	-
Input Voltage Dynamic Range (V)	–0.25V to +0.25V @ X, Z –0.25V to +0.2V @ W	-	±0.25	+0.75 to +1.23 @ X, Z and W	+0.82 to +1.2 @ X, +0.84 to 1.2 @ Z, W	±0.65
SR, average (V/ms)	48.2@ W,	-	50	-	-	-

	21.8 @ X, Z					
THD (dB)	–42.5[a] @ W, –50.2[a] @ X, Z	-	-	–39.2[b] @ W, –44.4[b] @ X, Z	–20[b] @ W, –27[b] @ X, –21[b] @ Z,	-
Inoise (μV/√Hz) @ 1 kHz	0.8 @ X, Z, 0.9 @ W	-	535	-	-	2.5
FOM (nW/kHz)	4.3	-	15.7	1.6	1.9	3.8
Simulated/Fabricated	Simulated	Simulated	Simulated	Simulated	Simulated	Simulated

[a]for 100 mV peak @ 250 Hz, THD[b] @ 200 mV

The performance of CFOA cell can be determined in terms of figure of merit (FOM), which defines the ratio of total power dissipation per 3-dB bandwidth.

FOM = (Total Power Dissipation)/Bandwidth (19)

The Fig.11 - Fig.13 shows simulated input referred noise for this CFOA cell.

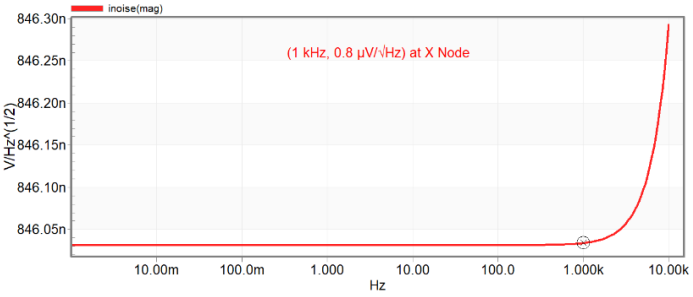

Fig.11. Input referred noise at X node

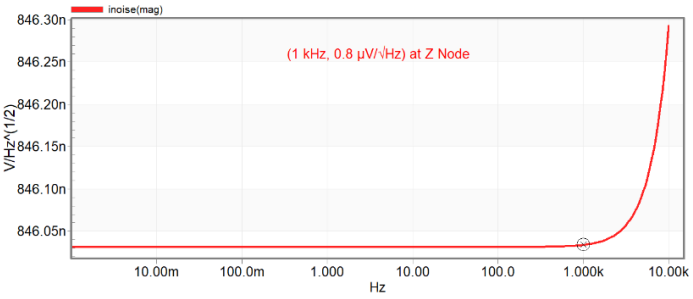

Fig.12. Input referred noise at Z node

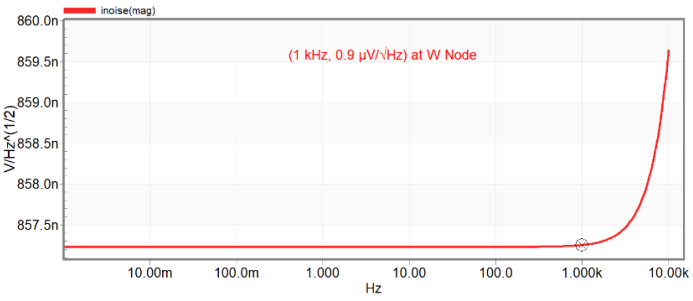

Fig.13. Input referred noise at W node

4. APPLICATIONS

To ensure the workability and utility of proposed LV-LP new high gain OTA based CFOA cell, it has been utilized to design voltage mode SIMO type biquadratic filter and single ended and fully differential instrumentation amplifier as analog signal processing applications.

4.1 SIMO TYPE BIQUADRATIC FILTER

The circuit shown in Fig.14 is a SIMO type biquadratic filter which is adopted from the book referred in [8]. The circuit is capable to produce all five generic filter responses, namely: Low-Pass (LP), High-Pass (HP), Band-Pass (BP), Band-Reject (BR) and All-Pass (AP).

The circuit is comprised of 4-CFOA cells, 9-resistors and 2-capacitors. The circuit contains two integrators with two grounded capacitors made of $CFOA_2$ and $CFOA_3$ and two summers made of $CFOA_1$ and $CFOA_2$.

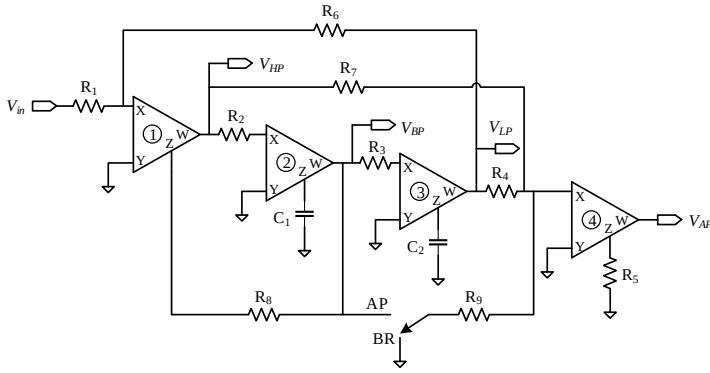

Fig.14. SIMO Type Voltage Mode Biquadratic Filter

The filter responses like LP, HP, BP and AP are obtained to their respective nodes V_{LP}, V_{HP}, V_{BP}, and V_{AP}, respectively while BR response can be obtained by setting the switch to BR position and obtained at V_{BR} node. For the simulation, the equal value design has been considered for simplicity and all the resistors have been loaded for equal value of 100 kΩ and all the capacitors have equal value of 10 nF. Using routine analysis, their transfer function have been obtained in Table 3.

Table.3. Transfer function of voltage mode SIMO type biquadratic filter

Filter Type	Transfer Function
Low-Pass (LP)	$\frac{V_{LP}}{V_{in}} = \frac{H_0\omega_0^2}{D(s)} = \frac{-\left(\frac{R_6}{R_1}\right)\frac{R_8}{R_6R_2C_1R_3C_2}}{S^2 + \frac{1}{R_2C_1}S + \frac{R_8}{R_6R_2C_1R_3C_2}}$

High-Pass (HP)	$\frac{V_{HP}}{V_{in}} = \frac{H_0 s^2}{D(s)} = \frac{-\left(\frac{R_8}{R_1}\right)S^2}{S^2 + \frac{1}{R_2C_1}S + \frac{R_8}{R_6R_2C_1R_3C_2}}$
Band Pass (BP)	$\frac{V_{BP}}{V_{in}} = \frac{H_0 \frac{\omega_0}{Q_0} S}{D(s)} = \frac{\left(\frac{R_8}{R_1}\right)\frac{1}{R_2C_1}S}{S^2 + \frac{1}{R_2C_1}S + \frac{R_8}{R_6R_2C_1R_3C_2}}$
Band-Reject (BR)	$\frac{V_{BR}}{V_{in}} = \frac{H_0\left(s^2+\omega_0^2\right)}{D(s)} = \frac{\left(\frac{R_8}{R_1}\right)\left(S^2 + \frac{R_9}{R_6R_2C_1R_3C_2}\right)}{S^2 + \frac{1}{R_2C_1}S + \frac{R_8}{R_6R_2C_1R_3C_2}}$
All-Pass (AP)	$\frac{V_{AP}}{V_{in}} = \frac{H_0\left(s^2 + \left(\frac{\omega_0}{Q_0}\right)s + \omega_0^2\right)}{D(s)} = \frac{\left(\frac{R_8}{R_1}\right)\left(S^2 - \frac{1}{R_2C_1}S + \frac{R_8}{R_6R_2C_1R_3C_2}\right)}{S^2 + \frac{1}{R_2C_1}S + \frac{R_8}{R_6R_2C_1R_3C_2}}$

The Fig.15 shows SIMO type biquadratic filter responses that has been simulated for the equal value of the capacitors $C_1 = C_2 =$ 10 nF and all resistors have equal value of 100 kΩ. It is found that for the LP response, f_H = 162 Hz, for the HP response, f_L = 107.6 Hz, for BP response f_L = 85.8 Hz, f_H = 196.3 Hz, BW = 110.5 Hz, central frequency f_0 = 129.8 Hz and the quality factor Q is obtained as Q = 1.174 and for BR f_L = 74.7 Hz, f_H = 285.3 Hz, BW = 210.6 Hz, central frequency f_0 = 146 Hz and the simulated central frequency is obtained as 134 Hz with a notch depth of –30.2 dB. Each filter response dissipates a power of 1.9 µW.

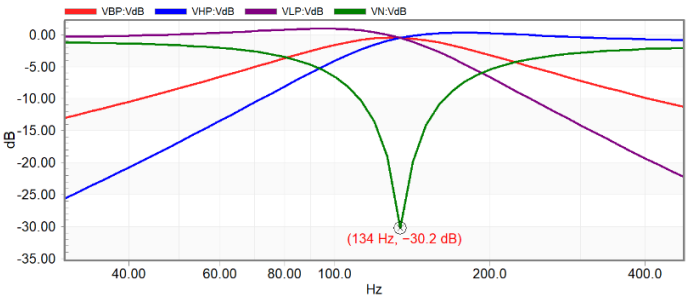

Fig.15. SIMO type biquadratic filter responses

4.2 INSTRUMENTATION AMPLIFIER

An instrumentation amplifier (IA) is device which has large differential gain and very low common mode gain. It amplifies well a very low-level input signal buried in high noise levels and provides very high signal to noise ratio (SNR) at its output. The major advantages of IA are high input impedance, high common-mode rejection ratio (CMRR). An IA is a device which amplifies the difference between the two input lines while highly attenuating any common-mode noise [29]. The circuit diagram shown in Fig.16 is a single ended instrumentation amplifier which are comprised of 2-CFOA cells and a grounded resistor [8].

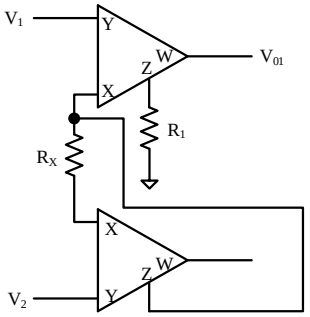

Fig.16. Single Ended Instrumentation amplifier

The voltage gain of this IA is given by Eq.(20),

$$A_v = \frac{V_{01}}{(V_2 - V_1)} = \frac{R_1}{R_X} \tag{20}$$

The Fig.17 shows the gain and phase plot of single ended instrumentation amplifier and determined as 63 dB of gain at 1 Hz, 93.2 kHz GBW and 50.3° of phase-margin (PM) which shows stable operation of the circuit. The Fig.18 shows its CMRR which is determined as 68.2 dB at 1 Hz and reduces to 40 dB at 1.3 kHz. This IA consumes power of 1.1 µW.

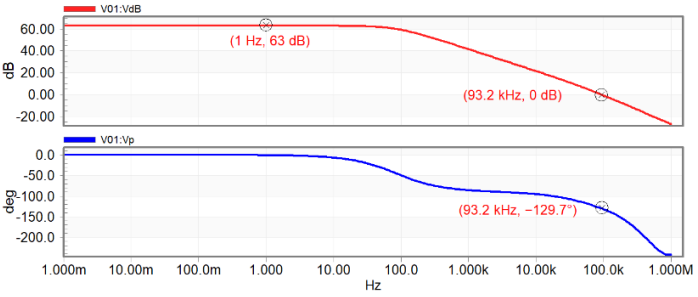

Fig.17. Gain and Phase Plot of single ended instrumentation amplifier

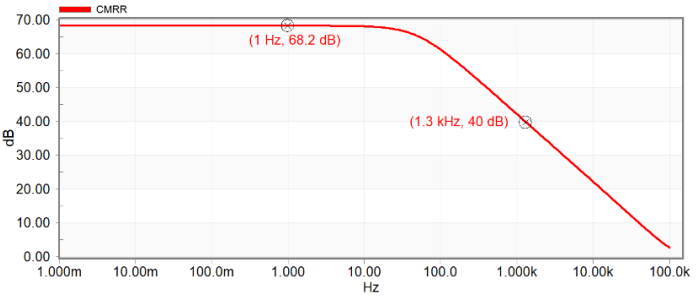

Fig.18. CMRR of single ended instrumentation amplifier

The Fig.19 shows the fully differential instrumentation amplifier which is comprised of 2-CFOA cells and two grounded resistors connected at Z nodes of CFOA cells.

It provides two-fold currents at Z node of $CFOA_1$ to facilitate 6 dB gain rise compared to a simple IA of unfolded I_Z type for $CFOA_2$. For the equal value of resistors at Z node, $R_1 = R_2 = R$; The voltage gain of this IA is given by Eq.(21),

$$A_v = \frac{V_{02} - V_{01}}{(V_2 - V_1)} = \frac{2R}{R_X} \quad (21)$$

The Fig.20 shows the gain and phase plot of fully differential amplifier and determined as 66.4 dB gain at 1 Hz, 126 kHz of GBW and 57.6° of phase-margin (PM) which shows stable operation of the circuit. This IA consumes power of 1.1 µW.

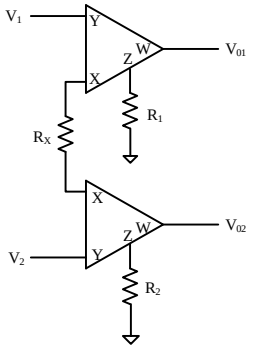

Fig.19. Fully differential instrumentation amplifier

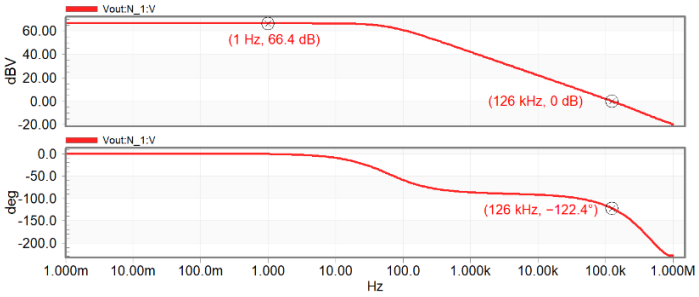

Fig.20. Gain and Phase Plot of fully differential instrumentation amplifier

5. CONCLUSION

In this paper, a LV-LP bulk driven new high gain OTA followed by CCII+ and voltage buffer-based CMOS CFOA cell presented. The circuit utilizes the dual power supply of ± 0.25 V and the bias current of 20 nA. The circuit dissipates a total power of 485.3 nW. The circuit offers a very good input common mode range (ICMR) and shows linearity nearly rail to rail operation of about ± 0.25 V at X and Z node while linearity for W node is very close to rail to rail operation of about −0.25 V to +0.2 V. The circuit has least input referred noise of 0.8 µV/sqrt Hz at 1 kHz for X and Z node while 0.9 µV/sqrt Hz at 1 kHz for W node and total harmonic distortion of −50.2 dB at X, Z nodes and −42.5 dB at W node with 100 mV of peak value at 250 Hz is applied. To demonstrate the workability of the proposed circuit, voltage mode SIMO type biquadratic filter using four CFOA cells and single ended and fully differential instrumentation amplifiers have been designed as an application example. The proposed circuit can be used for LV-LP applications like bioelectronics, biosensors and extended to the biomedical systems.

REFERENCES

[1] B.J. Maundy, A.R. Sarkar and S.J. Gift, "A New Design Topology for Low-Voltage CMOS Current Feedback Amplifiers", *IEEE Transactions on Circuits and Systems-II*, Vol. 53, No. 1, pp. 34-38, 2006.

[2] S. Pennisi, "High-performance CMOS Current Feedback Operational Amplifier", *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 1573-1576, 2005.

[3] S.J.G. Gift and B. Maundy, "Improving the Bandwidth Gain-Independence and Accuracy of the Current Feedback Amplifier", *IEEE Transactions on Circuits and Systems-II*, Vol. 52, No. 3, pp. 136-139, 2005.

[4] R. Mita, G. Palumbo and S. Pennisi, "Low-Voltage High-Drive CMOS Current Feedback Op-Amp", *IEEE Transactions on Circuits and Systems-II*, Vol. 52, No. 6, pp. 317-321, 2005.

[5] P. Mongkolwai, T. Pukkalanun, T. Dumawipata and W. Tangsrirat, "CFOA-Based Single Resistance Controlled Quadrature Oscillator", *Proceedings of Annual Conference on Micro-Processor and Controller*, pp. 1147-1150, 2008.

[6] G.Ferri and N. Guerrini, "High-Valued Passive Element Simulation using Low-Voltage Low Power Current Conveyors for Fully Integrated Applications", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 48, No. 4, pp. 405-409, 2001.

[7] B.J. Maundy, I.G. Finvers and P. Aronhime, "Alternative Realizations of CMOS Current Feedback Amplifiers for Low-Voltage Applications", *Analog Integrated Circuits and Signal Processing*, Vol. 32, pp. 157-168, 2002.

[8] R. Senani and V.K. Singh, "Current Feedback Operational Amplifier and Their Applications", Springer, 2013.

[9] A.K. Singh and R. Senani, "CFOA-based State-Variable Biquad and its High-Frequency Compensation", *IEICE Electronics Express*, Vol. 2, No. 7, pp. 232-238, 2005.

[10] G. Palumbo and S. Pennisi, "Analysis of the Noise Characteristics of Current-Feedback Operational Amplifier", *Microelectronics Reliability*, Vol. 40, No. 2, pp. 321-327, 2000.

[11] B. Maundy, P.B. Aronhime and S. Gift, "A New Configuration for Current Feedback Operational Amplifiers", *Proceedings of Midwest Symposium on Circuits and Systems*, Vol. 3, pp. 547-550, 2002.

[12] B.J. Maundy, I.G. Finvers and P. Aronhime, "Alternative Realizations of CMOS Current Feedback Amplifiers for Low Voltage Applications", *Analog Integrated Circuits and Signal Processing*, Vol. 32, pp. 157-168, 2002.

[13] G.D. Cataldo, A.D. Grasso and S. Pennisi, "Two CMOS Current Feedback Operational Amplifiers", *IEEE Transactions on Circuits and Systems-II*, Vol. 54, No. 11, pp. 944-948, 2007.

[14] F. Elsayed, M.F. Ibrahim, Y.H. Ghallab, W. Badawy and B. Maundy, "A New 90nm CMOS Current Feedback Operational Amplifier", *Proceedings of Canadian Conference on Electrical and Computer Engineering*, pp. 903-906, 2009.

[15] G. Skotis and C. Psychalinos, "Multiphase Sinusoidal Oscillators using Current Feedback Operational Amplifiers", *Proceedings of International Conference on Microelectronics*, pp. 86-89, 2009.

[16] S. Nikoloudis and C. Psychalinos, "Multiple Input Single Output Universal Biquad Filter with Current Feedback Operational Amplifiers", *Circuits, Systems and Signal Processing*, Vol. 29, pp. 1167-1180, 2010.

[17] S. Saxena and P.K. Mishra, "A Novel Equi-amplitude Quadrature Oscillator Based on CFOA", *International Journal of Advanced Science and Technology*, Vol. 31, pp. 93-98, 2011.

[18] H.C. Chien, "Three-Mode Controllable Master-Slave Monostable Multivibrators using Current-Feedback Operational Amplifiers", *IET Circuits, Devices and Systems*, Vol. 8, No. 6, pp. 543-553, 2014.

[19] E. Yuce, S. Minaei and M.A. Ibrahim, "A Novel Full-Wave Rectifier/Sinusoidal Frequency Doubler Topology based on CFOAs", *Analog Integrated Circuits and Signal Processing*, Vol. 93, pp. 351-362, 2017.

[20] S.F. Wang, H.P. Chen, Y. Ku and P. Y. Chen, "A CFOA-Based Voltage-Mode Multifunction Biquadratic Filter and a Quadrature Oscillator using the CFOA-Based Biquadratic Filter", *Applied Sciences*, Vol. 9, Issue 11, pp. 1-19, 2019.

[21] S. Tandel, N. Bhagat and U.P. Khot, "CMOS CFOA based Quadrature Oscillator", *Proceedings of International Conference on Electronics and Sustainable Communication Systems*, pp. 940-943, 2020.

[22] S.F. Wang, H.P. Chen, Y. Ku and M.X. Zhong, "Analytical Synthesis of High-Pass, Band-Pass and Low-Pass Biquadratic Filters and its Quadrature Oscillator Application using Current-Feedback Operational Amplifiers", *IEEE Access*, Vol. 9, pp. 13330-13343, 2021.

[23] J. Roh, "High-Gain Class-AB OTA with Low Quiescent Current", *Analog Integrated Circuits and Signal Processing*, Vol. 47, pp. 225-228, 2006.

[24] T. Sharan and V. Bhadauria, "Ultra-Low-Power Bulk and Gate-Driven, Class AB, Subthreshold Transconductor", *Proceedings of International Conference on Signal Processing and Integrated Networks*, pp. 921-926, 2015.

[25] A. Reda, M.F. Ibrahim and F. Farag, "Input-Output Rail-to-Rail CMOS CCII for Low Voltage-Low Power Applications", *Microelectronics Journal*, Vol. 48, pp. 60-75, 2016.

[26] M. Kumngern, F. Khateb and T. Kulej, "0.5 V Bulk-Driven CMOS Fully Differential Current Feedback Operational Amplifier", *IET Circuits, Devices and Systems*, Vol. 13, No. 3, pp. 314-320, 2019.

[27] G. Raikos and C. Psychalinos, "Low-Voltage Current Feedback Operational Amplifiers", *Circuits, Systems and Signal Processing*, Vol. 28, pp. 377-388, 2009.

[28] S.A. Mahmoud, A.H. Madian and A.M. Soliman, "Low-Voltage CMOS Current Feedback Operational Amplifier and Its Application", *ETRI Journal*, Vol. 29, No. 2, pp. 212-218, 2007.

[29] H. Austerlitz, "*Analog Signal Conditioning*", 2nd Edition, Parker Hannifin Corporation, 2003.