ISSN: 2229-6948(ONLINE)
DOI: 10.21917/ijct.2013.0101

IMPLEMENTATION AND COMPARISON OF DIFFERENT CIC FILTER STRUCTURE FOR DECIMATION

M. Madheswaran[1] and V. Jayaprakasan[2]
[1]*Centre for Advanced Research, Department of Electronics and Communication, Mahendra Engineering College, India*
Email: madheswaran.dr@gmail.com
[2]*Department of Electronics and Communication, Jawaharlal Nehru Technological University Anantapur, India*
Email: jprakasan@gmail.com

Abstract
This paper briefs an implementation of different CIC filter architectures for decimation. The different decimation filter structures are implemented using cascaded integrator-comb filter to work for the down sampling ratio of 8. The prototype is designed with MATLAB Simulink model and it is converted to VHDL code using Xilinx system generator. Prototype is implemented in Virtex V-XC5VLX110T-3ff1136 FPGA kit and simulation results and device utilization reports are generated and tabulated. Finally different architectures are compared using number of used LUTs, Registers, Power consumption etc.

Keywords:
FPGA – Field Programmable Gate Arrays, SRC - Sampling Rate Conversion, DDC – Digital Down Converter, CIC - Cascaded Integrator Comb Filter

1. INTRODUCTION

In recent years, with the rapid development of VLSI (Very Large Scale Integration) technologies, FPGA (Field Programmable Gate Array) has been widely applied in the field of digital signal processing, because of its reprogrammability, reconfigureability, low cost, high logic density and high reliability. Sample rate conversion (SRC) is the process of changing sampling rate of data stream from a specific sampling rate to another sampling rate. With the conversion of communication and software market SRC is a necessary component in many of today's applications, like CDs, Audio players, Multitask Digital audio workstations, Tape recorders, computer communication, WiMAX, WiFi etc.

In most of these applications, very high quality sample rate converter is required. Most high quality SRCs currently available in the market employ a digital filter that provides the required quality by upsampling the data to a very high sampling rate followed by down sampling to the required output sampling rate. The digital filters used in the SRC are the strong options for removing noise, shaping spectrum and minimizing Inter Symbol Interference (ISI) in communication system. The CIC filter is one which is used for larger data rate changes.

The use of non-recursive filter structures has been increasing in the recent years for various applications. This is due to the low power consumption and increase in the circuit speed, especially when the decimation factor and the filter order are high. The frequency response of CIC (Cascaded-integrator comb) decimation filter with various techniques has been reported in the past few decades by many researchers. In 1981, Eugene Hogenauer [1] has proposed a class of digital filter without multipliers for interpolation and decimation and used limited storage elements to have better economical hardware implementations. The filter was designated as CIC filter, because it consists of an equal number of integrator sections operating at the high sampling rate and a comb section operating at the low sampling rate as compared to Integrator section.

H.Aboushady et al. [3] have presented a multistage polyphase structure with maximum decimation factor in the first stage which significantly improved the power consumption, area and maximum sampling frequency. G. J. Dolecek and S. K. Mitra [4] designed a CIC filters with improved magnitude response. The authors proposed a different structure that consists of a comb section and a sharpening comb section with the latter section operating at a lower rate than the high input rate for the realization of comb-decimation filter with a sharpened magnitude response. G. J. Dolecek et al. [5] proposed the CIC decimation filter structure with compensation techniques to improve the passband performance. With this review of literatures there is a need for comparative study of different CIC filter structure for research work.

2. CASCADED INTEGRATOR-COMB FILTER

CIC (cascaded-integrator-comb) filter is widely used as the sample rate change filter due to its simplicity. The CIC filters are multiplierless structures, consisting of only adders and delay elements which is a great advantage when aiming at low power consumption. These filters are frequently used in digital down and up converters. The Direct implementation of CIC decimation filter is shown in Fig.1.

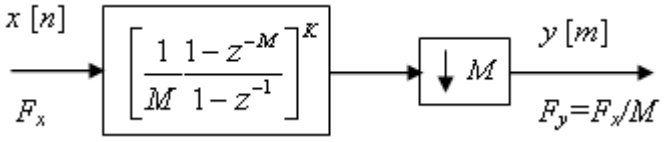


Fig.1. Direct Implementation Structure of CIC filter

In direct implementation of CIC decimation filter structure the whole circuit is operate at maximum sampling frequency F_x before decimation takes place. Hence the power consumption of direct implementation CIC decimation filter is very high. So in this paper, we present a different representation of the CIC filter structure for decimation.

The transfer function of the cascaded-comb decimation filter shown in Fig.1 is given by,

$$H(z)=\left[\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right]^K \quad (1)$$

2.1 IIR – FIR STRUCTURE

A simplified implementation of CIC filter structure is shown in Fig.2. In this structure, the IIR filters work at the higher input sampling frequency and the FIR filters work at a sampling frequency M times lower than IIR filter. Hence the power consumption of this architecture is reduced significantly. But the major drawback of this architecture is operating at maximum sampling frequency.

2.2 NON-RECURSIVE STRUCTURE

The transfer function of the cascaded comb decimation filter given in Eq.(1) can be rewritten in simplified form as,

$$H(z) = \prod_{i=0}^{(\log_2 M)-1} (1+z^{-2^i})^K \quad (2)$$

This decimation filter can be realized using a cascade of $\log_2 M$ FIR filter. This structure shown in Fig.3, is called as 'non-recursive structure' because there are only FIR filters needed for implementation while in IIR-FIR structure is a recursive one due to IIR filters. So there is no stability related issues in non-recursive structure. Reducing sampling rate in the earlier stages helps to reduce the power consumption.

2.3 POLY-PHASE STRUCTURE

In the non-recursive structure the output is decimated by factor of 2, implies that half of the output is not used. This leads to waste of computational resources and increased power consumption. By applying polyphase decomposition we can get a more efficient implementation as shown in Fig.4. Each FIR filter in non-recursive structure can be implemented by 2-component polyphase decomposition of its transfer function [3].

$$H(z) = (1+z^{-1})^K = H_0(z^2) + z^{-1} H_1(z^2) \quad (3)$$

In this work we are using filter of order $K = 1$, so the Eq.(3) becomes,

$$H(z) = 1 + z^{-1} \quad (4)$$

where, $H_0(Z)$, $H_1(Z)$ are given as,

$$H_0(Z) = 1$$

$$H_1(Z) = 1$$

This structure allows the placement of the downsamplers at the input of the filter, making whole structure work at half the frequency it used to work in non-recursive structure at the cost of increased circuitry.

3. SIMULINK MODEL AND FPGA DESIGN OF DIFFERENT CIC FILTER STRUCTURE

Simulink is a software package for modeling, simulating and analyzing dynamical systems. It supports linear and nonlinear systems modeled in continuous time, sampled time, or a hybrid of the two. Systems can also be multirate, i.e., have different parts that are sampled or updated at different rates. For modeling, Simulink provides a graphical user interface (GUI) for building models as block diagrams, using click-and-drag mouse operations. Simulink includes a comprehensive block library of sources, sinks, linear and nonlinear components and connectors.

We can also customize and create our own blocks. Fig.5, Fig.6 and Fig.7 shows the Simulink design of different CIC filter structure. The digital sine wave signal is given as input and output is plotted in the output scope. The recent advancement in the VLSI technology particularly in FPGA as made possible, the realization of advanced Digital Signal Processing algorithm in high frequency domain. With this development a single chip solution is possible for complex DSP based applications like, ADC, Decimation and Interpolation in the communication system. Digital implementation couples with signal processing algorithms greatly enhance the system performance, reduced the cost and increase the reliability of the system. Low power DSP systems are implemented by changing the sampling clock for each subsystem depending on the real requirements. The sampling rate change results in aliasing; this necessitates the use of filters to overcome it. So in this paper we discuss the implementation of different style of CIC structure.

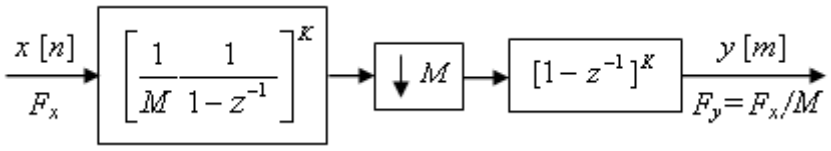


Fig.2. IIR – FIR Structure of CIC filter

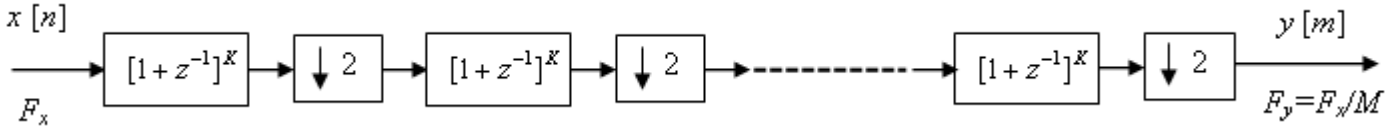


Fig.3. Non-Recursive Structure of CIC filter

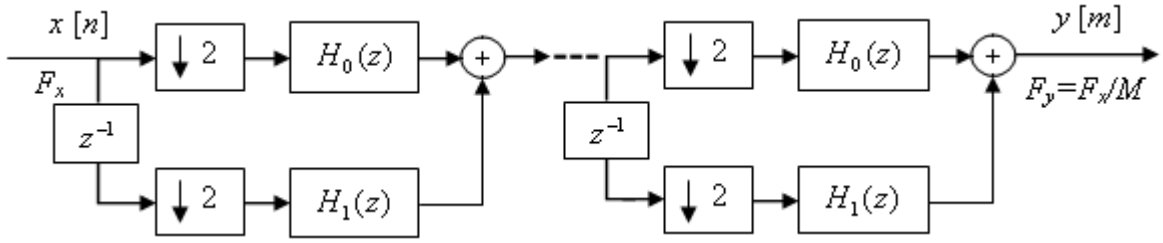


Fig.4. Polyphase Structure of CIC filter

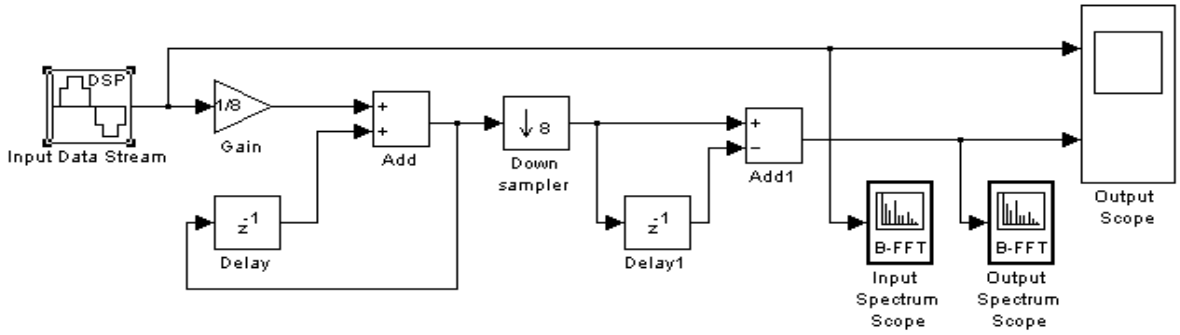


Fig.5. Simulink Model for IIR – FIR CIC filter Structure

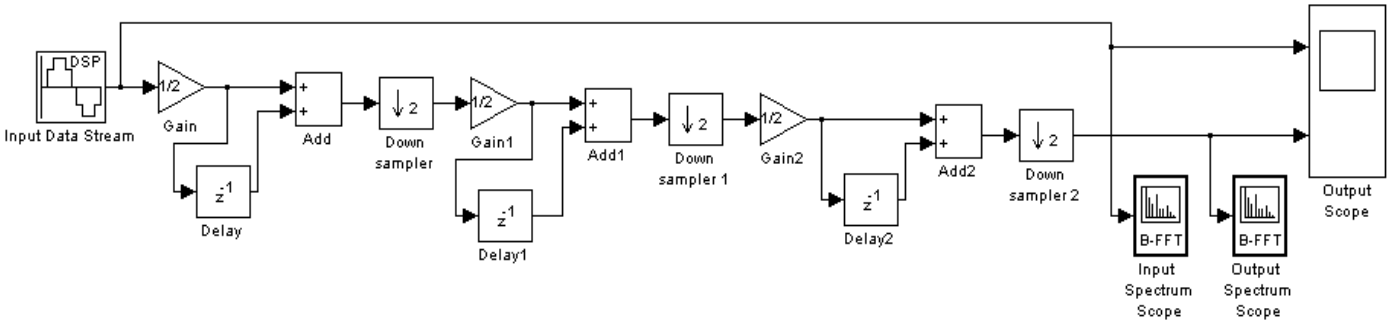


Fig.6. Simulink Model for Non-Recursive CIC filter Structure

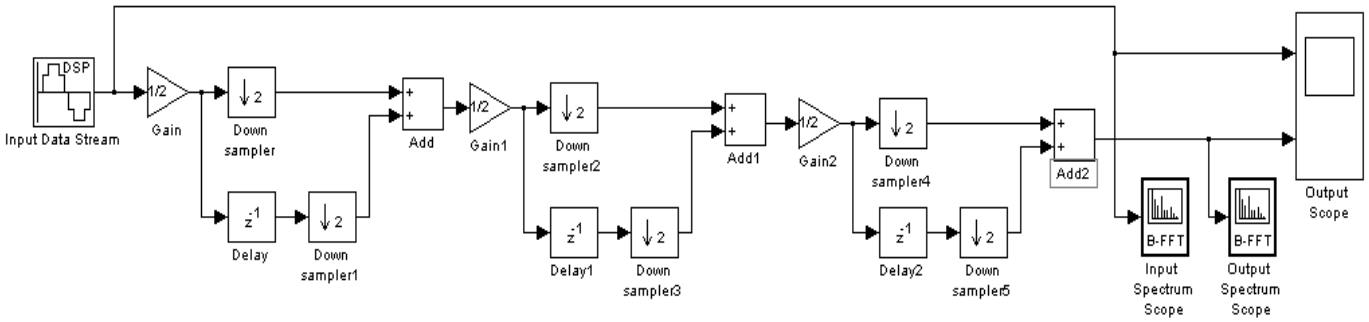


Fig.7. Simulink Model for Polyphase CIC filter Structure

The initial model was designed and tested in Simulink, a software package from The Mathworks for modeling, simulating and implementing the dynamic systems. The Fig.8, Fig.9 and Fig.10 shows the implementation model of the different CIC Filter structure. Here the Simulink model is used as the reference model for synthesis of the design in FPGA. To target the module for FPGA, we choose to use Xilinx System Generator, which provide a Simulink blockset that is then converted to VHDL for synthesis and implementation.

Each filter structure is designed in MATLAB Simulink environment using FDA Tool and tested the Decimation filter architecture with different input signal sample rate. The same will be implemented using Xilinx tool boxes FIR Compiler 5.0 and FDA Tool, the VHDL code and Testbench for the designed Simulink model was generated using System Generator HDL Coder. This method efficient and it takes less time to test and implement a design as compared to the task of writing HDL Code for individual component.

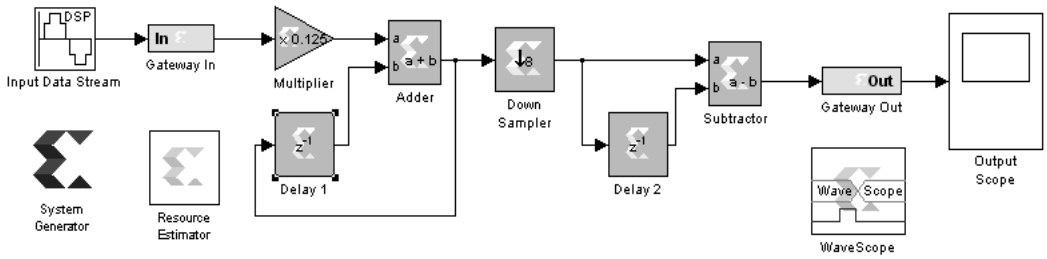


Fig.8. IIR – FIR Implementation Structure of CIC filter

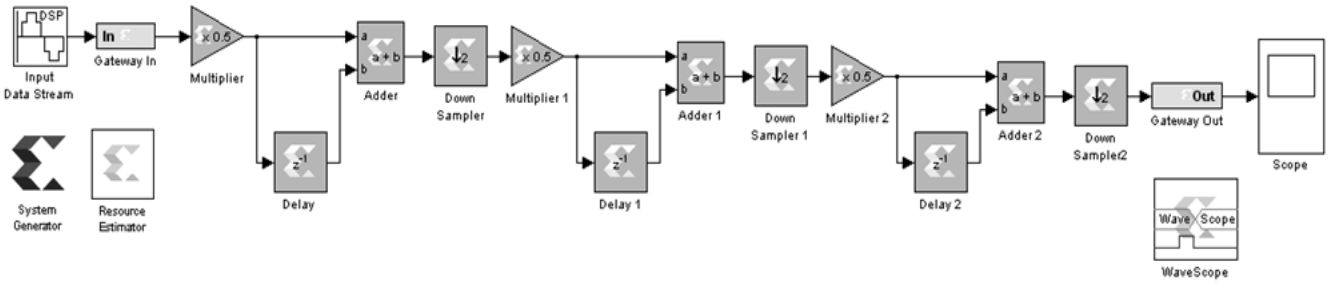


Fig.9. Non-Recursive Implementation Structure of CIC filter

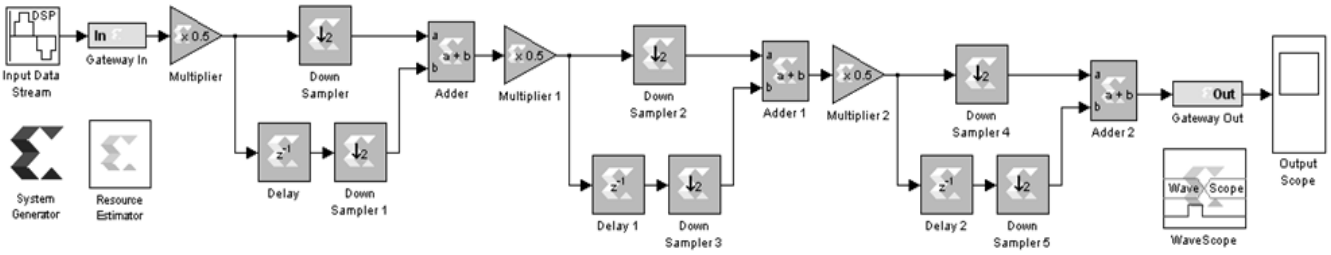
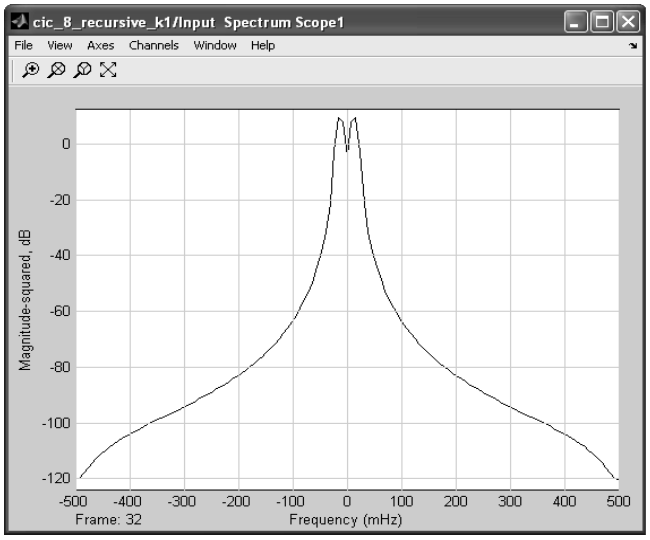


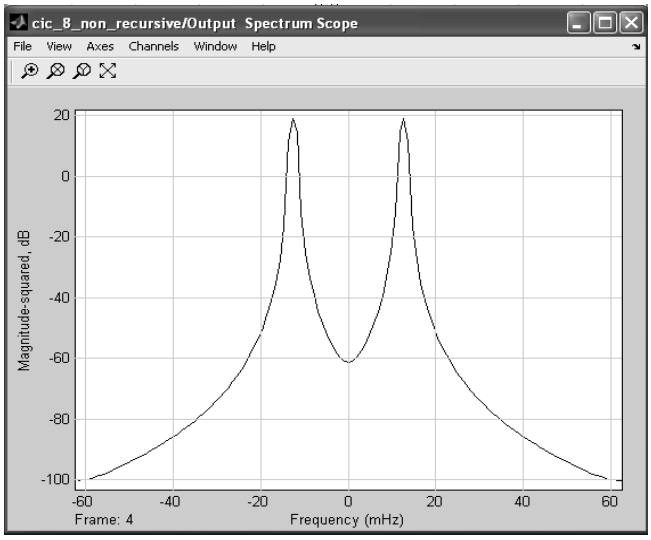
Fig.10. Polyphase Implementation Structure of CIC filter

4. RESULTS AND COMPARISIONS

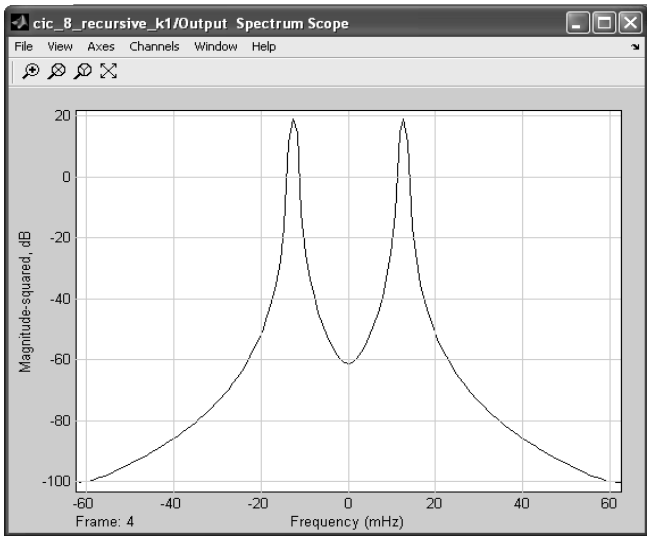
The different CIC Filter structures are designed in MATLAB Simulink environment. The same will be implemented using Xilinx tool boxes, the VHDL code and Testbench for the designed Simulink model was generated using System Generator HDL Coder. All the CIC filter structures are implemented for decimation ratio of M = 8 with K = 1 and K = 2. IIR-FIR structure has minimum resource utilization for a given decimation factor and the increase in the resource utilization with decimation factor is minimum compared to other structures. Moreover the increase in resource utilization with increase in the decimation factor remains the same. From the comparison shown in the Table.1, non-recursive structure has the minimum power consumption followed by recursive structure and worst in case of polyphase CIC filter structure. The power spectral density of the input and output signals are plotted using Buffered FFT scope which is shown in Fig.11. Fig.12 – Fig.15 shows the input and output signals of recursive, non-recursive and polyphase CIC based decimation filter structures respectively.



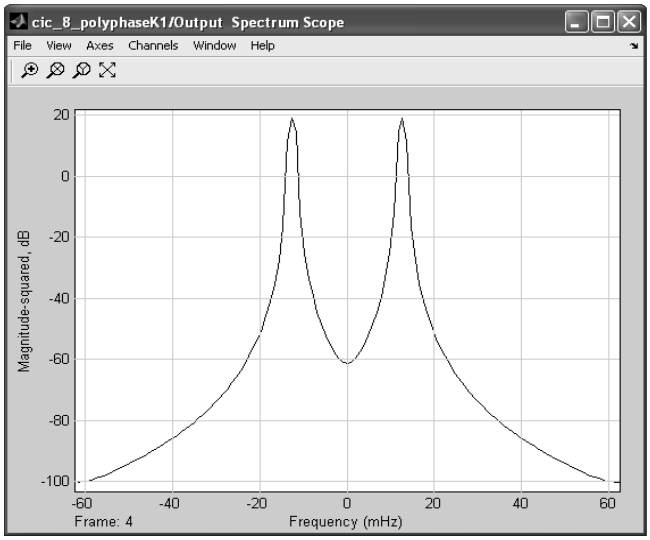
(a) Input Signal to the Simulink Model



(c) Decimated Output Signal (Non-Recursive)



(b) Decimated Output Signal (Recursive)



(d) Decimated Output Signal (Polyphase)

Fig.11. Power Spectrum of Input and Output Signals

Table.1. Device Utilization Summary for Decimation Factor $M = 8$

Device	**Recursive Structure**		**Non-Recursive Structure**		**Polyphase Structure**	
	***K* = 1**	***K* = 2**	***K* = 1**	***K* = 2**	***K* = 1**	***K* = 2**
Number of Slice Registers	63	101	133	186	190	256
Number of Slice LUTs	52	84	102	150	101	194
Number of LUT Flip Flop pairs used	79	125	152	212	225	361
Number of Bonded IOB'S	30	30	33	33	32	31
Average Fan-out	1.87	1.82	1.79	1.79	2.37	2.11
Power Consumption in Watts	0.029	0.033	0.028	0.029	0.031	0.034

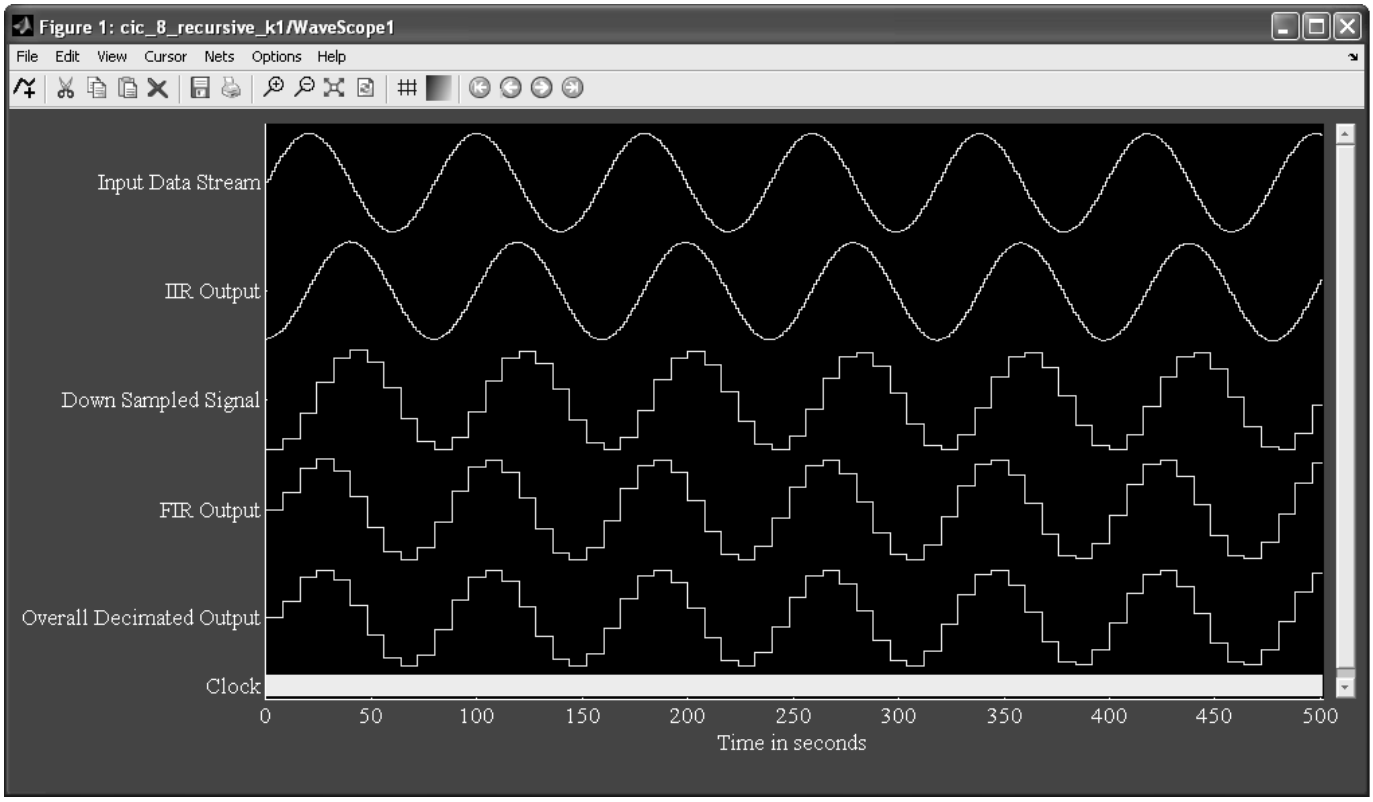


Fig.12. Simulation results of IIR – FIR based CIC filter Structure

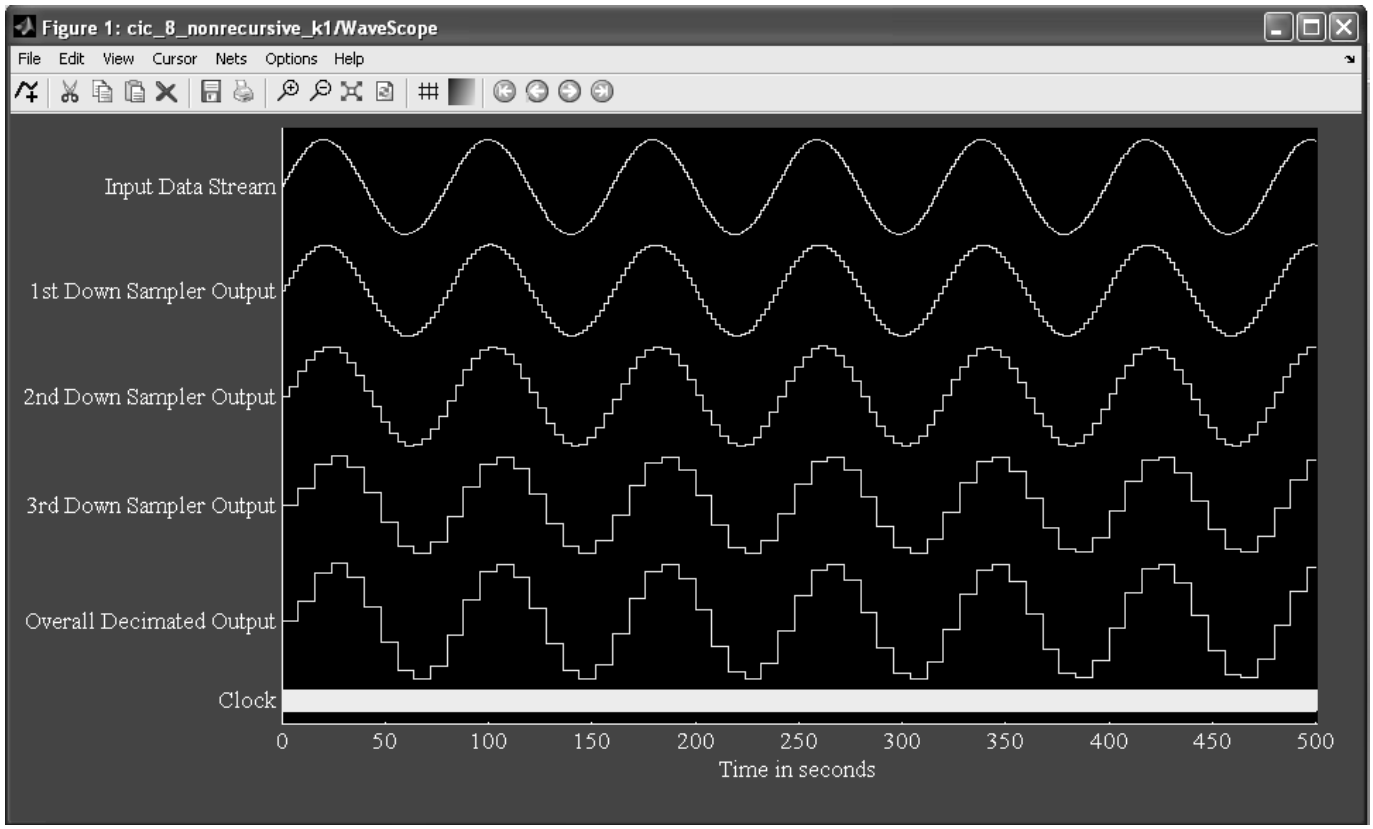


Fig.13. Simulation results of Non – Recursive based CIC filter Structure

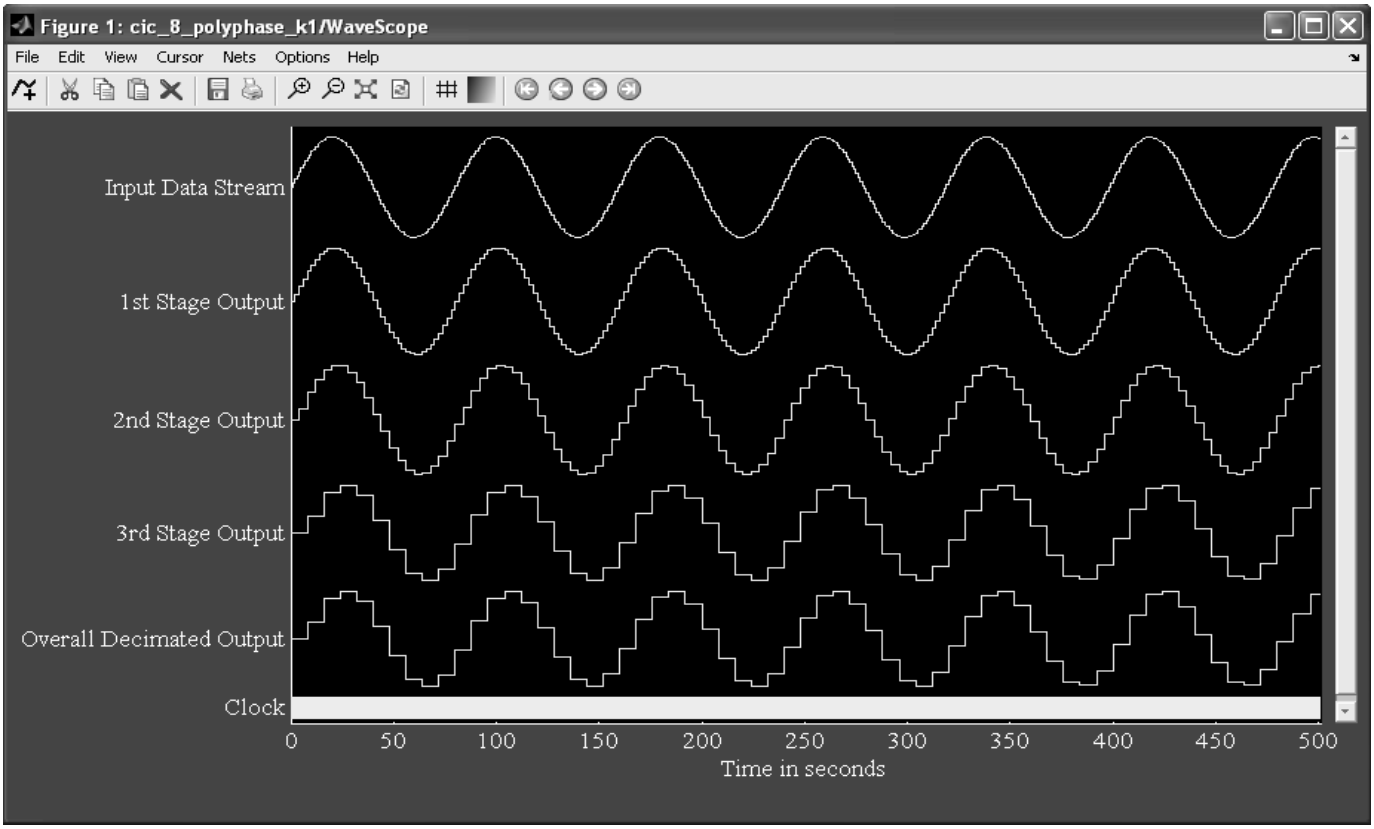


Fig.14. Simulation results of Polyphase based CIC filter Structure

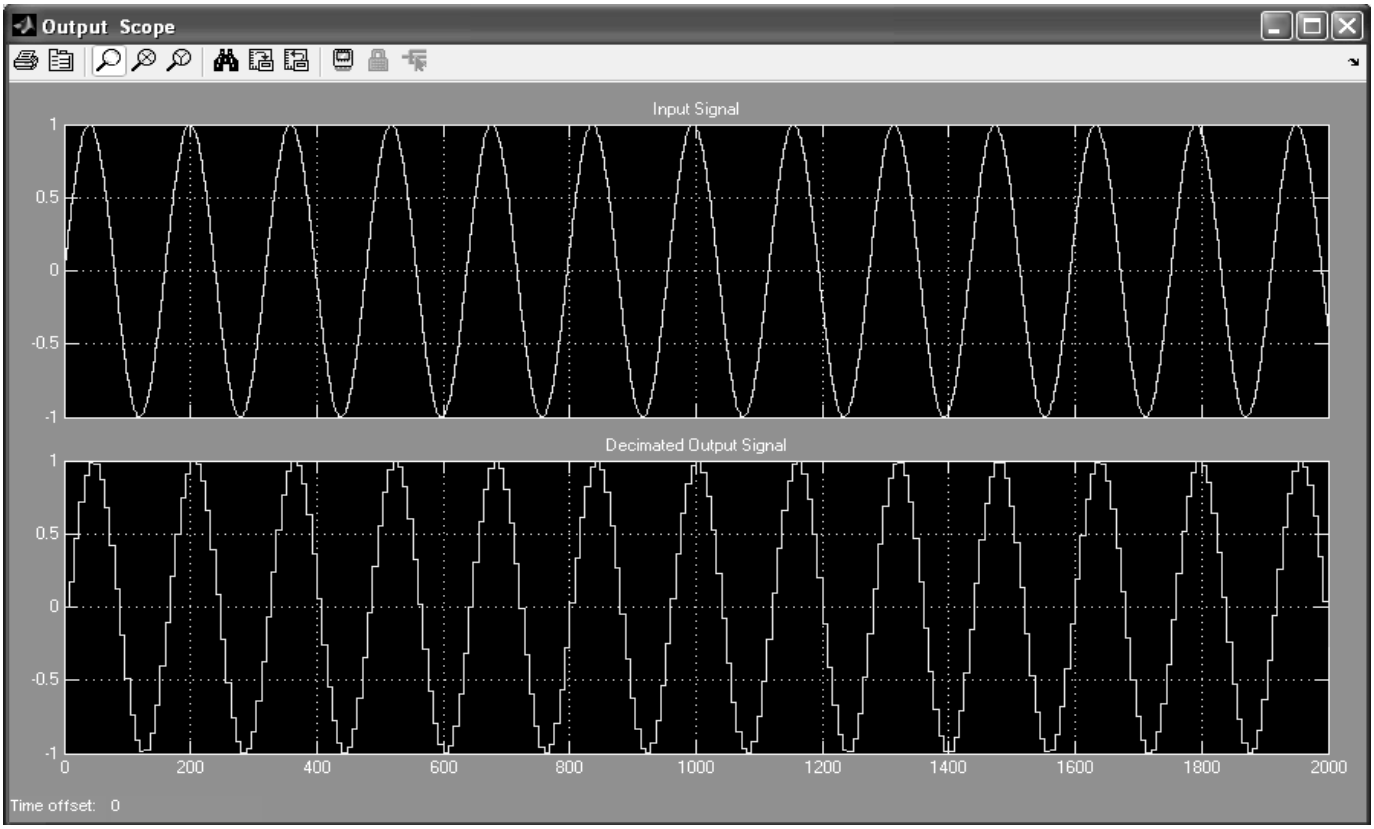


Fig.15. Different CIC Filter Structures input and decimated output signal representation by scope

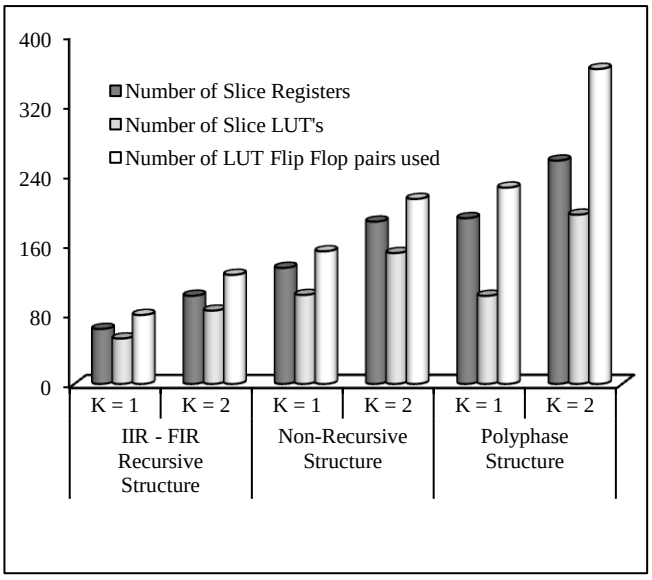


Fig.16. Resource Utilization Comparison Chart between different CIC Filter structures

5. CONCLUSION

The CIC Filter structures are implemented with the help of Virtex-V XC5VLX110T-3ff1136 FPGA kit considering decimation factor 8 and the results are obtained. The performance of the filter with various structures was compared. The result shows that each CIC filter structure has some advantages and disadvantages. Recursive structure utilizes less LUT's compared to other two structures and non-recursive structure consumes less power compared to other two structures. Comparing all three CIC filter structures, the non-recursive structure consumes less power and utilizes less LUTs. Hence for design and implementation of CIC decimation filter the non-recursive structure is best for wireless applications.

REFERENCES

[1] E. B. Hogenauer, "An economical class of digital filters for decimation and interpolation", *IEEE Transactions on Acoustics, Speech and Signal Processing*, Vol. 29, No. 2, pp. 155–162, 1981.

[2] S. K. Mitra, "*Digital Signal Processing—A Computer Based Approach*", Second Edition, McGraw-Hill, 2001.

[3] H. Aboushady, Y. Dumonteix, M. M. Louerat and H. Mehrez, "Efficient polyphase decomposition of comb decimation filters in Sigma-Delta analog-to-digital converters", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 48, No. 10, pp. 898 – 903, 2001.

[4] Gordana Jovanovic-Dolecek and Sanjit K Mitra, "On Design of CIC Decimation Filter with Improved Response", *IEEE 3rd International Symposium on Communications, Control and Signal Processing*, pp. 1072 - 1076, 2008.

[5] Gordana Jovanovic Dolecek and Fred Harris, "Design of CIC Compensator Filter in a Digital IF Receiver", *IEEE International Symposium on Communications and Information Technologies*, pp. 638 - 643, 2008.

[6] Ljiljana Milić, "*Multirate Filtering for Digital Signal Processing: MATLAB Applications*", Information Science Reference, First Edition, 2009.

[7] Rozita Teymourzadeh and Masuri Othman, "VLSI Implementation of Cascaded Integrator Comb Filters for DSP Applications", *4th National Technical Postgraduate symposium*, 2006.

[8] Xilinx, Inc., "*Virtex-V platform FPGA handbook*", Vol. 3, No. 1, 2012.

[9] The Mathworks Inc., "*Simulink, Dynamic System Simulation for matlab using Simulink*", Natick Massachusetts, 1999.