ISSN: 2229-6948 (ONLINE)
DOI: 10.21917/ijct.2010.0007

FPGA BASED ASYNCHRONOUS PIPELINED MB-OFDM UWB TRANSMITTER BACKEND MODULES

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Abstract
In this paper, a novel scheme is proposed which comprises the advantages of asynchronous pipelining techniques and the advantages of FPGAs for implementing a 200Mbps MB-OFDM UWB transmitter digital backend modules. In asynchronous pipelined system, registers are used as in synchronous system. But they are controlled by handshaking signals. Since FPGAs are rich in registers, design and implementation of asynchronous pipelined MB-OFDM UWB transmitter on FPGA using four-phase bundled-data protocol is considered in this paper. Novel ideas have also been proposed for designing asynchronous OFDM using Modified Radix-2^4 SDF and asynchronous interleaver using two RAM banks. Implementation has been performed on ALTERA STRATIX II EP2S60F1020C4 FPGA and it is operating at a speed of 350MHz. It is assured that the proposed MB-OFDM UWB system can be made to work on STRATIX III device with the operating frequency of 528MHz in compliance to the ECMA-368 standard. The proposed scheme is also applicable for FPGA from other vendors and ASIC.

KeyWords:
MB-OFDM UWB, Asynchronous Pipelining, FPGA, Asynchronous OFDM, Stratix III.

1. INTRODUCTION

Over the last six and half years, Ultra-Wide Band (UWB) communication systems have attracted many people from industry and the academia. The reason for all this excitement is that this technology promises to deliver data rates that can scale from 110 Mb/s at a distance of 10 meters up to 480 Mb/s at a distance of **2** meters in realistic multi-path environments all while consuming very little power and silicon area.[1]. In February 2002, the FCC (Federal Communication Commission) opened up 7,500 MHz of spectrum (from 3.1 GHz to 10.6 GHz*)* for use by UWB devices. In the Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) UWB system, the entire available UWB spectrum is divided into several sub-bands of 528 MHz bandwidth each. In each sub-band, an OFDM symbol is transmitted and then, the system switches to another sub-band. The MB-OFDM transceivers could be used in portable devices, such as camcorders, and laptops, as well as in fixed devices, such as TVs and desktops [2].Therefore the complexity, high speed and power consumption of the transceivers are very important issues to be addressed.

Asynchronous designs which do not require a global clock for synchronization have many potential advantages like avoiding clock-skew problem, low power consumption, high speed, low EMI, etc., Asynchronous designs have been successfully applied to control oriented applications such as chip interfaces [3], datapath Components such as adders and dividers [4] as well as general purpose microprocessors such as SUN CounterFlow Processor [5].. They use handshaking signals between their components in order to perform the necessary synchronization and sequencing of events. Micropipelines is a popular design style for building asynchronous circuits, invented by Ivan Sutherland and introduced in his Turing Award Lecture in 1988[6]. Among various asynchronous protocols, in our work, four-phase bundled-data protocol is used to generate the handshaking signals between the components. The bundled-data protocol uses a single REQuest and ACKnowledge wire and a set of data wires. The REQ wire is used to inform the receiver about the validity of the data on the data bundle. The four-phase protocol ensures the validity of the data by a low-to-high transition of REQ wire. A Muller-C element is used to generate the various control signals like REQ and ACK in the handshaking circuit.

FPGA based system design gains extensive popularity due to the flexibility and complexity they provide. The advanced FPGA cores include on a single chip, the embedded RAM, a RISC processor, dedicated multiplier blocks, multigigabit transceivers in addition to the logic cells and flip flops. Intellectual property (IP) cores have been developed for a variety of applications and are available off the shelf. The availability of the RISC processor and the logic cell arrays as well as the embedded RAM on a single FPGA enables the apportioning of a task between software and hardware in an optimum manner [7]. The Internet reconfigurability of these devices enables the partitioning to be carried out even dynamically by remote control.

In our previous work, synchronous pipelined MB-OFDM UWB transmitter backend is implemented on ALTERA FPGA [8]. In this paper, FPGA based and asynchronous pipelined MB-OFDM UWB transmitter backend is proposed to exploit the advantages of both asynchronous techniques and FPGAs. This paper is organized as follows. In section II, MB-OFDM UWB transmitter is discussed. In section III, asynchronous pipelining system is described. In section IV, the proposed asynchronous pipelined MB-OFDM UWB transmitter is explained. Section V deals with the implementation results and this paper is concluded in section VI.

2. MB-OFDM UWB TRANSMITTER

The multi-band OFDM system is an OFDM solution proposed for the UWB WPAN (ECMA 368) physical layer standard. In that proposal, the whole available ultra- wide band spectrum between 3.1GHz-10.6GHz is divided into several sub-bands with smaller bandwidth. The bandwidth of each sub-band is larger than 500MHz in compliance with FCC rules for UWB transmission. Specifically, the proposal uses 528MHz sub-bands. Fig.1 shows the band planning for the multiband OFDM system.[8] . In each subband a normal OFDM modulated signal with N=128 subcarriers and QPSK modulation is used. The transmission is not done continually on all sub-bands. Rather, it is time multiplexed between different bands in order to use a single hardware for communications over different sub-bands.

2.1 TRANSMITTER BLOCKS

The transmitter architecture for a MB-OFDM UWB system is shown in Fig. 2 [8].

2.1.1 Scrambler and Encoder:

The input data is randomized by using a scrambler with a polynomial $1+x^{14}+x^{15}$ as shown in Fig.3 [8]. A rate 1/3 convolutional code, with a generator polynomial of $[133, 145, 175]_8$ with the constraint length of K=7 is used to correct channel errors as shown in Fig.4 [8]. Additional coding rate of 5/8 used to obtain the data rate of 200Mbps is generated by puncturing the rate 1/3 mother code with a puncturing code of 15/8.

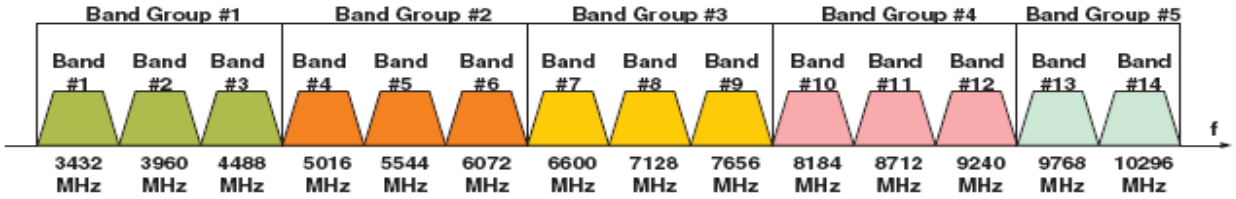

Fig.1 Frequency Planning for MB-OFDM UWB System

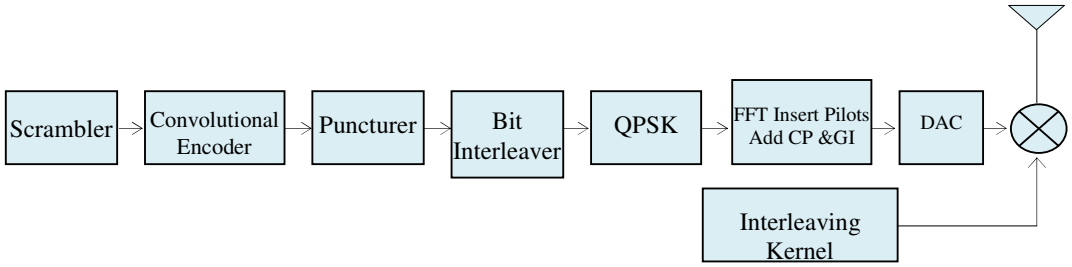

Fig. 2 MB-OFDM UWB Transmitter Architecture

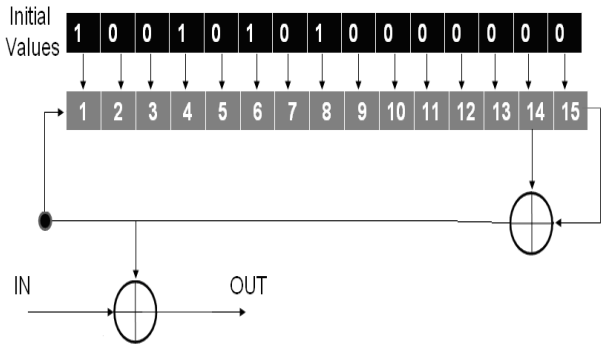

Fig.3. Scrambler

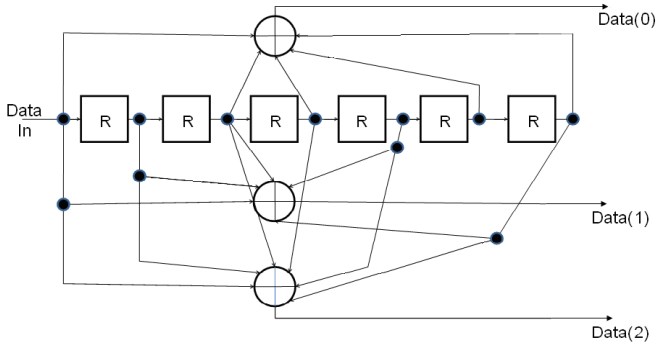

Fig.4 Convolutional Encoder

2.1.2 Bit Interleaver:

Bit interleaving is used to provide robustness against burst errors. Two stages of interleaving are performed in series to combat frequency selective fading. The first stage is referred to as inter-interleaving and it permutes bits to exploit frequency diversity across the 3 lower sub-bands (i.e., inter sub-band interleaving) [9]. The second stage of interleaving, known as inner-interleaving, permutes the bits across data tones of each OFDM symbol within each sub-band (i.e., inner sub-band interleaving) [9]. Interleaver also, carefully designed using two different RAM banks which are working in tandem with different write and read addresses and clock rates to provide optimum results as shown in the Fig 5 [8].

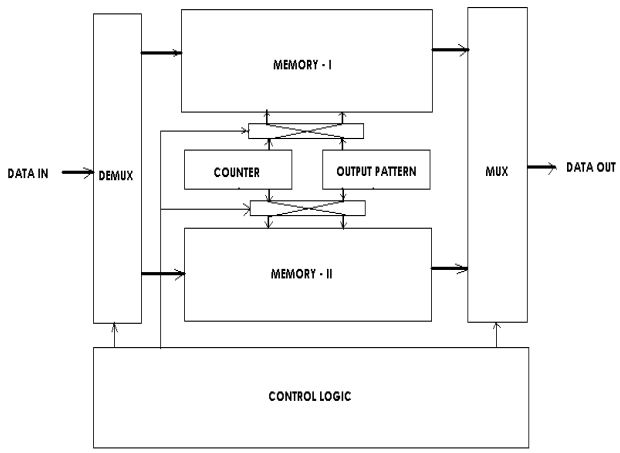

Fig. 5 Bit Interleaving Block Diagram

2.1.3 QPSK Constellation Mapping:

2 bits from the interleaver are converted into 4 bits as shown in the Table 1. The 2 bit input is converted into 4 bit complex number. The first 2 bits represent real part and the last 2 bits represent imaginary part.

Table .1 QPSK Mapping

Input Bits	Output Bits
00	1111
01	1101
10	0111
11	0101

2.1.4 FFT:

To reduce the hardware complexity, modified Radix-2^4 SDF pipelined OFDM module is used. The block diagram of the single data-path 128-point Radix-2^4SDF FFT/IFFT processor is shown in Fig. 6 [10]. This architecture consists of a memory block, butterfly units (BF1, BF2), programmable complex multipliers and CSD complex constant multipliers, register files and some multiplexers. Hardware complexity is significantly reduced by usage of constant coefficient canonical signed digit (CSD) multipliers.

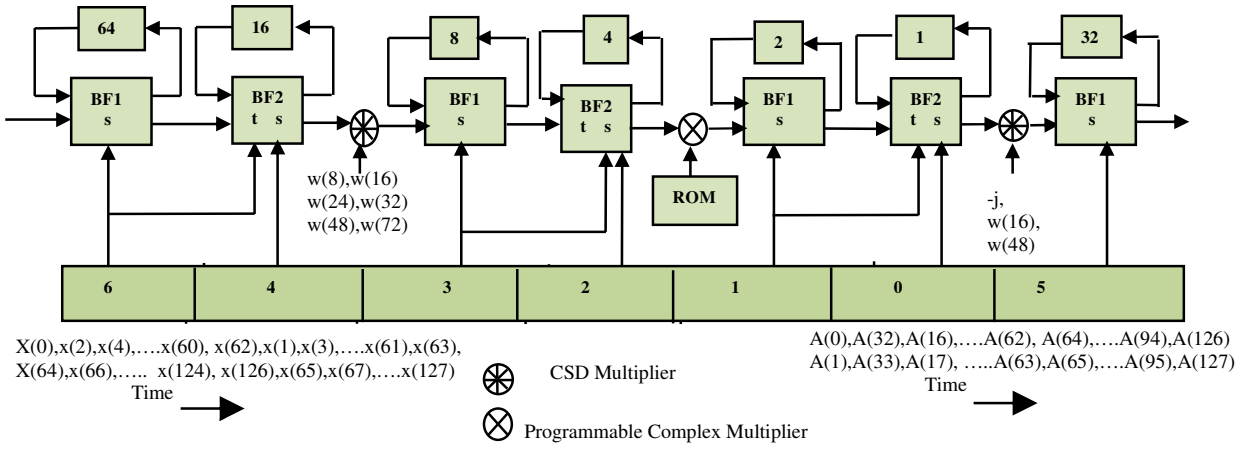

Fig. 6 Modified Radix-2^4 SDF FFT/IFFT processor

3. ASYNCHRONOUS PIPELINING SYSTEM

In synchronous systems, the subsystems change from one state to another state depending on a global clock signal. When the system is tend to become bigger and bigger, the problem of clock skew is becoming a bottleneck for many system designers. And also in synchronous systems, many gates switch unnecessarily just because they are connected to the clock, and not because they have to process new inputs [11]. Due to this, the synchronous systems consume more power than necessary. Therefore the design of clock-free or asynchronous systems has thus become attractive for digital system designers during the past few years [11].

An asynchronous system is one in which there is no global synchronization within the system; subsystems within the system are only synchronized locally by the communication protocols between them.

3.1 ADVANTAGES OF ASYNCHRONOUS SYSTEMS

- No Clock Skew and Clock Distribution
- Less Emission of Electromagnetic Noise
- High Operating Speed
- Better Composability and Modularity
- Robustness towards variations in
- Supply Voltage
- Temperature
- Fabrication Process Parameters
- Low Power Consumption

In asynchronous systems, a subsystem can be replaced by another subsystem with the same functionality but different performance with ease. But in synchronous systems this is not an easy task as the clock period has to be recomputed [11].

3.2 BUNDLED-DATA PROTOCOL

The bundled-data protocol uses a single request (acknowledge) wire and a set of data wires (hence the name bundle) as shown in Fig.7 [12]. The request wire is used to inform the receiver about the validity of the data on the data bundle. This

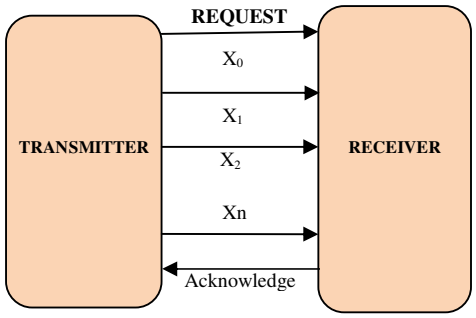

Fig.7 Bundled-data protocol

inherently places a constraint on the request wire, known as the bundling constraint. According to this constraint, the request wire must be asserted only after the bundled data is valid at the receiver end.

3.3 FOUR-PHASE SIGNALING

The 4-phase protocol is shown in Fig.9. The actions of 4-phase protocol are 1) the sender issues data and sets request high, 2) the receiver absorbs the data and sets acknowledge high, 3)the sender responds by taking request low, and 4) the receiver acknowledges this by taking acknowledge low. At this point the sender may initiate the next communication cycle.

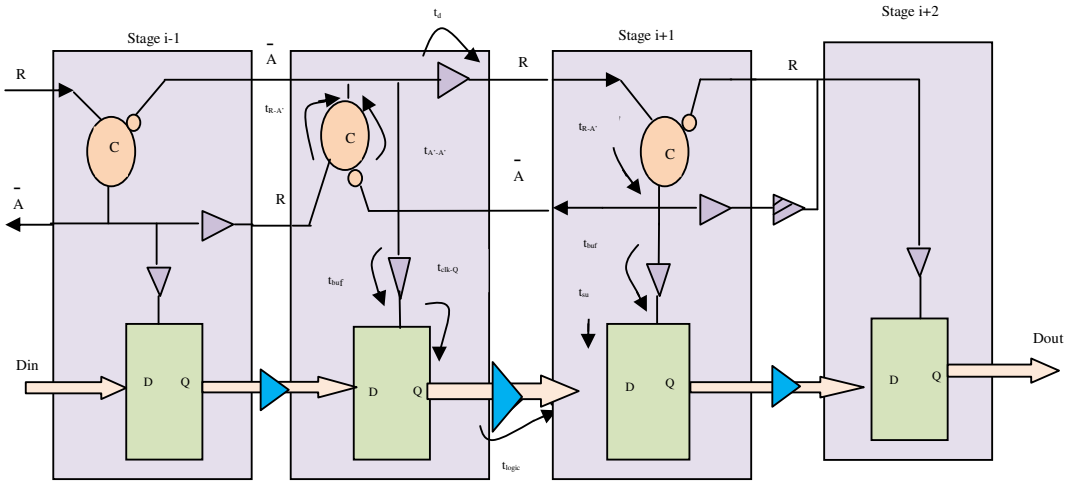

Fig. 8 Four-phase bundled-data Micropipeline

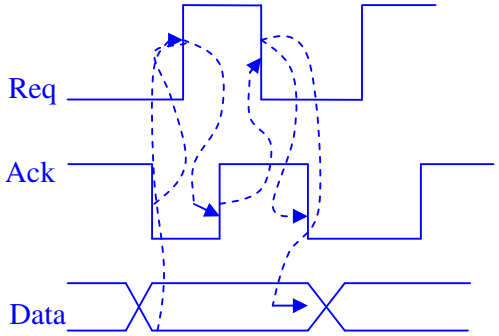

Fig.9 Four-Phase Signaling

3.4 FOUR-PHASE MICROPIPELINE

The micropipeline for four-phase bundled-data protocol is shown in Fig. 8 [12]. When data is ready, request pulse is generated. This request pulse is used to generate the enable signal to latch the data which is processed by the combinational block. This enable signal is also sent as request pulse for the next stage after a delay corresponding to the delay of the combinational block. The enable signal generated by the second block is used to latch the output of the combinational block and also sent as the acknowledgement signal to the previous stage in order to get the next data. The new input data is latched only after it is available and any previously stored data has been consumed by a subsequent stage, thereby ensuring that no data is lost. This event-Anding can be implemented using a Muller C-element.

3.5 MULLER C-ELEMENT

Muller C-element is a state-holding element like an asynchronous set-reset latch. It is indeed a fundamental component that is extensively used in asynchronous circuits [13]. A Muller C-Element and its truth table are shown in Fig.10 and Table 2 respectively. When both inputs are '0' the output is set to '0', and when both inputs are '1' the output is set to '1'. For other combinations the output does not change.

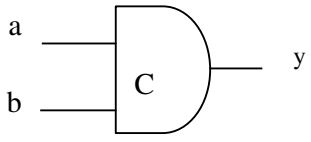

Fig.10 Muller C-Element

Table 2. Truth Table

a	b	y
0	0	0
0	1	No Change
1	0	No Change
1	1	1

4. PROPOSED ASYNCHRONOUS MB-OFDM UWB TRANSMITTER

To meet the high speed and low power requirements of MB-OFDM UWB systems, in this paper, transmitter is proposed. The block diagram of the proposed asynchronous pipelined MB-OFDM UWB system is shown in Fig. 11. The MB- OFDM UWB transmitter backend is divided into 3 stages and these are pipelined asynchronously. The first stage contains scrambler, convolutional encoder and 3bits to 15 bits converter. A REQ1 pulse is given to the first stage, whenever data is ready at the input,. An En1 signal is used as the enable signal for the first stage of the blocks. Separate pipelining is not required for these blocks because registers are involved in the first stage blocks.
MB-OFDM UWB transmitter with 200Mbps data rate, 125MHz REQ1 pulse (to communicate with the 125 Mbps input data rate) is given to the C-element which generates En1 signal.
The second stage contains puncturer and interleaver blocks. As the second stage has to operate with a speed of 5 times less than the En1 signal, a mod 5 counter with En1 as the clk and another C-element is used to generate En2 signal. This En2 signal is used as the enable signal for puncturer and interleaver blocks. Since interleaver has to operate with different reading and writing speeds, En2 signal is used as the write enable (Wr En) for writing into the interleaver and En3 generated by an external REQ2 pulse and a C-element is used as the read enable (Rd. en) for reading from the interleaver. En3 is generated by using C-element and a 528MHz REQ2pulse (to communicate with the outside world).

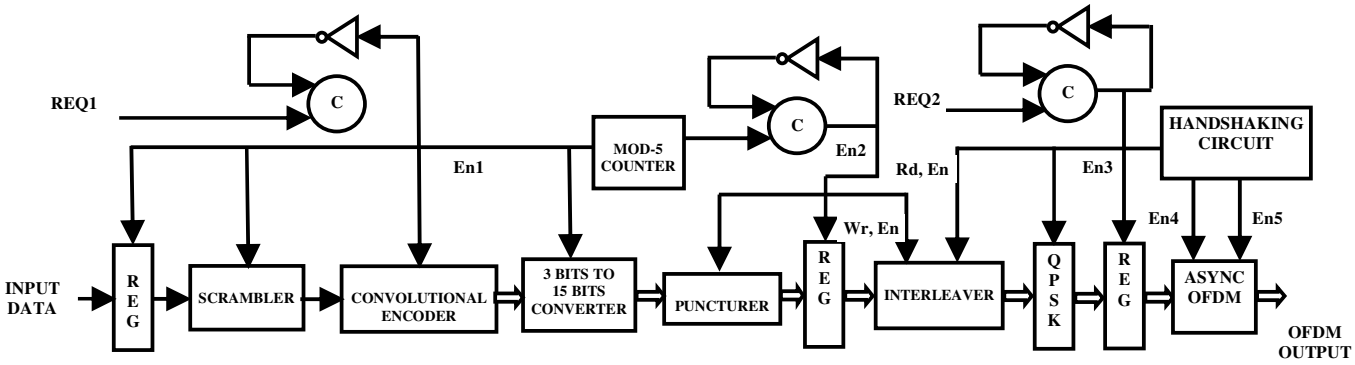

Fig. 11 Asynchronous Pipelined MB-OFDM UWB Transmitter

5. IMPLEMENTATION RESULTS

The proposed asynchronous pipelined MB-OFDM UWB transmitter is implemented on ALTERA STRATIX II EP2S60F1020C4 FPGA and the results are tabulated in Table 3. The table shows that asynchronous pipelined MB-OFDM UWB system is operated with the frequency of 350MHz on STRATIX II. The FPGA based asynchronous pipelined MB-OFDM UWB transmitter digital backend is of first kind to the best of our knowledge. Hence it is difficult to compare the results with the previous implementations. But, this system definitely comprises the advantages of asynchronous pipelined system and the advantages of FPGA.

Table.3 Implementation Results

FPGA	ALTERA
Family	STRATIX II
Device	EP2S60F1020C4
ALUTs	7883
Registers	7797
Pins	276
ALMs	4847
Total Memory Bits	13,296
DSP block 9 bits elements	6
Static Power Dissipation	635.25mW
Dynamic Power Dissipation	364.34mW
I/O Power Dissipation	962.98mW
Total Power Dissipation	1962.57mW
No. of transitions	81,25,585
Operating frequency	350MHz

6. CONCLUSION

The proposed FPGA based asynchronous pipelined MB-OFDM UWB transmitter digital backend is implemented successfully on ALTERA STRATIX II EP2S60F1020C4 FPGA with the operating frequency of 350MHz. In our previous work, we have implemented synchronous pipelined MB-OFDM UWB on STRATIX II device with the operating frequency of 350MHz and on STRATIX III device with the operating frequency of 528MHz [10]. So, asynchronous pipelined MB-OFDM UWB can be made to work on STRATIX III with the operating frequency of 528MHz in compliance to the ECMA-368 standard. The asynchronous pipelined OFDM module which is a 128 point IFFT processor is implemented using four-phase bundled-data protocol in an efficient way to give maximum frequency with minimum area by using Altera LPM (Library Parameterized Modules) modules.x

The high throughput rate of the OFDM can meet the UWB specifications on STRATIX III device without the use of parallel processing. Furthermore, the hardware costs of memory and complex multiplier are saved by adopting delay feedback and data scheduling approach on asynchronous OFDM. In addition, the number of complex multiplications is reduced effectively by using a higher radix algorithm and using CSD complex multipliers. The asynchronous Interleaver is also carefully designed using two different RAM banks which are working in tandem with different write and read addresses and enables to provide optimum results.

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