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Retraction

Retracted: DESIGN AND SOFTWARE CHARACTERIZATION OF FINFET BASED FULL ADDERS

ICTACT Journal on Microelectronics Retraction Statement:

ICTACT Journal on Microelectronics hereby retracts the article titled "Design and Software Characterization of FinFET based Full Adders", originally published in ICTACT Journal on Microelectronics, Volume 4, Issue 4, pp. 676-680, January 2019, DOI: 10.21917/ijme.2019.0117. This retraction is being issued after careful consideration and investigation by the editorial board.

After thorough examination, it has come to our attention that the same article has been published in multiple journals simultaneously, which is a violation of ethical publishing standards. The duplicate publication undermines the integrity of the scientific literature and violates the policies of ICTACT Journal on Microelectronics.

The editorial board has communicated with the authors regarding this matter. The authors have responded to correspondence regarding this retraction.

In light of the breach of publishing ethics, the editorial board of ICTACT Journal on Microelectronics has decided to retract the article. The decision to retract has been made in accordance with journal publication Ethics.

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DESIGN AND SOFTWARE CHARACTERIZATION OF FINFET BASED FULL ADDERS

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Abstract

Adder is the most important arithmetic block that is used in all processors. Most of the logical circuits till today were designed using Metal Oxide Semiconductor Field Effect Transistors (MOSFET's). In order to reduce chip area, leakage power and to increase switching speed, MOSFET's were continuously scaled down. Further scaling below 45nm, MOSFET's suffers from Short Channel Effects (SCE's) which leads to degraded performance of the device. Here the Performance of 28T and 16T MOSFET based 1-bit full adder cell is characterized and compared with FinFET based 28T and 16T 1-bit full adders at various technology nodes using HSPICE software. Results show that FinFET based full adder design gives better performance in terms of speed, power and reliability compared to MOSFET based full adder designs. Hence FinFET are promising candidates and better replacement for MOSFET.

Keywords:

Adder, MOSFET, FinFET, CMOS, Pass Transistor Logic

1. INTRODUCTION

Today there is a huge demand for portable applications such as laptops, iPhones etc. with limited amount of power availability, requiring minimum area and high switching speed circuitry [1]. Therefore, circuits which provide low power consumption and high switching speed becomes the major candidates for design of microprocessor and other subsystems [2]. Addition is a basic arithmetic operation and is used in most of the VLSI subsystems like application specific DSP architectures and microprocessors [9]. Therefore 1-bit Full Adder cell is the most important and basic block of arithmetic logic unit in digital systems.

In low power VLSI systems, Metal Oxide Semiconductor field effect Transistors (MOSFET's) are the basic transistors used in most of the digital circuits. Continuous scaling of MOSFET's has resulted in better performance of the device parameters such size, delay and power. Further scaling of MOSFETs below 45nm node technology leads to short channel effects (SCE's), which modifies the device characteristics. The major SCE's includes

- Drain Induced Barrier Lowering.
- Velocity saturation.
- Hot electrons effect.
- Channel length modulation.
- Oxide breakdown.

To avoid these effects as well as to improve the switching speed ad to reduce the power requirements, MOSFET's were replaced by FINFET's in design circuitry [5] [6]. FINFET's are multiple gate devices. These multiple gates provide better control over the channel and hence reduce the short channel effects [6]. FINFET based adder in general shows an average of 94% drop in delay, 97% decrease in power dissipation over the conventional MOSFETs [7] [8].

2. FINFET TECHNOLOGY

FINFET known as Fin Field Effect Transistors non-planar or 3D transistor used to design modern processor. The main characteristics of FINFET is that it has a conducting channel wrapped by a thin silicon "fin" and hence the name FINFET. The thickness of the fin determines the effective channel length of the device. This wrap around gate structure provides better electrical control over the channel and this helps in reducing the leakage current and overcoming other short channel effects. This fin allows multiple gates to operate on single transistor. The multiple gates of FINFET extend Moore's Law which allows the semiconductor manufacturers to create microprocessor subsystem and memory modules that provides faster performances, less energy consumption and reduction in space complexity.

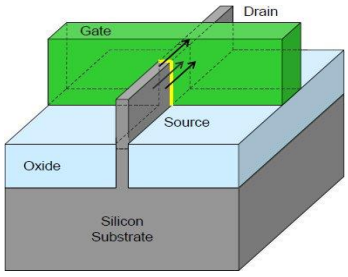

Fig.1. FinFET Structure [7]

The Fig.1 shows a FinFET structure. It has four terminals and it consists of source, drain and channel wrapped by multiple gates. Here we consider two gates FinFET structure namely front gate and back gate. FinFET can substitute in place of MOSFET by merely shorting the front and back gates together during device fabrication and allow FinFET work as single gate device.

3. 1-BIT FULL ADDER CELL

The operation of 1-bit full adder cell includes three inputs *A*, *B*, C_{in} using which outputs sum and carry are calculated.

$$Sum = A \oplus B \oplus C_{in}$$

$$C_{out} = A \cdot B + C_{in}\,(A \oplus B)$$

In this paper, a 1-bit full adder is implemented using both CMOS and FINFET technology. The full adder circuitry has been designed using different logic styles:

- Conventional CMOS logic style.
- Complementary pass transistor logic and transmission gates logic.

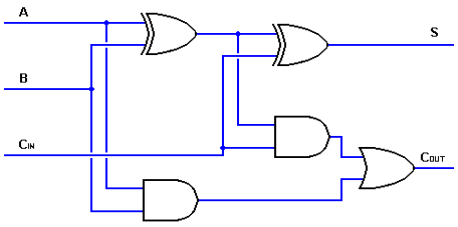

Fig.2. Basic Adder Circuit [9] [10]

Table.1. Full Adder Truth Table [9] [10]

A	*B*	C_{in}	*Sum*	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4. MOSFET BASED FULL ADDER

The device parameters considered are based on predictive Technology Model (PTM) for developing a spice model and then simulating using HSPICE tool. The parameters are considered with respect to PTM as shown in the Table.2.

Table.2. Design considerations

Parameter	90nm MOSFET	45nm MOSFET
Gate Length (L_g)	90nm	45nm
Supply Voltage	1.5V	1.2V

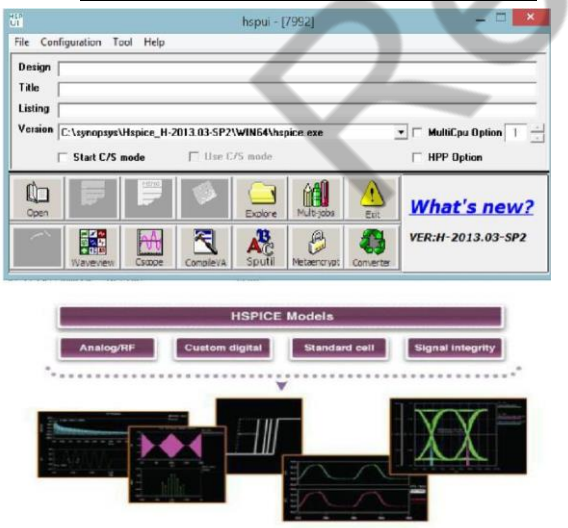

Fig.3. Hspice user interface and integration

The Fig.3 shows HSPICE user interface and integration, the netlist written for a particular circuit model is characterized via the Hspice user interface and the software is powerfully integrated to find the errors and produce the output results in accurate manner.

4.1 28T CONVENTIONAL CMOS FULL ADDER

This CMOS full adder consists of both PMOS and NMOS in the form of pull-up and pull- down network. The Fig.4 shows the schematic diagram of 28T conventional CMOS full adder cell.

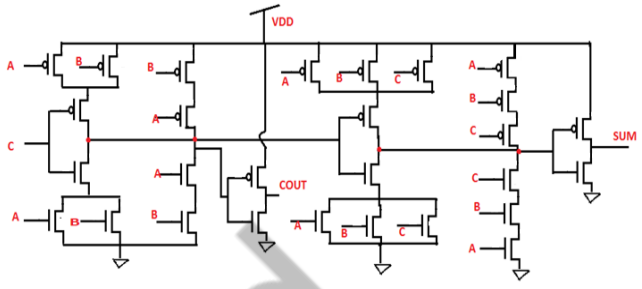

Fig.4. 28T conventional CMOS full adder

Output waveform of 28T full adder cell is as shown in Fig.5.

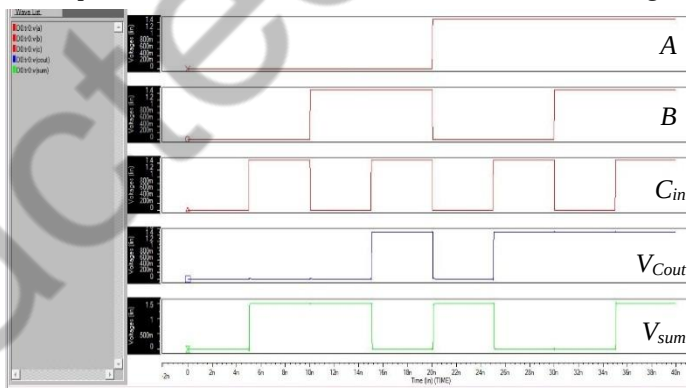

Fig.5. Output waveform at 90nm

In Fig.5, *A*, *B* and C_{in} are inputs to the adder circuit and V_{sum} and C_{out} are the sum and carry outputs respectively. The switching delay in generating sum and carry out along with power are calculated and tabulated in the Table.3. Same procedure is applied to all the node technologies evaluated using MOSFET and FinFET devices.

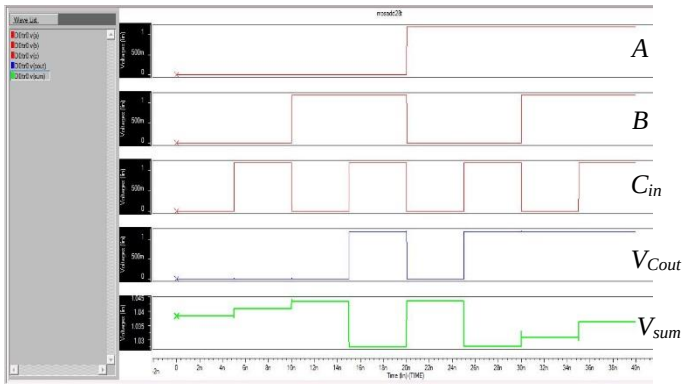

Fig.6. Output waveform at 45nm

Table.3. Results of 28T full adder cell

Node	Average Power (W)	Maximum Power (W)	Sum Delay (s)	Carry Delay (s)
250nm	23.6828µ	1.7951m	211.7751p	136.2695p
180nm	6.5605µ	557.1307µ	176.1207p	112.5616p
90nm	1.1997µ	158.9428µ	66.3052p	45.6138p
45nm	27.3311m	27.4380m	Failed	Failed

From the Table.3, it is clear that performance of MOSFET based full adder in terms of the power and delay values are obtained and it can be concluded that there is an increase in the power and delay values of MOSFET based Full Adder at 45nm node and below due to short channel effect faced by MOSFET devices.

4.2 16T MOSFET FULL ADDER

In order to reduce the number of transistors and to obtain optimum results, 16T full adder is designed and simulated using complementary pass transistors and transmission gates. The simulation is done in HSPICE tool. The Fig.7 shows the design of 16T MOSFET full adder cell.

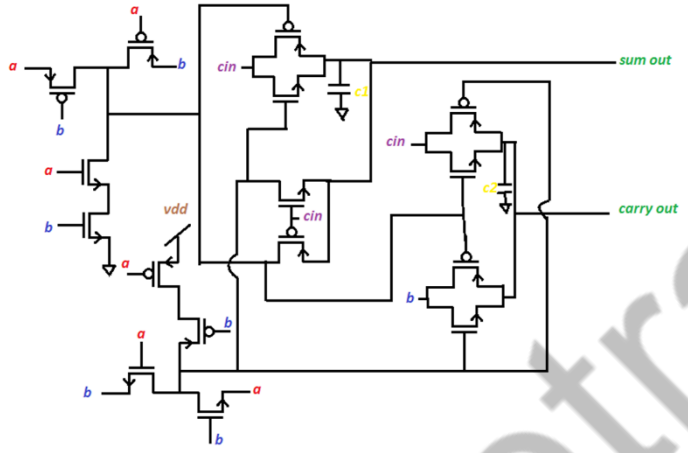

Fig.7. 16T MOSFET full adder cell

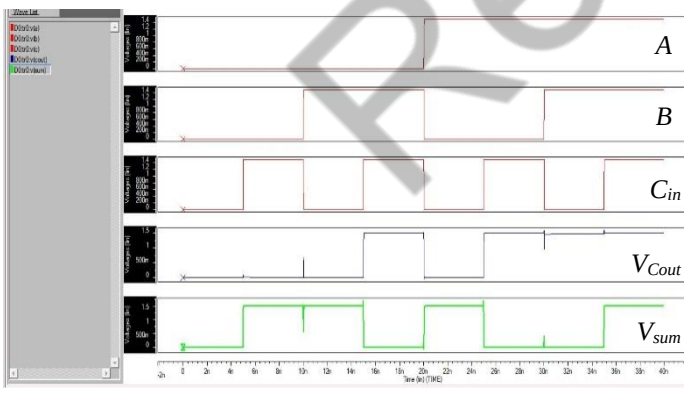

Fig.8. Output waveform at 90nm

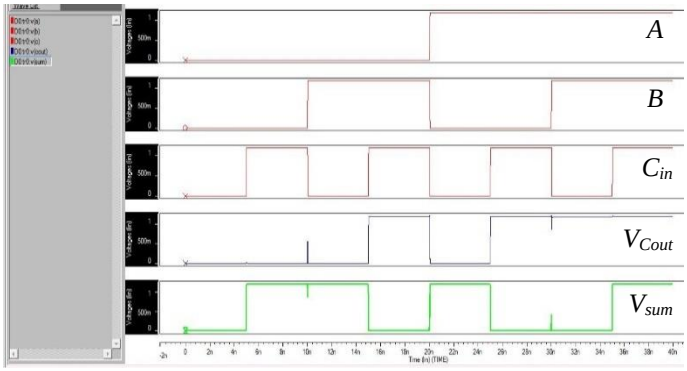

Fig.9. Output waveform at 45nm

Table.4. Results of 16T full adder cell

Node	Average Power (W)	Maximum Power (W)	Sum delay (s)	Carry delay (s)
250nm	17.0502µ	1.9958m	23.6453p	3.6746p
180nm	3.6266µ	548.9434µ	21.5174p	3.2325p
90nm	2.1733µ	195.1429µ	15.0140p	2.6017p
45nm	1.8895µ	90.9523µ	3.5366p	1.2495p

The Table.4 contains the power and delay values for MOSFET based full adder. It is observed that there is an increase in the power and delay values of MOSFET based Full Adder at lower nodes due to short channel effect faced by MOSFET devices.

5. FINFET BASED FULL ADDER

To overcome the scaling issue faced by MOSFET, full adder cell is designed using FINFET. The FinFET allows further scaling up to 14nm.

Table.5. Design considerations

Parameter	22nm FinFET	14nm FinFET
Gate length (L_g)	22nm	14nm
Supply voltage	0.9V	0.8V
Fin height (h_{fin})	23nm	30nm
Fin width (t_{fin})	10nm	10nm

5.1 28T FINFET FULL ADDER

This full adder cell consists of both nFET and pFET to replace the complementary CMOS logic. The Fig.10 gives the schematic diagram of 28T FinFET full adder cell.

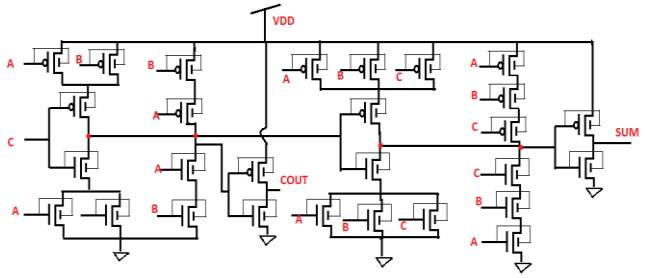

Fig.10. 28T FinFET full adder cell

The output waveforms of 28T full adder cell is as shown in Fig.11 and Fig.12.

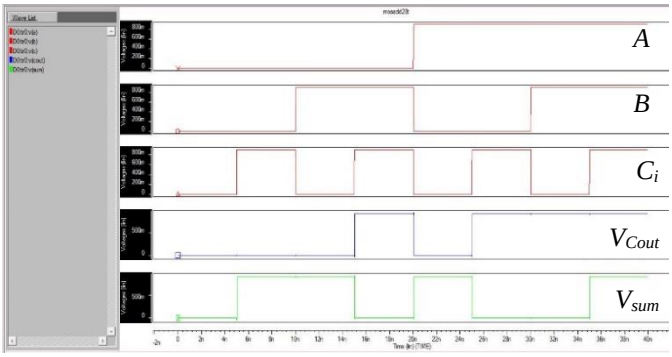

Fig.11. Output waveform at 22nm

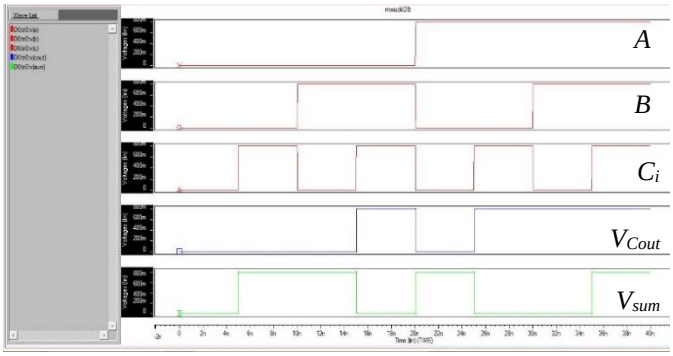

Fig.12. Output waveform at 14nm

Table.6. Results of 28T FinFET full adder cell

Node	Average Power (W)	Maximum power (W)	Sum delay (s)	Carry delay (s)
22nm	62.147n	26.768µ	25.489p	15.966p
14nm	32.242n	25.230µ	13.944p	9.7921p

From the simulated results of Table.5 contains the power and delay values for 28T FinFET based Full Adder it can concluded that FinFET is a better replacement for MOSFET devices.

5.2 16T FINFET FULL ADDER

Similar to Fig.13 with 28T FinFET full adder cell, a schematic diagram of 16T FinFET based full adder cell can be drawn and characterized at 22nm and 14nm technology nodes as observed in following waveforms. The output waveforms of 16T full adder cell are as shown in Fig.13 and Fig.14.

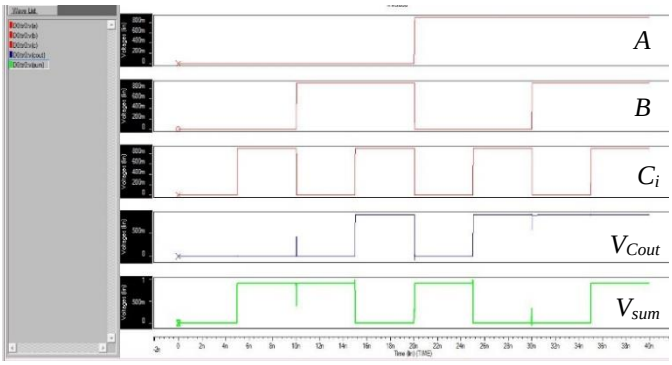

Fig.13. Output waveform at 22nm

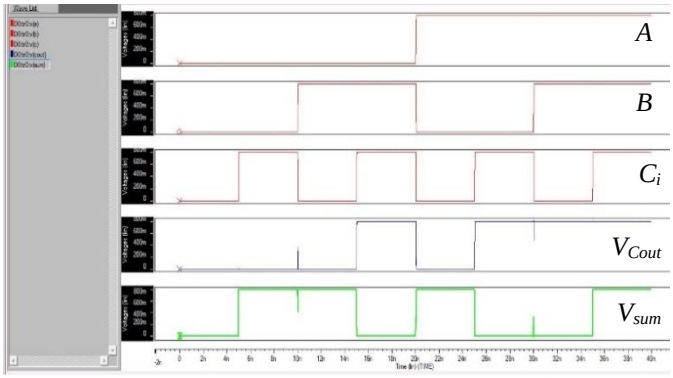

Fig.14. Output waveform at 14nm

Table.7. Results of 16T FinFET full adder cell

Node	Average Power (W)	Maximum Power (W)	Sum delay (s)	Carry delay (s)
22nm	35.012n	20.056µ	10.503p	2.089p
14nm	19.721n	10.426µ	8.942p	2.069p

6. RESULTS AND DISCUSSIONS

The spice models of MOSFET based full adders are created for 28T and 16T at 90nm and 45nm and are simulated using HSPICE. The simulation waveforms are viewed using Avanwaves. The comparison of the results between 28T and 16T MOSFET based full adder cell is as shown in Table.8.

Table.8. Comparison of MOSFET based full adder at 90nm

No. of transistors	Average power (W)	Maximum Power	Sum delay	Carry delay (s)
28T	1.199µ	158.942µ	63.382p	42.161p
16T	1.185µ	93.037µ	13.846p	2.439p

Table.9. Comparison of MOSFET based full adder at 45nm

No. of transistors	Average power	Maximum Power	Sum delay(s)	Carry delay(s)
28T	29.321m	29.939m	Failed	30.127p
16T	1.816µ	108.223µ	3.536p	1.428p

From the comparisons made, it is analysed that (1) as number of transistors decreases, the power dissipation has decreased. (2) Scaling of MOSFET from 90nm to 45nm has led to increase in power dissipation. Hence further scaling down of MOSFET leads to degraded output and increase in leakage power.

The spice models based on PTM files are referred from BSIM-IMG for characterization of device and FinFET based full adders are built for 28T and 16T at 22nm and 14nm and are simulated using HSPICE. The comparison of the results between 28T and 16T FinFET based full adder cell at 22nm and 14nm nodes is as shown in Table.10.

Table.10. Comparison of FinFET based full adder at 22nm

No. of transistors	Average power (W)	Maximum Power (W)	Sum delay (s)	Carry delay (s)
28T	62.147n	26.768µ	25.489p	15.966p
16T	35.012n	20.056µ	10.503p	2.089p

Table.11. Comparison of FinFET based full adder at 14nm

No. of transistors	Average power (W)	Maximum Power (W)	Sum delay (s)	Carry delay (s)
28T	32.242n	25.230µ	13.944p	9.7921p
16T	19.721n	10.426µ	8.942p	2.069p

From the comparisons of FinFET based full adder cell, we can analyse that FinFET has overcome the scaling issues of MOSFET as illustrated above at 22nm and 14nm.

7. CONCLUSIONS

The MOSFET and FinFET based full adder cell for 28T and 16T at different nodes are characterized using software mainly in terms of Power dissipation and delay. The obtained results for the FinFET full adder spice models used here shows a promising solution for MOSFETs scaling issues. The power dissipation in 28T FinFET based adder at 14nm is reduced to 32nW from 62nW at 22nm adder, similarly delay get reduced from 25ps to 13.9ps when node size is reduced from 22nm to 14nm node. Likewise, the results for the power and delays values for sum and carry operation are for 16T FinFET based full adders. And from the result table 6.3 and 6.4 it can be concluded that FinFET based full adder cell is reliable at lower technology nodes and the tolerant capacity is better at the nanometer regime. The power dissipation of the FinFET based device has decreased significantly at lower technology nodes. The speeds of the adder circuits are increased terms of the sum and carry delay operation. Thus FinFET based circuits are promising candidates for the future Digital systems.

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