DOI: 10.21917/ijme.2015.0012

DESIGN AND IMPLEMENTATION OF LOW-NOISE AMPLIFIER FOR ULTRA-WIDEBAND RECEIVER IN 180nm CMOS TECHNOLOGY

Neelam Gautam[1], Manish Kumar[2] and Abhay Chaturvedi[3]
Department of Electronics and Communications, GLA University Mathura, India
E-mail: [1]neelamgautam123@gmail.com, [2]manish.kumar@gla.ac.in, [3]abhay.chaturvedi@gla.ac.in

Abstract

This paper presents an ultra-wideband (UWB) low noise amplifier (LNA) using two stage cascading topology to obtain high gain. Inductive degeneration and peaking inductor techniques are used to obtain wideband matching and flatness of gain. The proposed UWB LNA is implemented by using 180nm based CMOS TSMC technology using Advanced Design System (ADS) software.LNA achieves maximum gain of 15.5dB, minimum noise figure of 2.88dB, -6dBm of IIP3 and wideband input matching in the UWB frequency range of 3.1GHz to 10.6GHz. The proposed LNA provides group delay of 60ps and isolation of less than 25dB under the 1.8V DC power supply.

Keywords:
CMOS, UWB, Gain, Noise Figure, Isolation

1. INTRODUCTION

In the year 2002, the UWB radio technology (3.1GHz to 10.6GHz) was approved by Federal Communication Commission (FCC) in USA, for short range wireless applications.

Low noise amplifiers are significant block in UWB receivers which receive weak signal from the UWB frequency and amplify this signal with low noise figure and high gain. LNA in wireless receiver is responsible for high and flat gain, low power consumption, low noise figure, good input impedance matching and linearity. LNA can be broadly divided into three parts: input matching network, amplifier network and output matching network. Filters are used in input matching part to provide low input reflection coefficient (S11) for wideband performance and low noise characteristics. The output matching part of LNA is responsible for decreasing output reflection coefficient (S22). Different kinds of techniques exist for amplifier network of CMOS LNA to provide high and flat gain, low power consumption and low noise figure.

The third order Chebyshev filter topology is used for wideband input matching. Chebyshev filter requires a number of reactive elements in input stage of LNA, which requires large on chip area and generates large amount of thermal noise [2]. To improve the performance of wideband input matching network, RC shunt-shunt feedback topology is used [3], [4]. The distributed topology of LNA provides wideband input matching, large power consumption, large on chip area and high noise figure [5]. To compensate the effect of high power consumption, the current reuse topology is used in LNA design which requires no external biasing. Current reuse topology is widely used in cascoding topology to eliminate the miller effect [8] as well as to provide high and flat gain, low power consumption and low noise figure, [1], [6].

This paper presents a performance of LNA using 0.18μm CMOS technology for UWB receiver. The analyses and designing of proposed circuit is shown in section 2 and section 3 shows the simulation result of gain, noise figure, reflection coefficient, isolation and group delay. Conclusion of LNA is given by section 4.

2. CIRCUIT DESIGNING

Inductive source degeneration topology is used in proposed circuit for wide-bandwidth input matching and low power consumption shown in Fig.1.

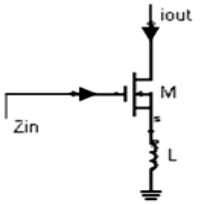

Fig.1. Inductive source degeneration [7]

The input impedance of the circuit (Z_{in}) and inductor L is selected to obtain desired input resistance (R_{in}) of 50Ω in Fig.1. The C_{gs} and g_m represents gate to source capacitance and trans-conductance of the transistor *M*.

$$Z_{in} = sL + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L \tag{1}$$

The current reuse cascoding topology and two stage cascading topology is used in proposed LNA design as shown in Fig.2.

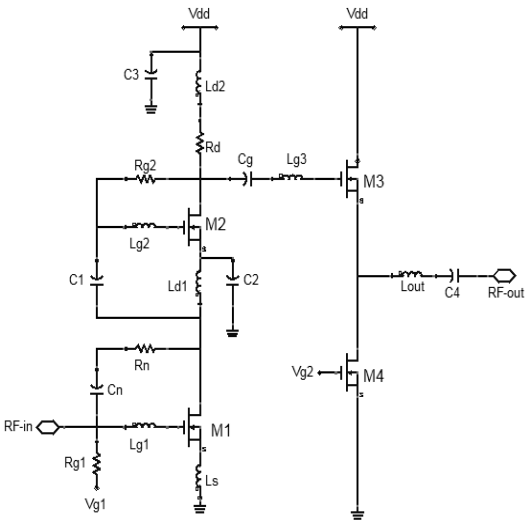

Fig.2. Proposed CMOS LNA circuit diagram

The cascaded transistor M_1 and M_3 improve the isolation and reduce the miller capacitive effect. It is difficult to obtain a high gain in a very large bandwidth like 3.1GHz to 10.6GHz of UWB range, therefore cascading topology is used at the input and output stages to enhance the gain in UWB range. The inter stage peaking inductor L_{g3} provide the input impedance matching for the output stage (M_3) and output impedance matching for the input stage (M_2), which provides flatness in gain with extended bandwidth for impedance matching. The output stage of LNA consists of common source transistors M_3 and M_4 with cascode topology to obtain the maximum gain. The combination of inductor (L_{out}) and capacitor (C_4) gives output impedance matching for the output stage of CMOS LNA. The DC gain (A_0) of cascoded transistor M_1 and M_2 is given below.

Cascade input stage (M_1, M_2) and output stage (M_3, M_4) with peaking inductor L_{g3} in series with shunt feedback of L_{g2} are used in proposed circuit. The Input and output stages of amplifier circuit work simultaneously by the use of cascoding topology. Common source and common gate transistor M_1 and M_2 are connected in form of cascode topology. A degeneration inductor L_s, connected to the transistor M_1 shows a negative feedback effect. It provides a noise impedance matching and stability effect. The capacitor C_1 block the DC current of transistor M_1 and extra DC biasing current is not required to drive the transistor M_2. The inductor L_{g1} and L_{g2} offer the impedance matching for the transistor M_1 and M_2 which is important to obtain the wide-bandwidth response. Inductive load (L_{d1}, L_{d2}) and current reuse of transistor M_2 provide low power consumption. Inductive load and L_{g1}, L_{g2} with gate to source capacitance of transistor M_1, M_2 works as resonant circuit for the transistor M_1 which provide better impedance matching and enhanced -3dB bandwidth to cover-up the entire 3.1 to 10.6GHz UWB frequency range. The cascaded transistor M_1 and M_3 improve the isolation and reduce the miller capacitor effect. It is difficult to obtain a high frequency in a very large bandwidth like 3.1GHz to 10.6GHz of UWB range, therefore cascading topology is used at input and output stage to enhance the gain in UWB range. The inter stage peaking inductor L_{g3} provide the input impedance matching for the output stage (M_3) and output impedance matching for the input stage (M_2), which provides flatness in gain with extended bandwidth for impedance matching. The output stage of LNA consists of common source transistors M_3 and M_4 with cascode topology to obtain the maximum gain. The combination of inductor (L_{out}) and capacitor (C_4) gives output impedance matching for the output stage of CMOS LNA. The DC gain (A_0) of cascoded transistor M_1 and M_2 is given below.

$$A_0 = \frac{-R_d}{\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right)} \tag{2}$$

where, g_{m1} and g_{m2} represents the trans-conductance of transistor M_1 and M_2. Gain with resistive feedback is given by Eq.(3).

$$A_v = \frac{-\left(R_d \| R_{g2} \| R_n\right)}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \tag{3}$$

Input impedance (Z_{in}) of circuit is calculated using input equivalent circuit as shown in Fig.3.

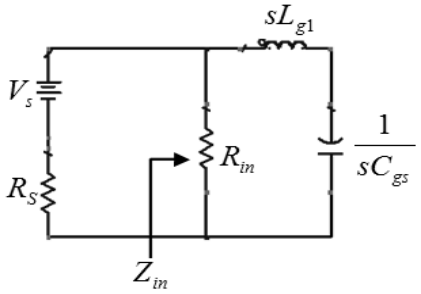

Fig.3. Input equivalent circuit

$$Z_{in} = R_{in} \left\| \left(sL_{g1} + \frac{1}{sC_{gs}} \right) \right. \tag{4}$$

where, C_{gs}, R_s and R_{in} are gate to source capacitance of transistor, source resistance and input resistance respectively. The input resistance, calculated using the miller's theorem is given by Eq.(5).

$$R_{in} = \frac{\left(\frac{R_d + R_{g2}}{1 - A_{02}} + R_n \right)}{1 - A_{01}} \tag{5}$$

A_{01}, A_{02} represent the open circuit gain of M_1, M_2. When the value of (sL_{g1}+sC_{gs}) satisfies the resonance condition then Z_{in} = R_{in} and R_{in} = R_s = 50Ω, thus input matching is obtain. Bandwidth of the circuit in term of its quality factor (Q_{in}) is given by ω_0/Q_{in}, where Q_{in} is given by Eq.(6).

$$Q_{in} = \frac{\omega_0 L_{g1}}{R_{in} + R_s} \tag{6}$$

Therefore by decreasing the value of Q_{in} input bandwidth can be increase [9]. The expression of noise factor, given Su Limei [9] can be used to obtain the noise factor expression for proposed LNA as shown by Eq.(7).

$$F > 1 + \frac{R_s}{R_{g2} \| R_n} \left[1 + \frac{1}{g_{m1} R_s} \right]^2 + \frac{\gamma}{g_{m1} R_s} \tag{7}$$

where, γ is a constant and the value of γ = 2 for short – channel MOS-FETs [10]. Combination of $R_{g2} \| R_n$ is a main parameter to obtain tradeoff between impedance matching, noise factor and gain.

The noise factor is optimized by choosing the width of transistor M_1 = 168μm. Optimized value of the components are L_{g1} = 0.897pH, L_{g2} = 1.29nH, L_s = 0.236nH, R_{g1} = 2.27kΩ and optimized value of shunt feedback RC components are R_n = 684Ω, C_n= 951fF. The parasitic capacitances are reduced by choosing cascode device as small as possible. The value of the transistor M_2 of 98.8μm is selected by optimizing noise improvement. All the transistors M_1, M_2, M_3 and M_4 are taken as minimum length devices (0.18μm). The value of inductive load are L_{d1} = 8.23nH, L_{d2}= 1.01nH and load resistance R_d = 27.3Ω, R_{g2} = 2.27kΩ with capacitances C_1 = 2.85pF, C_2 = 8.56pF and C_3 = 9.51pF. The width of cascade transistor M_3 and M_4 are chooses 98μm with the inductor value of L_3 = 5nH. The output matching stage component value are L_{out} = 9pH and C_4 = 951fF.

3. SIMULATION AND MEASURED RESULTS

In 0.18µm TSMC CMOS technology is used for simulation of proposed LNA. Simulated result of gain S21 is shown in Fig.4. Result shows the maximum and flat gain (S21) of 15.5dB from 3.1GHz to 6GHz frequency range.

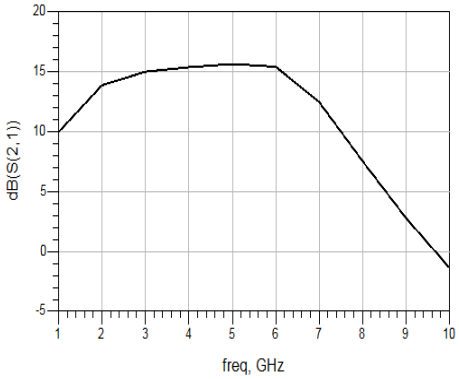

Fig.4. Result of gain S21 in dB versus frequency in GHz

The simulated result of noise figure is shown in Fig.5. The optimized noise figure is 2.88dB at 3.1GHz frequency.

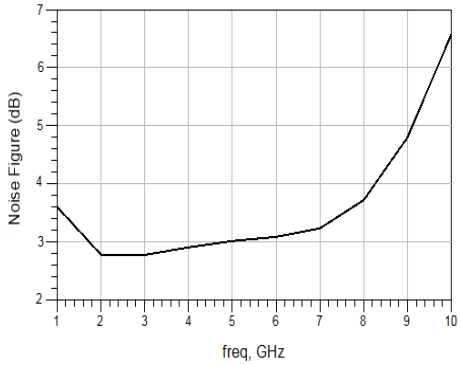

Fig.5. Result of noise figure in dB versus frequency in GHz

The simulated result of input return loss (S11) versus frequency is less than -9 dB as shown in Fig.6.

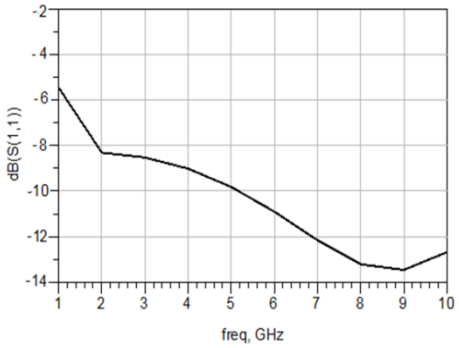

Fig.6. The result of input return loss S11 in dB vs frequency in GHz

The simulated result of output return loss (S22) versus frequency is shown in Fig.7. The output return loss decreases upto -13dB at 6GHz frequency.

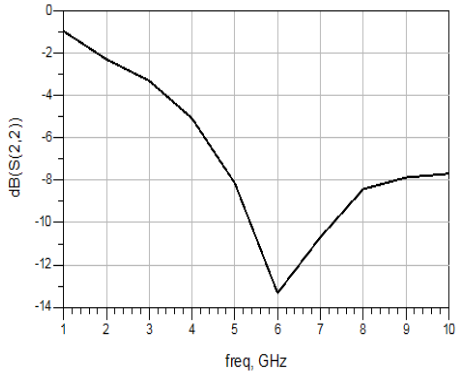

Fig.7. Result of output return loss S22 in dB vesus frequency in GHz

The simulated result of isolation (S12) is lesser than -25dB due to cascading of input stage M_2 and output stage M_3 shown in Fig.8.

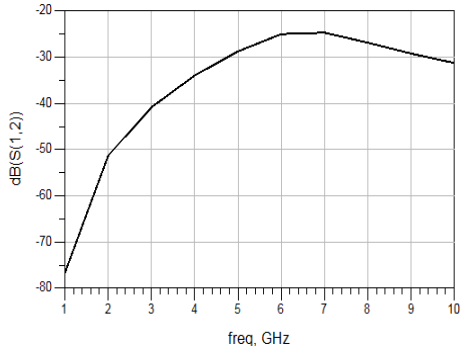

Fig.8. Result of isolation in dB versus frequency in GHz

The simulated result of group delay variation is 160ps to 60ps over the frequency range 3.1 to 10.6GHz as shown in Fig.9. The obtained IIP3 is -6dBm under the 1.8V DC supply.

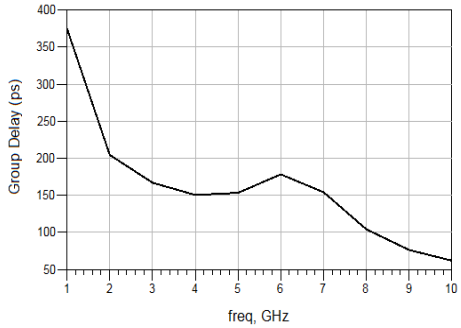

Fig.9. Result of group delay in ps versus frequency in GHz

Comparision of the simulated results of praposed LNA with other works are shown in Table.1.

Table.1. Summary of Simulated CMOS UWB LNA and Comparison

	This work 0.18µm CMOS	**[1], 0.18µm CMOS**	**[3], 90nm CMOS**	**[4], 0.18µm CMOS**
Frequency (GHz)	3.1 – 10.6	3.1–10.6	3 – 10	1.2 – 11.9

S11 (dB)	< - 9	< - 10	< - 9	< - 12
$S21_{max}$ (dB)	15.5	12.52	11	8.73
S12 (dB)	< - 25	< - 26.1	< - 40	< - 33
Group Delay (ps)	160-60	100-60	120-90	NA
NF_{min} (dB)	2.8	4	3	4.8
IIP3 (dBm)	-6	-6.5	NA	- 6.2

4. CONCLUSION

A 0.18µm TSMC CMOS ultra-wideband low noise amplifier is proposed using cascading topology to improve the gain. RC shunt-shunt feedback topology and an inductive degeneration technique are used to obtain wideband input matching to a 50Ω source resistance. A peaking inductor is used for two stage cascading topology to improve the flatness of gain with minimum noise figure. The simulated results show flat and high gain of 15.5dB, flat and minimum noise figure of 2.8dB, output return loss of -13dB, input return loss less than -9dB, and isolation less than -25dB in the UWB frequency range of 3.1GHz to 10.6GHz with 1.8V DC power supply.

ACKNOWLEDGEMENT

The authors wish to acknowledge the Keysight Technologies for providing the temporary license of Advanced Design System (ADS) Software.

REFERENCES

[1] Chia-Hsing Wu, Yo-Sheng Lin, Jen-How Lee, Chien-Chin Wang, "A 2.87±0.19dB NF 3.1~10.6GHz ultra-wideband low-noise amplifier using 0.18µm CMOS technology", *Radio and Wireless Symposium (RWS)*, pp. 227-230, 2012.

[2] Andrea Bevilacqua and Ali M. Niknejad, "An Ultra-Wideband CMOS LNA for 3.1 to 10.6 GHz Wireless Receiver", *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 12, pp. 2259-2269, 2004.

[3] G. Sapone and G. Palmisano, "A 3-10-GHz Low-Power CMOS Low- Noise Amplifier for Ultra- Wideband Communication", Microwave Theory and Techniques, IEEE Transactions on Microwave Theory and Techniques, Vol. 59, No. 3, pp. 678-686, 2011.

[4] Chih. Fan. Liao and S. I. Liu, "A Broadband Noise-Canceling CMOS LNA for 3.1–10.6-GHz UWB Receivers", *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 2, pp. 329-339, 2007.

[5] B. M. Ballweber, R. Gupta and D. J. Allstot, "A fully integrated 0.5–5.5-ghz CMOS distributed amplifier", *IEEE Journal Solid- State Circuits*, Vol. 35, No. 2, pp. 231–239, 2000.

[6] R. M. Weng, C. Y. Liu and P. C. Lin, "A Low-Power Full-Band Low- Noise Amplifier for Ultra-Wideband Receivers", *IEEE Transactions Microwave Theory and Techniques*, Vol. 58, No. 8, pp. 2077-2083, 2010.

[7] Thomas. H. Lee, "*The Design of CMOS Radio-Frequency Integrated Circuits"*, 1st Edition, New York: Cambridge University Press, 1998.

[8] G. R. Aiello and G. D. Rogerson, "Ultra-wideband wireless systems", *IEEE Microwave Magazine*, Vol. 4, No. 2, pp 36-47, 2003.

[9] Su Limei, "A 1.2 V 3.1–10.6 GHz CMOS low noise amplifier with 24 dB gain and 2.4 dB noise figure", *International Conference on Wireless Communication and Signal Processing*, pp.1-4, 2009.

[10] Behzad Razavi, "*RF Microelectronics*", 2nd Edition, New York: Prentice Hall, 1998.