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PERFORMANCE AND RELIABILITY ANALYSIS FOR VLSI CIRCUITS USING 45nm TECHNOLOGY

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Abstract

The objective of this research paper is to analyze and estimate the reliability of an inverter circuit and two CMOS gate interconnect circuit , a combination of two inverters connected with an RC model as an interconnect structure using cadence virtuoso tool utilizing at gpdk 45 nm technology. Reliability in terms of electronic circuit basically depends on hot-carrier injection, negative biasing temperature instability, positive biasing temperature instability and slightly due to the effect of time-dependent gate oxide breakdown. The inverter used in this work is without any load effect at output terminal and further a capacitive load has been applied at the output terminal. The reliability predictions are done by comparing power, delay and output voltage after a specific interval of time.

Keywords:

HCI, NBTI, PBTI, TDDB

1. INTRODUCTION

The performance and reliability is a key issue in defining the operation of the transistors and circuit over the prolong period. The bias temperature instability is one of the most challenging issues in the circuit reliability aspect. There are generally four terms which play vital role in defining the reliability of transistors, as HCI, NBTI, PBTI and TDDB. The most effecting reliability performance parameters are noise margin, leakage current, delay between input-output voltages and reliability in terms of aging. These parameters are mainly responsible for the performance and reliability degradation of any electronic circuit. All the stated parameters are illustrated below. In this research initially these performance phenomenon are implemented on transistor mainly effecting the drain current and inverted channel and then inverter with applied input voltage, I_{DP} and I_{DN} [1].

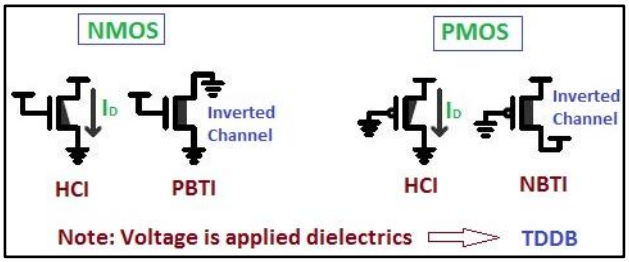

Fig.1. Schematic of NMOS & PMOS circuit

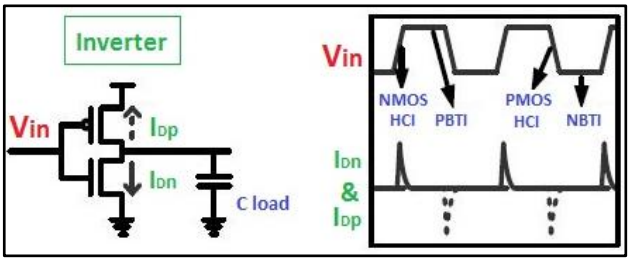

Fig.2. Schematic of an inverter circuit

HCI: It is basically one of the mechanisms that severely affect the reliability of semiconductors of solid-state devices. HCI manifests itself for an increase in the value of the threshold voltage and secondary degradation of the carrier mobility, especially for the NMOS transistors. The degradation takes place when a device is generally biased in strong inversion with a large V_{DS}. It is a strong voltage dependence factor [2].

NBTI: NBTI in PMOS transistor is recognized as the major reliability concern in advanced CMOS process technologies. This mechanism is recognized by a positive shift in the absolute value of the PMOS V_{th}. It occurs when a device is biased in strong inversion region without affecting the large V_{DS}.

It is one of the major reliability issues in MOSFETs. NBTI plays a vital role to manifests as an increase in the V_{th} and consequent fall in value of I_D and G_m of a MOSFET, especially for the PMOS transistors. It is of valid concern for devices operating in p-channel, since they almost operate with negative gate-to-source voltage [3].

PBTI: It is a critical circuit reliability issue in highly scaled CMOS technologies. It is generally concerned for NMOS transistors and becomes a serious degrading factor in high-k metal gate technology [4].

TDDB: It is mainly a failure mechanism in MOSFETs, when the gate oxide breaks down which results from long time utilization, concerning low electric field. It is commonly used as test for constant stress. Cu interconnects are greatly affected and vulnerable to failure due to time-dependent gate oxide breakdown of low-k die-electrics. One of the major concern is of the decrease in life time with increased porosity. In addition to these issues, the HCI, NBTI and PBTI effects will further degrade the margin and can eventually lead to reduced ID, reduced speed, shift in threshold voltage, degradation in transconductance or mobility, generation of unwanted current components and circuit failures over prolonged periods [5].

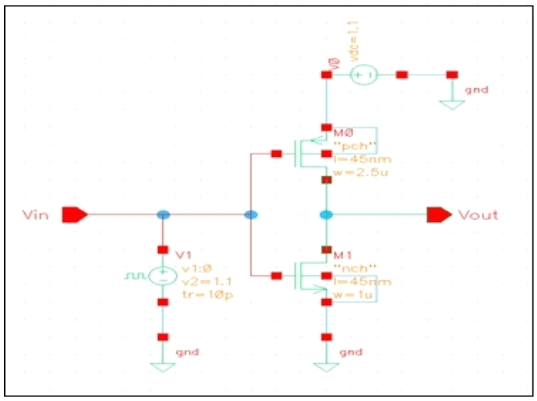

Fig.3. Implemented schematic of an inverter in cadence software using 45nm technology

The above Fig.3 shows the schematic of an inverter circuit designed with a PMOS of width 2.5µm and length 45nm and an NMOS width 1µm and length 45nm, using PCH and NCH model libraries respectively. The input is applied using a pulsating signal of 1.1V, rise time of 10ps, fall time 10ps, pulse width 10ns and period of 20ns respectively. The circuit is operated with V_{DC} 1.1V using BSIM4 model files, addresses the MOSFET physical effects into sub-100nm regime for 40ns [1]. The simulated results waveform and tabulated analysis has been shown in Fig.4 and Table.1 respectively.

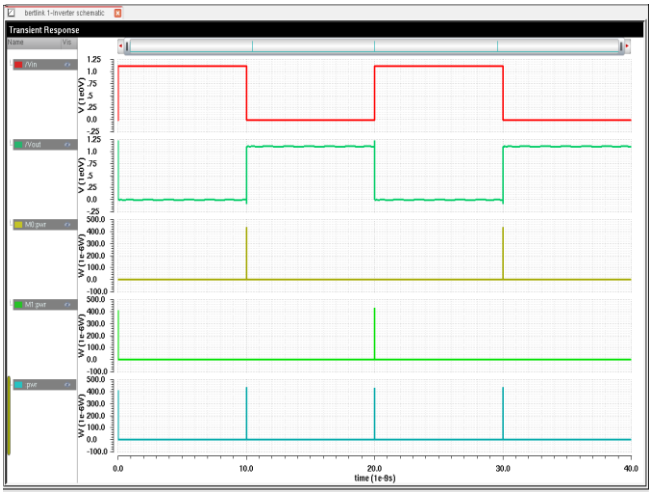

Fig.4. Transient response of an inverter (V_{in}, V_{out}, Power of PMOS, Power of NMOS & Power of the Inverter)

Table.1. Values obtained in transient analysis of inverter for duration of 0 to 40ns

Max Power of Inverter	432.9E-6W	Max. Value of V_{in}	1.1V
Min Power of Inverter	49.09E-12W	Min. Value of V_{in}	0V
Avg. Power of Inverter	185.6E-9W	Avg. Value of V_{in}	550.6E-3V
Max. Value of V_{out}	1.226V	Max. Power of PMOS	427E-6W
Min. Value of V_{out}	-105.2 E-3V	Min. Power of PMOS	48.33E-18W
Avg. Value of V_{out}	549.5E-3V	Max. Power of NMOS	432.9E-6W
Delay B/w V_{in} & V_{out}	11.18E-12s	Min. Power of NMOS	2.12E-18W

Further DC analysis is done and the corresponding values of V_{in}, V_{out} and power is calculated. DC analysis is done from -5V to 5V. The evaluated result has been shown in Fig.5 and tabulated in Table.2 respectively.

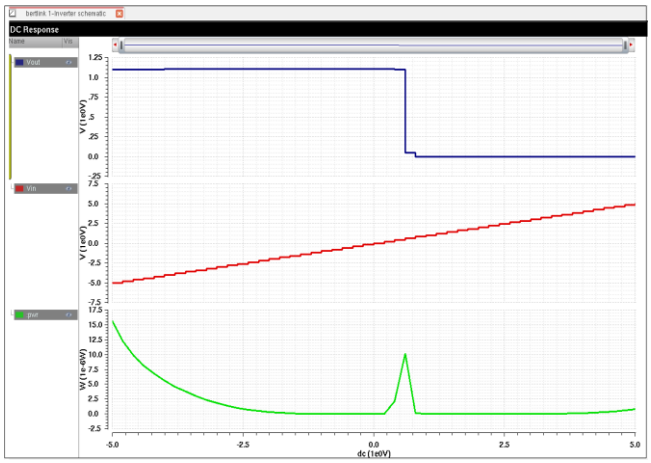

Fig.5. DC response of inverter (V_{out}, V_{in} & Power of the Inverter)

Table.2. Values obtained at DC analysis of inverter circuit

Max. Value of V_{in}	+5V	Min. Value of V_{out}	42.02E-9V
Min. Value of V_{in}	-5V	Max. Value of Power	15.54E-6W
Max. Value of V_{out}	1.1V	Min. Value of Power	17.96E-12W

The inverter is implemented and also tested for noise performance at operational frequency of 5GHz and amplitude of 10dBm ranging from input to output. The result obtained is very much significant and acceptable since the noise reduces drastically as the inverter starts operating and continues decreasing.

For the analysis the noise ports are added at both terminals and capacitor is placed. The Fig.6 below depicts the schematic diagram of the inverter designed for noise analysis. The value of capacitor used has been listed in the figure also. Three capacitors are used, one at the input terminal and two at output terminal. The input Capacitor (C_0) is of 10fF in series with port -0. The output Capacitor (C_1) is of 10fF and Output Capacitor (C_2) is of 500fF and is realized in parallel with the port-1.

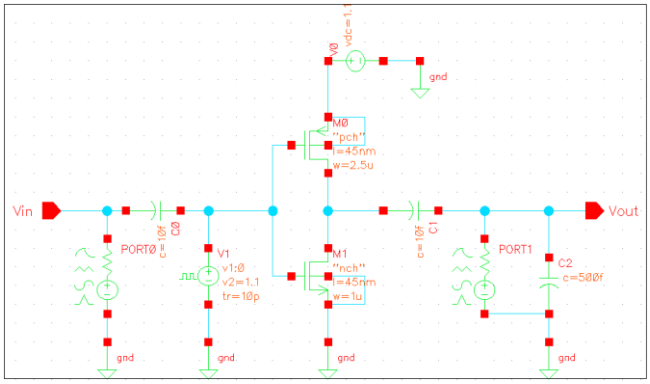

Fig.6. Schematic of inverter for noise analysis using ports at both terminals at 5GHz frequency

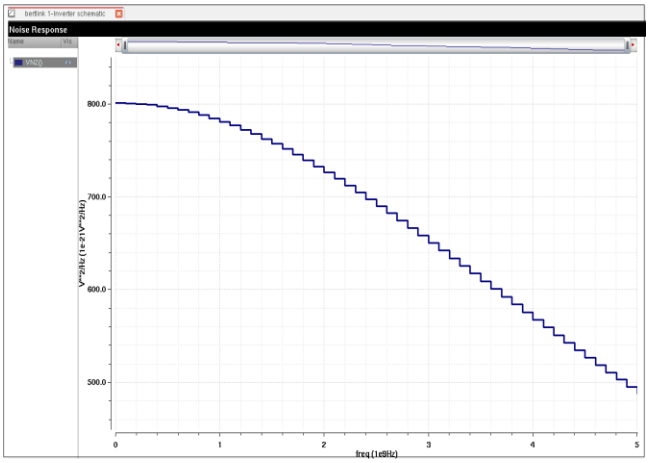

Fig.7. Noise response of inverter at operational frequency of 5GHz

2. RELIABILITY ANALYSIS OF INVERTER IN TERMS OF AVERAGE POWER

In the conventional sense, the reliability of a system is defined as the probability that which will perform its required function under stated conditions, for a stated period of time. The reliability of inverter is analyzed at five different time intervals. The major concern is the impact of HCI degradation on circuit performance. It is generally observed that under static DC stress condition, HCI device degrades for both NMOS and PMOS transistors produces changes in the threshold voltage, transconductance and current-driving capability. It is noted that when the transistors are under the dynamic operating conditions of a CMOS circuit, the MOSFET terminal voltage varies with respect to time. For this we need to model ID as a function of time.

Average power delivered falls in consideration with the time period, due to the effects of HCI, NBTI, PBTI & TDDB and circuit failures occurs over prolonged periods [6]. The reliability in terms of average power has been shown in Fig.8.

To estimate the effect of electrical interconnects, the case of two CMOS gate (a combination of two inverters joined through an RC model) has been implemented. The schematic diagram of the design having two CMOS gate has been illustrated in Fig.9.

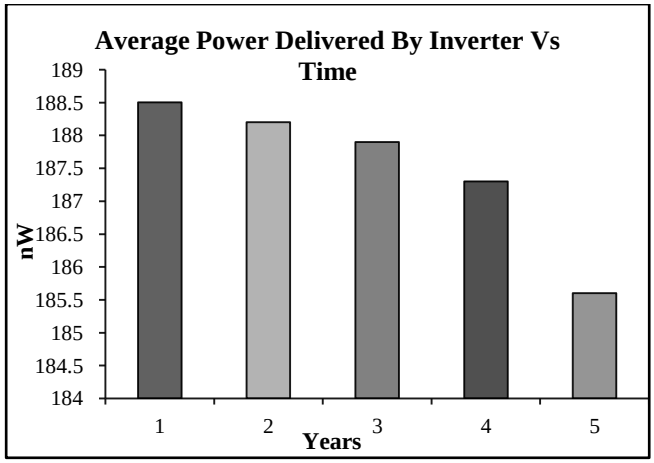

Fig.8. Reliability analysis of inverter in terms of average power delivered and time

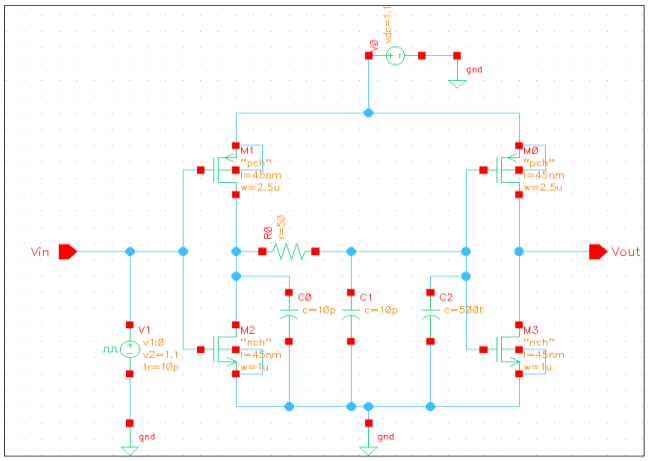

Fig.9. Schematic of two CMOS gate interconnect circuit

The schematic of two CMOS gate interconnect circuit. designed contains two PMOS having width of 2.5µm and length 45nm and two NMOS having width of 1µm and length 45nm, using pch and nch model libraries respectively. The input is applied using a pulsating signal of 1.1V, rise time of 10ps, fall time 10ps, pulse width 10ns and period of 20ns respectively. The circuit is operated with VDC 1.1V using BSIM4 model files, addresses the MOSFET physical effects into sub-100nm regime for 40ns. The electrical interconnection between the inverter is composed of an RC model [7].

Table.3. Values of passive components used in two CMOS gate schematic

R_0	50Ω	C_0	1pF
C_1	1pF	C_2	5fF

The transient analysis is analyzed for 100ns, and V_{in} vs.V_{out} is calculated. Table.3 shows various components value in the CMOS gate interconnect circuit. Schematic Fig.10 depicts the transient analysis of the circuit and power consumed by the each transistor, and the tabulated transient analysis results are given in Table.4 respectively.

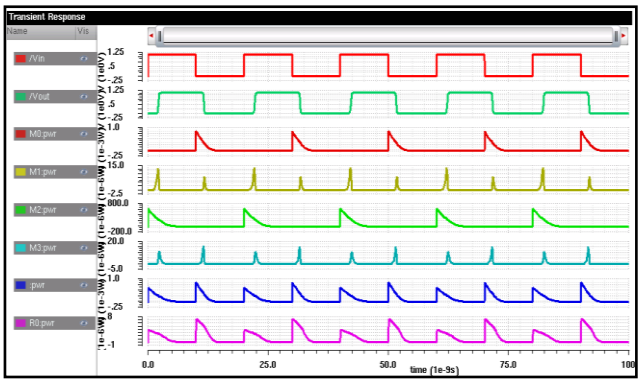

Fig.10. Transient response of two CMOS gate interconnect circuit (V_{in}, V_{out}, power consumed by Mo, M1, M2, M3, Power of the circuit & power consumed by of resistance)

Table.4. Values obtained in transient analysis of two CMOS gate interconnect circuit for duration of 0 to 100ns

Max. Value of V_{in}	1.1V	Min. Power of PMOS-1	12.09E-18W
Min. Value of V_{in}	0V	Max. Power of NMOS-1	13.24E-6W
Avg. Value of V_{in}	550.6E-3V	Min. Power of NMOS-1	333.4E-18W
Max. Value of V_{out}	1.1V	Max. Power of PMOS-2	610.1E-6W
Min. Value of V_{out}	-149.4E-6V	Min. Power of PMOS-2	449.9E-18W
Avg. Value of V_{out}	519.5E-3V	Max. Power of NMOS-2	15.9E-6W
Max. Power of Circuit	837.6E-6W	Min. Power of NMOS-2	2.454E-18W
Min. Power of Circuit	114.0E-12W	Max. Power of R0	7.150E-6W
Avg. Power of Circuit	123.3E-6W	Min. Power of R0	469.2E-21W
Max. Power of PMOS-1	837.5E-6W		

Further DC analysis is done and the corresponding values of V_{in}, V_{out} and power is calculated. DC analysis is analyzed in the range from -5V to 5V. The result has been illustrated in Fig.11 and Table.5 respectively.

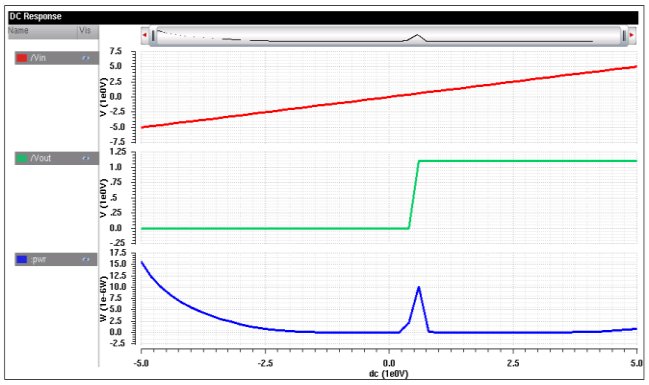

Fig.11. DC response of two CMOS gate interconnect circuit (V_{in}, V_{out} & Power of the circuit)

Table.5. Values obtained for DC analysis of two CMOS gate interconnect circuit

Max. Value of V_{in}	+5V	Max. Value of Power	15.54E-6W
Min. Value of V_{in}	-5V	Min. Value of Power	82.91E-12W
Max. Value of V_{out}	1.1V	Avg. Value of Power	1.704E-6W
Min. Value of V_{out}	40.80E-9V		

The two CMOS gate interconnect circuit is also being tested and verified for noise performance at 5GHz frequency and amplitude of 10dBm ranging from input to output. The result obtained is very much significant and acceptable since as the noise reduces drastically when the inverter starts operating and continues decreasing. The Fig.12 below shows the schematic diagram of two CMOS gate using ports at both terminals which has been designed for noise analysis. The circuit contains three capacitors, one at the input terminal and two at output terminal. The input Capacitor (C_0) is of 1pF and is added in series with port-0, the output capacitor (C_1) is of 1fF and Output Capacitor (C_2) are of 500fF, implemented in parallel with the port-1. The results have been evaluated and depicted in Fig.13 and Fig.14 respectively. The outcome suggests that with the increase in the value of frequency the noise decreases drastically. The average value of the noise for two CMOS gate circuit has been estimated to be **800.8E-21**.

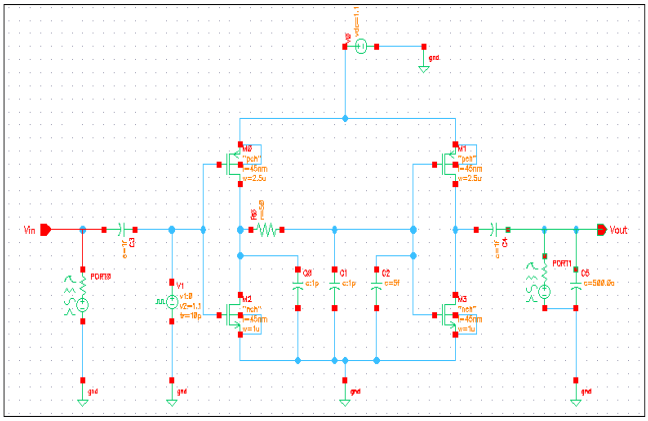

Fig.12. Schematic of two CMOS gate for noise analysis using ports at both terminals @ 5GHz

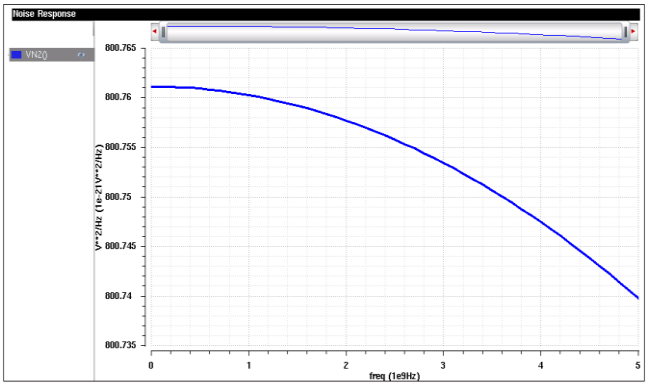

Fig.13. Noise response of two CMOS gate @ 5GHz

The reliability analysis is done in terms of delay vs. time. As it can be seen that the delay between input and output voltages increases as the interconnect circuit is analysed over prolonged period [8].

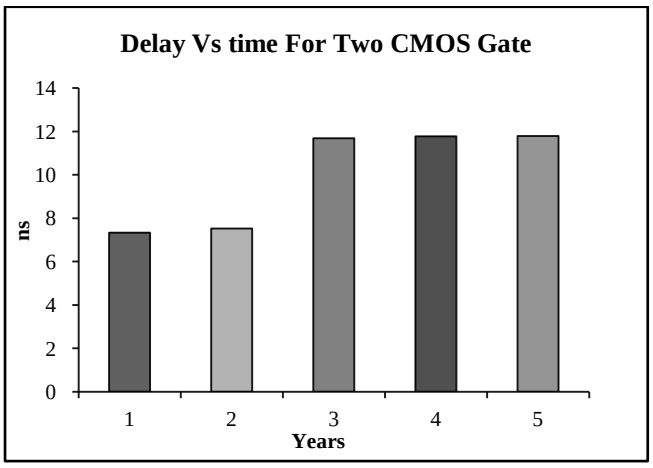

Fig.14. Reliability analysis in terms of delay vs. time for two CMOS gate

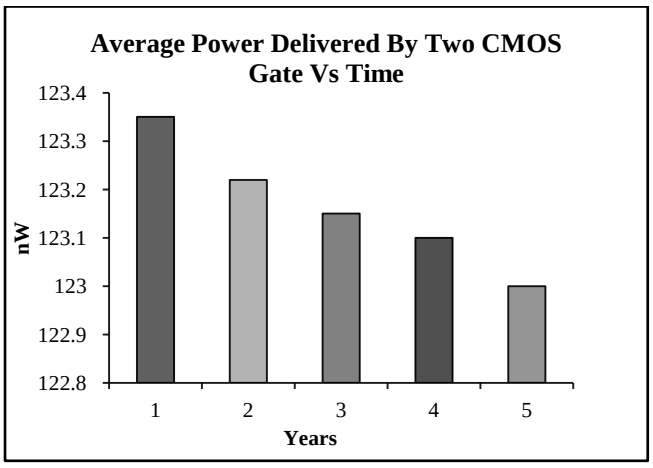

Fig.15. Reliability analysis in terms of average power delivered vs. time for two CMOS gate interconnect circuit

3. CONCLUSION

The performance and reliability analysis of an inverter and two CMOS gate interconnect circuit has been analyzed. It has been observed that with the increase in time their performance degrades due to the effects of HCI, NBTI, PBTI and TDDB phenomenon. The reliability analysis for inverter is done only in terms of average power delivered by the circuit whereas the estimation of the reliability for two CMOS gate interconnect circuit is done in terms of delay between input-output voltage and average power delivered by the circuit over different time intervals. All the reliability simulation tools developed till yet are based on transistor level circuit simulation. Hence taking into account higher level reliability simulator need to be developed, which may consider the factors like switching activity, voltage overshoot, circuit sensitivity, etc., also.

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