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BEHAVIORAL MODELLING OF CMOSFETs AND CNTFETs BASED LOW NOISE AMPLIFIER

Navaid Z. Rizvi[1], Rajesh Mishra[2] and Prashant Gupta[3]
[1,2,3]*School of Information and Communication Technology, Gautam Buddha University, India*
E-mail: navaid@gbu.ac.in[1], rmishra@gbu.ac.in[2] and mtech.prashantgupta@gmail.com[3]

Abstract

Low Noise Amplifier is considered as one of the most important component at the receiver end. The basic characteristics and features that a device should possess in the field of Wireless Sensor Network is high gain with low power consumption and size as miniaturize as possible. The Carbon Nano Tube Field Effect Transistors (CNTFETs) are being widely studied as possible successors to silicon based CMOSFETs that have a size much smaller than that of the conventional transistors. This paper presents the behavioral modeling and comparative performance interpretations of a Low Noise Amplifier based on CMOSFETs and CNTFETs using Verilog-A hardware description Language.

Keywords:

CNTFET, RF-MEMS Switch, Low Noise Amplifier, Behavioral Modeling, Verilog-A

1. INTRODUCTION

The transistors are one of the greatest inventions in the field of technology in the twentieth century which has brought about both the information as well as computation age. Its success lies in the reduced size and high operating speed. This property is described in Moore's law [1]. According to Moore's law the transistor size will decrease exponentially while the speed will increase in the same manner every year and a half. However, both physical and economic barriers have made a limitation on the continuation of Moore's law in the next decade or so. The physical barriers as well as economical limitations arise due to the continuous shrinking of the current transistors used today. As a result, the thicknesses of the insulators, which are used to electronically isolate parts of the transistor, reduces which results in various effects like short channel and tunneling effects and interconnect problems, and others. One proposed solution is the use of carbon nanotubes instead of silicon based transistors.

The Carbon nanotubes are hexagonal sheets of graphene, which are single layers of graphite atoms in the form of rolled up chicken wires as shown in figure 1. They are a part of class of molecules called Fullerenes due to its hexagonal nature. Fullerenes are closed-caged molecules containing only hexagonal and pentagonal interatomic bonding networks [2]. There are two types of carbon nanotubes, Single-Wall-Nanotube and Multi-Walled- Nanotubes. The SWNTs are most promising, cylindrical in shape. The MWNTs are a bunch of SWNTs where smaller SWNTs are placed within a larger SWNT.

The hexagonal structure of CNT offers it strength. In fact, they are found to be 50 times stronger than that of steel and yet are only a quarter as dense. Also carbon nanotubes have very good elastic properties. Another amazing property is its heat transfer characteristics. Carbon Nanotubes are able to conduct heat so well that they are more efficient than diamond [3]. Unlike most materials, they come in both metallic and semiconducting forms. Their band-gaps can be set to a desired level by simply changing the physical properties. Another unique property is that they are one-dimensional ballistic conductors even above 24ºC. Any transistors irrespective of technology are mostly tailored in accordance to speed, scalability, and power. If somehow any technology has to be replaced with the existing one, it much at least match, if not outperform. Due to the ballistic property it has the capability of operating at speeds of Terahertz or even more, compared to existing processors. While the CNTFETs improve with scaling, it is not conventional. They seem to follow the behavior of Schottky barrier MOSFETs, instead of regular MOSFETs. For this reason, a group at IBM [4] has an impression that the CNTFETs limits for scaling are unclear. However, they do note that, in a structured array configuration, they will produce gain and fan out high enough for real life applications. In addition, despite the CNTFETs murky limits of scaling, it may still outperform silicon MOSFETs [5].

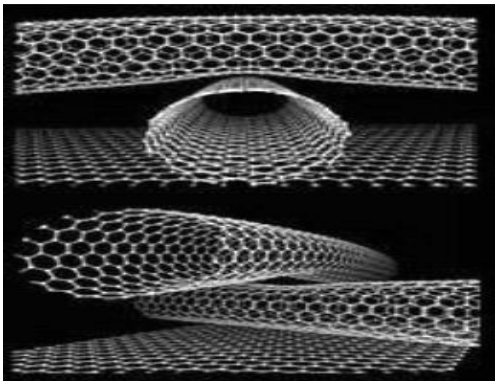
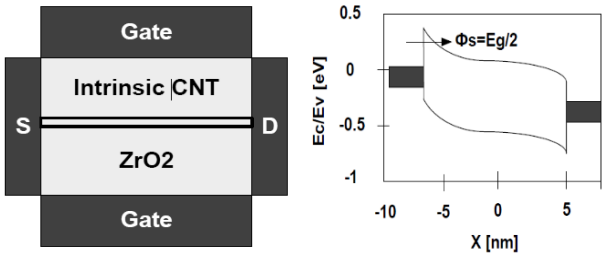


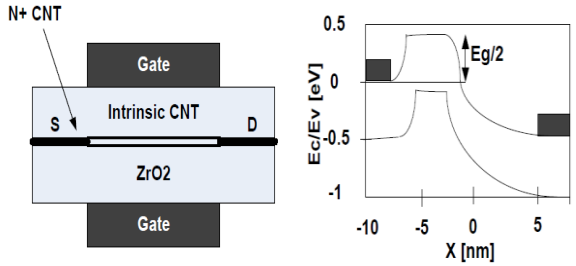
Fig.1. Carbon Nanotube sheets of Graphene

Due to "Short Channel Effects" beyond 10nm technology in CMOS based devices [6], more researchers have been ensuing on the alternative solutions. The CNTs as an alternative to CMOS technology are rolled up sheets of graphite. They can either be metallic or semiconductor depending upon the direction in which they are rolled (chirality) [7]. High-performance carbon nanotube field-effect transistors (CNFETs) with very high "on" currents have been reported and the device physics has evolved [8], [9]. Near ballistic transport no longer seems impossible looking at pace of investigation of high speed devices. The basic property of ballistic devices is the absence of scattering [10]. This makes them ultrahigh speed and suitable for high-performance circuit design. The CNT transistors based devices are still primitive and the technology is still in its early phase [9, 11].



(a) (b)

Fig.2. Two types of CNFETs. (a) A physical diagram of a Schottky barrier CNFET. Here a high K dielectric (ZrO) has been used. (b) The band diagram of the Schottky barrier CNFET indicating the tunneling barrier



(a) (b)

Fig.3. Two types of CNFETs. (a) A physical diagram of a MOSFET-like CNFET. Here a high K dielectric (ZrO) has been used. (b) The band diagram of the MOSFET-like CNFET indicating the absence of any tunneling barrier. Also, note that the barrier height at the source–channel junction is $E_{G/2}$

Depending on their chirality (i.e., the direction in which the graphite sheet is rolled), the CNTs can either be metallic or semiconducting in nature [7]. Its semiconducting nature has attracted widespread attention of electron devices and circuit designers. CNFETs are seen as potential successors to Silicon FETs. They have been proved to be promising molecular transistors because of their high "on" current density and moderately high "on-off" ratio. One of the devices is a tunneling device [Fig.2(a) and Fig.2(b)] which works on the principle of direct tunneling through a Schottky barrier at the source-channel junction [12]. By applying gate voltage the barrier width can be adjusted. The trans-conductance of the device is dependent on the gate voltage. To overcome the problems associated with the Schottky barrier CNFETs, attempts have been made to develop CNFETs that can behave like normal MOSFETs [Fig.3(a) and Fig.3(b)] [10, 13]. In this MOSFET-like device, the ungated portion (source and drain regions) is heavily doped [14] and operates on the principle of barrier-height modulation by application of the gate potential. In this case, the on-current that can be induced in the channel by gate is controlled by the amount of charge. It is obvious that the MOSFET-like device will give a higher on-current and, hence, would define the upper limit of performance [14], [15]. Recent experiments have demonstrated that the CNFET can typically be used in the MOSFET-like mode of operation with near ballistic transport [10, 16].

A comparison in the parameters for the CNTFETs and MOSFETs transistors are depicted in Table.1 [4, 17]. As can be seen in the table, the difference is in I_{OFF} current. As compared to the conventional MOSFET, CNTFET have a drop of about 70%. This means that the power being dissipated is reduced significantly in OFF state. Also, I_{ON} or drive current is three to four times larger than the conventional technology. The CNTFETs transistors would lead to higher power consumption but since the nanotube has ballistic conductance, it actually has a smaller resistance. Thus, the power consumption is the same if not smaller than the current MOSFET design. There is also an increase in trans-conductance by three to four times. The real big surprise is although the CNTFETs have large gate length and gate oxide they are able to outperform the existing and newer technologies.

Table.1. Comparison of CNFETs with MOSFETs [4, 17]

Parameters	CNTFET	MOSFET
Gate Length(nm)	260	15
Gate oxide Thickness (nm)	16	1.4
V_t (V)	-0.5	~ -0.1
I_{ON} (µA/µm)	2100	265
I_{OFF} (nA/µm)	150	<500
Subthreshold slope (mV/dec)	130	~ 100
Transconductance (µS/µm)	2321	975

2. DESIGN IMPLEMENTATION OF CMOS-FETs AND CNT-FETs BASED LNA

The proposed research work focused on the comparison for the performances of the CMOSFETs and CNTFETs based Low Noise Amplifiers. Regarding the same the most commonly used circuit of CMOS LNA [18], as shown in Fig.4, has been implemented in Cadence Analog Design environment. The LNA has an input stage that provides input match and current gain at the resonant frequency. A cascade block is added to the input stage to mitigate the interaction between the input and output tank. The stability of the circuit is increased by the cascade by reducing the reverse gain through the amplifier. Furthermore, by forming a low impedance node at the drain of transistor M1, the effect of the C_{gd} of M1 is reduced. The output inductor, L_d, is designed such that it resonates at ω_o with the node capacitance at the output. For a narrowband gain the input and output tank are aligned. The input and output are offset to achieve broader and flatter frequency response [6, 17].

For realization of Carbon Nanotube based Transistors, behavioral modeling using Verilog-A code has been utilized. A ballistic CNTFETs based 1-D electrostatics model has been implemented. This model is taken as it may be be used for a wide range of CNFETs having diameters in the range 0.6 to 3.5 nm and for all chirality as long as they are semiconducting. This model uses suitable approximations necessary for developing any quasi-analytical, circuit-compatible compact model. The proposed model is designed for unipolar behavior CMOS-like CNFET device. The minimum channel length (~10nm) is restricted by the complex quantum mechanisms. In principle, this model has no limitation on the maximum gate length of CNFET.

Devices with gate length longer than 100 nm are treated as long channel device. The transition from the short channel model (10nm < L_g < 100nm) to the long channel model (L_g > 100nm) is continuous and is automatically handled by the model [19].

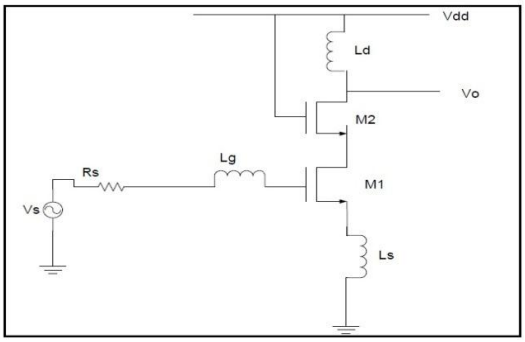


Fig.4. The CMOS Low Noise Amplifier [18]

The proposed transistor model has been implemented in Cadence Analog Design Environment and verified for DC and transient simulation analysis. The proposed single CNT transistor model's symbol is generated. This symbol replaced all the MOSFETs in the taken circuit of CMOS based LNA [18].

3. SIMULATION AND ANALYSIS OF PROPOSED CMOSFETs AND CNTFETs LNA

In this section the most relevant simulation results of both LNA design are presented. Simulations at the Behavioral level using Verilog A code have been performed using Cadence Spectre RF tool. The obtained V-I characteristics of CNTFET's I_d v/s V_{ds} and I_d v/s V_{gs} has been shown in Fig.5 and Fig.6 respectively. The parameters taken for realizing behavioral modeling of the proposed model using Verilog A code has been depicted in Table.2.

In the simulation of CMOS LNA, performance parameters like scattering parameters, power gain, noise figure, stability factors are obtained in the frequency range of 1GHz to 8GHz. The Fig.7 shows the return loss performance that is very important for matching determination of the LNA with other component. The S11 come out to be well below -2.5 dB. For perfectly matched condition the return loss should be as zero as possible but this only achieved in idealistic conditions.

While performing the behavioral modeling of CNTFETs based Low Noise Amplifiers the parameters are set in Verilog A code as per Table.2.

Table.2. Parameters taken in CNTFETs based LNA

Parameters	Description	Values
d	Diameter	1nm
Gate Oxide Thickness (nm)	16	1.4
θ	Chiral Angle	0
tins	Insulator Thickness	10nm
eins	Dielectric Constant of Insulator	25
tback	Substrate Insulator Thickness	100nm
eback	Substrate Insulator Dielectric Constant	3.9
L	Gate Length	100nm
Type	N type = 1 or P type = 1	1
phisb	Schottky Barrier Height	0eV
mob	Scattering Parameter	1
R_s/R_d	Parasitic Access Resistance	0
β	Coupling Coefficient	20
C_c	Coupling Capacitance	7aF/µm
Csubfit	Flat Band Correction Factor	1
C_p	Parasitic Capacitance	0

4. RESULTS AND DISCUSSION

The V-I characteristic and Variation of drain current with gate-source voltage of the proposed single CNT transistor have been obtained and depicted in Fig.5 and Fig.6 respectively.

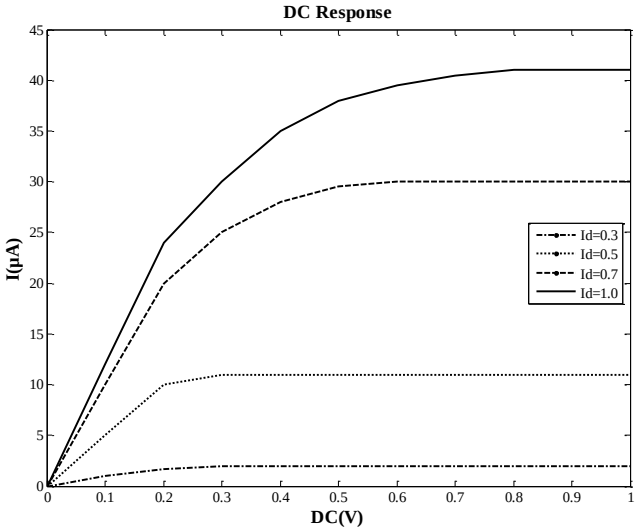


Fig.5. V-I Characteristics obtained of single CNTFET (I_d v/s V_{ds})

The reflection losses (Fig.7) and transmission losses (Fig.8) have been evaluated for implemented CMOSFETS based LNA.

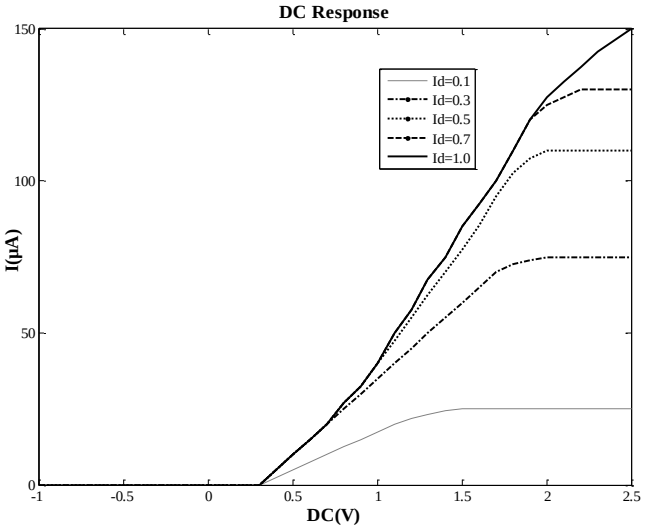


Fig.6. Variation of I_d with V_{gs} in a single CNTFET

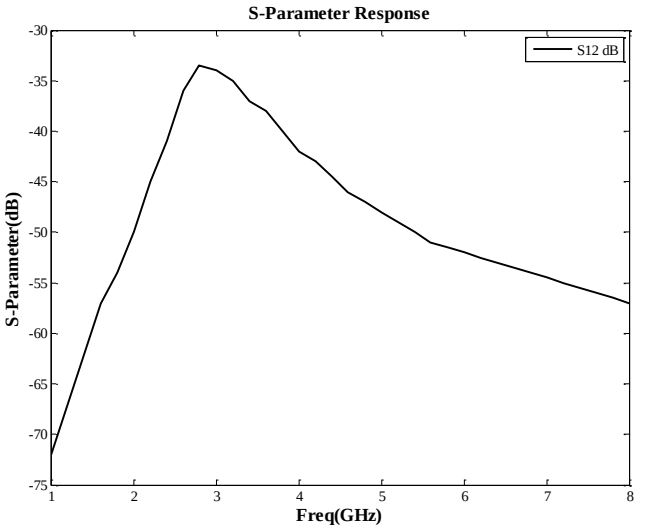


Fig.7. Reflection Loss for CMOSFET Low Noise Amplifier obtained through simulations

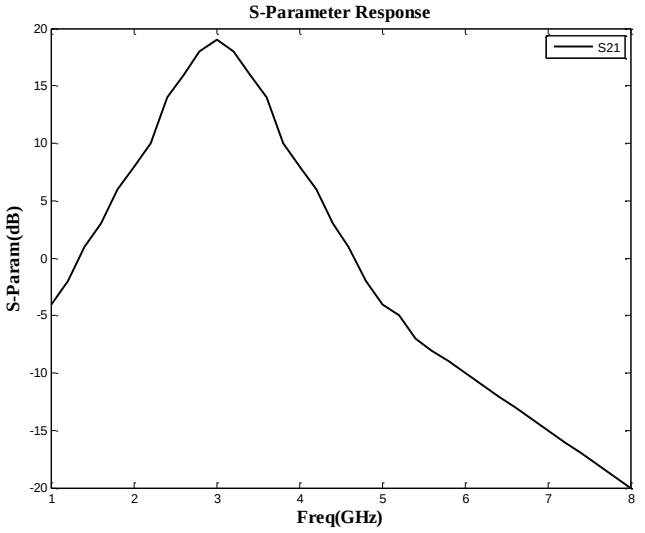


Fig.8. Transmission Coefficient parameter for CMOSFET Low Noise Amplifier obtained through simulations.

The Fig.9 which is the obtained simulations result of CNTFETs based LNA clearly indicates that the return loss S11 has been -872p dB which is quite close to 0 dB. The Reverse isolation, the power gain, noise figure and transmission coefficient parameter obtained for CNTFETs based LNA are -0.96k dB, 25 dB, 1.5μ dB and 22 dB respectively. For a LNA to be stable, parameters must satisfy K_f >1 and B_{1f} < 1.

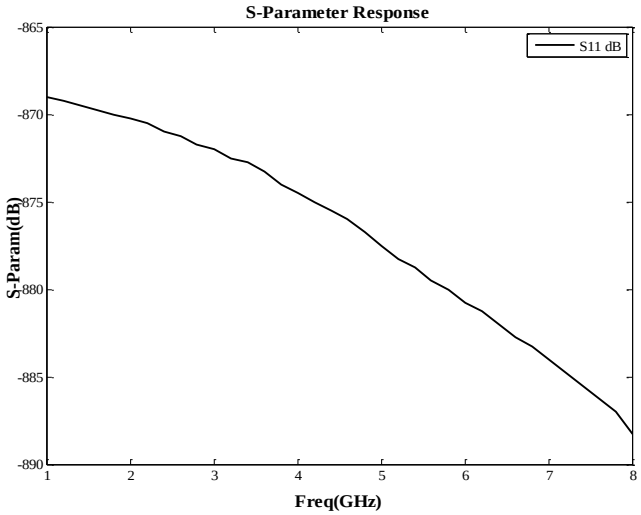


Fig.9. Obtained S11 parameter for the CNTFETs LNA

The obtained stability factor K_f and B_{1f} are 1.8 and 0 .8 respectively which makes the proposed CNTFETS design stable. The power gain evaluated to be 25 dB and the noise figure has been nearly 0 dB.

The Comparative results obtained from simulation of CMOSFETs based LNA and CNTFETs based LNA has been illustrated in Table.3 and Fig.10.

Table.3. Comparative obtained results of CMOSFETs and CNTFETs based LNA

Obtained Results	**CMOS LNA**	**CNT LNA**
Technology (channel length)	0.18 μm	0.18 μm
Forward Voltage Gain (S_{21}) dB	15 dB	22 dB
Reverse Isolation (S_{12}) dB	-40 dB	-96k dB
Reflection coefficient (S_{11}) dB	-2.5 dB	-872p dB
Output Matching (S_{22}) dB	-2.6 dB	-2.6m dB
Noise Figure (dB)	1.5 dB	1.5μ dB
Power Gain (dB)	20 dB	25 dB
K-Factor (>1)	1.8	1.8

The obtained results clearly indicate that CNTFETs LNA has nearly 0 reflection losses as compared to -2.5 dB. The forward Voltage gain (Transmission Coefficient) is also better for CNTFETs. The K-Factor for both the design is comparable. The estimated noise figure of the CNTFETs based has been 1.5 μdB

which shows nearly zero noise loss in the device. The power gain obtained for the CMOSFETs is less than the other design.

5. CONCLUSIONS

The Design of a LNA using CMOS and CNTFET has been presented and analysis are carried through obtained performance parameters like power gain, noise figure, reflection coefficient, transmission coefficient, and more. It enables integration of an RF CNTFET LNA design. Here design works are chosen in the frequency region of WLAN IEEE standard like 802.11g/n operated at the frequency of 2.4 GHz/5 GHz. The CNFET is evaluated for use in a low noise amplifier. The obtained performance clearly indicates that the CNTFET LNA can be much better RF performance device than CMOSFET LNA, with the exception of CNFET noise. The major limitation has been the realization of the device through actual fabrications. The findings in research work support the idea that a top-gated Ballistic CNFET which can be modeled and used to be used in nanoelectronics, as improvements in performance has trended upwards with new technologies.

6. FUTURE WORK

The research progress may be made that can resolve the unseen and still to discover the issues that are limiting CNFET technology for the RF performance. Outside of measurement issues, the challenges like the presence of parasitic capacitances, and a low current capacity and gain for individual nanotubes. By increasing the number of parallel nanotubes in the transistor channel, parasitic capacitances can be reduced and current capacity and gain can be improved.

With the daily increase in the scaling Moore's law is going to get violated (below 10nm). New transistor layouts which enable multiple gate fingers to reduce the parasitic capacitances while increasing gain will be introduced. Increasing the purity of nanotube arrays may improve the gain and bandwidth of transistors.

Further the proposed LNA can be designed for multi-frequency operations. This can be achieved by integrating this LNA with RF MEMS switch which can be utilized reconfigurability to the design.

7. ACKNOWLEDGEMENT

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REFERENCES

[1] H.S.P Wong, "Beyond the Conventional Transistor", *IBM Journal of Research & Development*, Vol. 46, No. 2/3, pp. 133-168, 2002.

[2] Deepak Srivastava, Madhu Menon and Kyeongjae Cho, "Computational Nanotechnology with Carbon Nanotubes and Fullerenes", *Computing in Science and Engineering*, Vol. 3, No. 4, pp. 42-55, 2001.

[3] Phaedon Avouris, Joerg Appenzeller, Richard Martel and S.J. Wind, "Carbon Nanotube Electronics", *Proceedings of the IEEE*, Vol. 91, No. 11, pp. 1772- 1784, 2003.

[4] S.J. Wind, J. Appenzeller, R. Martel, V. Derycke and Ph. Avouris, "Vertical Scaling of Carbon Nanotube Field-Effect Transistors Using Top Gate Electrodes", *Applied Physics Letters*, Vol. 80, No. 20, pp. 3817-3819, 2002.

[5] R. Martel, V. Derycke, J. Appenzeller, S. Wind and Ph. Avouris, "Carbon Nanotube Field-Effect Transistors and Logic Circuits", *Proceedings of the 39th Design Automation Conference*, pp. 94-98, 2002.

[6] K. Roy, S. Mukhopadhyay and H. Meimand-Mehmoodi, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicron CMOS Circuits", *IEEE Proceedings*, Vol. 91, No. 2, pp. 305-327, 2003.

[7] P.L. McEuen, Michael S. Fuhrer and Hongkun Park, "Single - Walled Carbon Nanotube Electronics", *IEEE Transactions on Nanotechnology*, Vol. 1, No. 1, pp. 78-85, 2002.

[8] Johan Janssens and Michiel Steyaert, "*CMOS Cellular Receiver Front-Ends*", Springer, 2002.

[9] Jing Guo, Supriyo Datta and Mark Lundstrom, "Assessment of Silicon MOS and Carbon Nanotube FET Performance Limits Using a General Theory of Ballistic Transistors", *Proceedings of International Electron Devices Meeting*, pp. 711-714, 2002.

[10] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. Mcintyre, P. Mceuen, M. Lundstorm and H. Dai, "High-K Dielectrics for Advanced Carbon Nanotube Transistors and Logic Gates", *Nature Materials*, Vol. 1, pp. 241-246, 2002.

[11] M. S. Lundstrom and Zhibin Ren, "Essential Physics of Nanoscale MOSFETs", *IEEE Transactions on Electron Devices*, Vol. 49, No. 1, pp. 133-141, 2002.

[12] J. Guo, S. Datta and M. Lundstrom, "A Numerical Study of Scaling Issues for Schottky Barrier Carbon Nanotube Transistors", *IEEE Transactions on Electron Devices*, Vol. 51, No. 2, pp. 172-177, 2003.

[13] A. Javey, J. Guo, Q. Wang, M. Lundstrom and H. Dai, "Ballistic Carbon Nanotube Field-Effect Transistors," *Nature*, Vol. 427, No. 6949, pp. 654-657, 2003.

[14] Jing Guo, Ali Javey, Hongjie Dai, Supriyo Datta and Mark Lundstrom, "Predicted Performance Advantages of Carbon Nanotube Transistors with Doped Nanotubes Source / Drain", *Mesoscale and Nanoscale Physics*, 2003.

[15] Ali Javey, Jing Guo, Qian Wang, M.S. Lundstrom and Hongjie Dai, "Schottky Barrier Free Nanotube Transistors Near the Ballistic Transport", *Nature*, Vol. 424, No. 6949, pp. 654-657, 2003.

[16] S.J. Wind, J. Appenzeller, and Ph. Avouris, "Lateral Scaling in Carbon Nanotube Field-Effect Transistors", *Physical Review Letters*, Vol. 91, No. 5, pp. 1-4, 2003.

[17] Navaid Z. Rizvi and Rajesh Mishra, "Realization and Performance Estimation of Integrated CMOS LNA with F-Inverted Antenna for Mobile Communication", *ICTACT Journal on Microelectronics*, Vol. 1, No. 1, pp. 14-18, 2015.

[18] Asha Balijepalli, Saurabh Sinha and Yu Cao, "Compact Modeling of Carbon Nanotube Transistor for Early Stage Process-Design Exploration", *Proceedings of the International Symposium on Low Power Electronics and Design*, pp. 2-7, 2007.