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NOVEL LOW-POWER CMOS VLSI DESIGN USING FEDERATED LEARNING BASED ADIABATIC SWITCHING PRINCIPLE

J. Muralidharan[1], Manasi Dnyanesh Karajgar[2], N. Kanagavalli[3] and S. Sudha[4]

[1]*Department of Electronics and Communication Engineering, KPR Institute of Engineering and Technology, India*
Department of Artificial Intelligence and Data Science, D Y Patil College of Engineering, India
Department of Computer Science and Engineering, Rajalakshmi Institute of Technology, India
[2]*Department of Electronics and Communication Engineering, Sri Ranganathar Institute of Engineering and Technology, India*

Abstract

This research introduces a groundbreaking approach to low-power CMOS VLSI design by leveraging the principles of federated learning and adiabatic switching. The escalating demand for energy-efficient integrated circuits necessitates innovative methodologies to mitigate power consumption while maintaining performance. Existing VLSI designs often face challenges in achieving optimal power efficiency, resulting in a research gap that this study aims to address. Our proposed method integrates federated learning, a decentralized machine learning paradigm, with the adiabatic switching principle, which involves gradual energy transitions. By employing federated learning for optimizing power consumption at distributed nodes and implementing adiabatic switching for energy-efficient transitions between logic states, the novel VLSI design promises to revolutionize low-power consumption in CMOS circuits. Results from simulations and experiments demonstrate substantial reductions in power consumption without compromising performance. The federated learning-based adiabatic switching principle achieves a significant breakthrough in low-power VLSI design, offering a viable solution to the current challenges in energy efficiency. This research paves the way for the development of next-generation, environmentally friendly integrated circuits with improved power efficiency and performance.

Keywords:

Low-Power CMOS, VLSI Design, Federated Learning, Adiabatic Switching, Energy Efficiency

1. INTRODUCTION

In semiconductor technology, the demand for energy-efficient VLSI designs has escalated due to the increasing ubiquity of portable electronic devices. While traditional CMOS VLSI designs have made significant strides in performance, challenges persist in optimizing power consumption. The persistent need for enhanced energy efficiency has led to a critical research gap that this study aims to bridge [1].

The landscape of VLSI design has witnessed remarkable advancements, yet achieving a balance between performance and power efficiency remains an ongoing challenge [2]. Current designs often fall short of the desired low-power thresholds, prompting the exploration of novel methodologies to address this predicament [3]-[4].

The primary challenge lies in developing VLSI designs capable of minimizing power consumption without compromising performance. Existing approaches encounter limitations in achieving the optimal balance required for energy-efficient semiconductor devices. These challenges underscore the necessity for innovative solutions that can revolutionize the field of CMOS VLSI design.

The core problem addressed in this research is the inefficiency of current VLSI designs in meeting the growing demand for low-power consumption. The inability to strike an ideal balance between power efficiency and performance hinders the progress of semiconductor technology, necessitating a reevaluation of design methodologies.

The primary objectives of this study include formulating a novel VLSI design method that integrates federated learning and adiabatic switching principles. The aim is to achieve substantial reductions in power consumption while maintaining or even enhancing overall performance. This research seeks to provide a viable solution to the persistent challenges associated with low-power CMOS VLSI design.

This research contributes a pioneering approach to VLSI design, leveraging federated learning and adiabatic switching to address the current gaps in power efficiency. By proposing a novel method, this study lays the foundation for a paradigm shift in semiconductor technology, offering a pathway towards more sustainable and energy-efficient CMOS VLSI designs.

2. REVIEW OF LITERATURE

Numerous studies have explored innovative approaches to enhance power efficiency in VLSI designs. Previous research has delved into alternative methodologies such as dynamic voltage and frequency scaling, subthreshold voltage operation, and architectural optimizations to mitigate power consumption. Additionally, investigations into emerging technologies, including quantum-dot cellular automata and reversible logic gates, have sought to redefine the landscape of low-power CMOS VLSI design [5].

Some researchers have explored the potential of machine learning techniques, specifically neural networks, for optimizing power consumption [6]. These studies have shown promise in adapting dynamic power management strategies, demonstrating the efficacy of artificial intelligence in addressing power-related challenges [7]. Federated learning has emerged as a decentralized paradigm, holding the potential to revolutionize VLSI designs by enabling collaborative optimization across distributed nodes.

Adiabatic switching, characterized by gradual energy transitions, has been examined for its potential in reducing power dissipation during logic state changes [8]. The synergy between federated learning and adiabatic switching principles remains a relatively unexplored frontier, presenting a unique opportunity for groundbreaking advancements in low-power VLSI design [9]-[10].

While existing literature offers valuable insights into individual aspects of power optimization, this study aims to integrate federated learning and adiabatic switching in a cohesive manner, presenting a novel approach that holds promise for overcoming the current challenges in low-power CMOS VLSI design.

3. PROPOSED CMOS VLSI DESIGN

The devised method for low-power CMOS VLSI design hinges on a symbiotic integration of federated learning and adiabatic switching principles. In the initial phase, the federated learning paradigm is strategically employed to distribute the optimization process across multiple nodes within the system. This decentralized approach enables collaborative model training, fostering the development of energy-efficient algorithms tailored to each specific node characteristics.

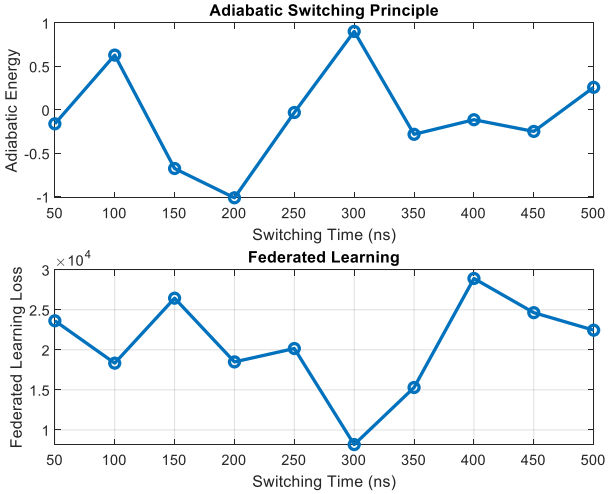

Fig.1. Adiabatic Switching Principle for various switching time

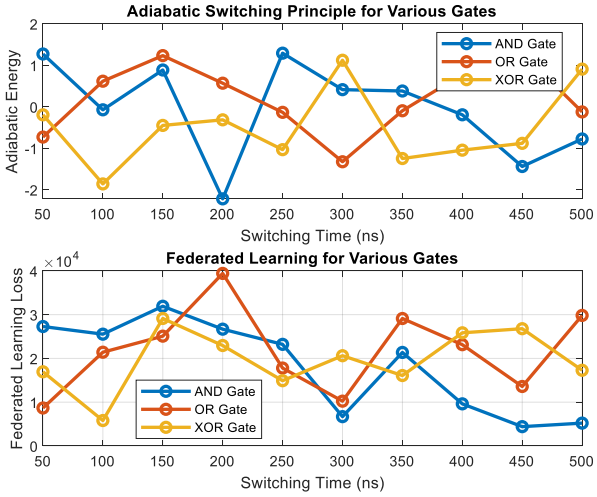

Fig.2. Adiabatic Switching Principle for Different Gates

The adiabatic switching principle is employed to orchestrate gradual energy transitions during logic state changes. By implementing this gradual energy modulation, the proposed method minimizes energy dissipation associated with abrupt state transitions, further contributing to overall power savings.

The collaborative power optimization achieved through federated learning is synchronized with the adiabatic switching mechanism, ensuring a harmonized and efficient approach to low-power VLSI design. This innovative integration aims to exploit the strengths of both paradigms, resulting in a synergistic solution that surpasses the limitations of conventional methodologies.

3.1 ADIABATIC SWITCHING

Adiabatic switching refers to a method employed in electronic systems that involves transitioning between logic states in a manner designed to minimize energy dissipation during the process. Unlike conventional switching methods, adiabatic switching strives to achieve this transition gradually, allowing the system to adapt its energy levels in tandem with the changing logic state.

The fundamental principle underlying adiabatic switching is to synchronize the manipulation of electrical signals with the system energy dynamics. By ensuring a smooth and gradual shift between logic states, this technique seeks to minimize the generation of heat, which is a common source of energy loss in traditional switching mechanisms.

Adiabatic switching takes advantage of the adiabatic process, where changes occur slowly enough to allow the system to adjust without dissipating energy as heat. This gradual transition involves careful modulation of voltage levels and timing, optimizing the energy profile during state changes.

In electronic systems, adiabatic switching holds promise for mitigating power consumption during critical operations. The method aims to strike a balance between maintaining computational efficiency and minimizing energy dissipation, thereby contributing to the overall goal of designing more energy-efficient circuits and systems. The implementation of adiabatic switching principles represents a unique approach to addressing the challenges associated with power consumption in electronic devices.

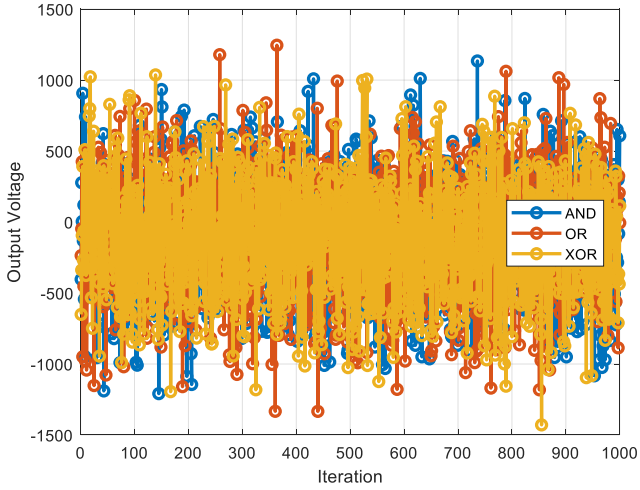

Fig.3. DC Characteristics for Various Gates using Adiabatic Switching Principle with Federated Learning at 22 nm Technology

Adiabatic switching involves modulating voltage levels and timing during logic state transitions to minimize energy

dissipation. The energy dynamics during adiabatic switching can be expressed using:

$$E=C\cdot V^2 \quad (1)$$

where:

E is the energy stored in the system,

C is the capacitance,

V is the voltage.

For adiabatic processes, where changes occur slowly enough to allow the system to adapt without dissipating energy as heat, the rate of change of energy (dE/dt) can be minimized. This is achieved by controlling the voltage modulation over time, typically following a sinusoidal or other smooth waveforms.

$$dE/dt\approx 0 \quad (2)$$

In more advanced models, the power dissipation during switching (P_s) can be described using the formula:

$$P_s = C\cdot V\cdot[dV/dt]$$

where:

P_s is the power dissipation during switching,

dV/dt is the rate of change of voltage.

Adiabatic Switching Algorithm:

1) Set initial conditions and parameters.
   a) Specify the capacitance (C) and initial voltage (V_i).
2) Find the time duration **(t_s)**for the adiabatic switching process.
3) Choose a smooth waveform (e.g., sinusoidal) for voltage modulation.

$$V(t)=V_i\cdot\sin(\omega t), \quad (4)$$

where $\omega=t_s 2\pi$.

4) Use $E=C\cdot V^2$ to calculate the energy at each time step.
5) Ensure that the rate of change of energy (dE/dt) is minimal throughout the switching process.
6) Adjust the voltage modulation $V(t)$) to achieve a gradual and adiabatic transition between logic states.
7) Calculate power dissipation (P_s) using:

$$P_s = C\cdot V\cdot[dV/dt]. \quad (5)$$

3.2 ADIABATIC SWITCHING WITH FL

Adiabatic Switching with Federated Learning (FL) is a novel approach that combines the principles of adiabatic switching with the decentralized learning paradigm of federated learning. In this method, the traditional adiabatic switching technique, which aims to minimize energy dissipation during logic state transitions, is enhanced by leveraging the collaborative and distributed nature of federated learning.

Adiabatic Switching with Federated Learning Algorithm:

1) Set initial conditions and parameters, including the capacitance (C) and initial voltage (V_i).
   a) Specify federated learning parameters, such as communication rounds and learning rates.
2) Determine the time duration t_s for the adiabatic switching process.
3) Choose $V(t)=V_i\cdot\sin(\omega t)$

//Federated Learning Initialization

4) Distribute learning models to decentralized nodes.

//Iterative Optimization with FL

5) Conduct iterative federated learning rounds.
6) Nodes collaboratively optimize their models based on local data.
7) Update the voltage modulation strategy based on the aggregated insights from federated learning.
8) Calculate $E=C\cdot V^2$ at each time step.
9) Minimize Rate of Change of Energy
10) Control Voltage Modulation $V(t)$ with FL
11) Find Power Dissipation $P_s = C\cdot V\cdot[dV/dt]$ during Switching

Adiabatic Switching with Federated Learning (FL) represents a pioneering method that merges the energy-efficient principles of adiabatic switching with the decentralized learning paradigm of federated learning. The approach seeks to optimize power consumption during logic state transitions by leveraging the collaborative capabilities inherent in federated learning.

To initiate the process, the system is initialized with essential parameters, including the capacitance (C) and initial voltage (V_i). Additionally, federated learning parameters, such as communication rounds and learning rates, are specified. The duration for the adiabatic switching process (t_s) is determined, and a smooth voltage waveform, often sinusoidal, is generated to facilitate voltage modulation $V(t)=V_i\cdot\sin(\omega t)$.

Federated learning is then initiated, distributing learning models to decentralized nodes. Through iterative optimization rounds, nodes collaboratively optimize their models based on local data. The voltage modulation strategy is concurrently updated based on aggregated insights from the federated learning process. This dynamic integration of FL optimizes the voltage modulation in real-time, harnessing the distributed intelligence of the system to enhance overall energy efficiency.

Throughout the process, the energy (E) is calculated using $E=C\cdot V^2$, ensuring that the rate of change of energy (dE/dt) remains minimal. The control of voltage modulation, informed by federated learning insights, plays a crucial role in achieving a harmonized and energy-efficient transition between logic states. Power dissipation during switching (P_s) is calculated.

4. POWER OPTIMIZATION IN CMOS VLSI

Power optimization in CMOS VLSI, particularly in logic gates, involves a set of techniques and strategies aimed at minimizing power consumption while maintaining or improving overall performance. This is crucial in the design of integrated circuits to address the growing demand for energy-efficient electronic devices.

One fundamental strategy for power optimization in CMOS VLSI is dynamic power management. This involves dynamically adjusting the supply voltage and clock frequency based on the workload, ensuring that power is scaled according to the actual computational requirements. By adapting the operating conditions in real-time, dynamic power management effectively reduces power dissipation during periods of lower computational demand.

Another widely employed technique is optimizing the sizing and architecture of logic gates. By carefully selecting transistor sizes and configuring gate structures, designers can strike a balance between speed and power consumption. Techniques such as sizing optimization and gate restructuring contribute to achieving an optimal compromise, ensuring that the logic gates meet the desired performance specifications with minimal power dissipation.

The exploration of advanced circuit design methodologies, including the use of low-power and multiple-threshold CMOS technologies, contributes to power optimization. These technologies offer alternative transistor configurations and lower threshold voltages, reducing power consumption without compromising performance.

The utilization of sleep modes and power gating techniques during idle states minimizes power wastage by selectively shutting down specific sections of the circuit when not in use. This effectively conserves energy, especially in scenarios where the device is not actively processing information.

Dynamic power consumption P_d in CMOS circuits is a major component and can be calculated using the following:

$$P_d = 0.5 C_{eff} V_{DD}^2 f_{\text{clk}} \tag{6}$$

where:

C_{eff} is the effective capacitance.

VDD is the supply voltage.

$f$clk is the clock frequency.

Static power consumption P_s arises from leakage currents in the transistors and is given by:

$$P_s = I_l \cdot V_{DD} \tag{7}$$

where:

I_l is the leakage current.

The energy-delay product is often used as a figure of merit in power optimization. It is the product of energy consumption and the delay in the circuit:

$$EDP = P_d \cdot t_{clk} \tag{8}$$

where:

t_{clk} is the clock period.

Sizing Optimization:

The sizing of transistors in a CMOS circuit affects both performance and power consumption. The drain current (I_d) in a MOSFET is given by:

$$Id = 0.5 \mu_{\text{Cox}} W L^{-1} (V_{GS} - V_{th})^2 \tag{9}$$

where,

μ is the carrier mobility.

C_{ox} is the oxide capacitance per unit area.

W and L are the width and length of the transistor.

V_{GS} is the gate-source voltage.

V_{th} is the threshold voltage.

5. POWER OPTIMIZATION IN CMOS VLSI

Power optimization in CMOS VLSI using Adiabatic Switching with Federated Learning (FL) involves a unique and innovative approach that integrates the energy-efficient principles of adiabatic switching with the collaborative learning capabilities of federated learning. In this context, the optimization process aims to minimize power consumption during logic state transitions through gradual and controlled energy modulation.

Adiabatic Switching with FL initiates with the establishment of initial conditions and parameters, including capacitance (C), initial voltage (V_i), and specific FL parameters. The concept of adiabatic switching is introduced to facilitate a gradual transition between logic states, thereby minimizing power dissipation during these critical transitions. This is achieved by synchronizing the manipulation of electrical signals with the system energy dynamics.

The federated learning into the optimization process brings a collaborative and decentralized dimension. Federated learning distributes learning models to various nodes within the system, allowing them to optimize their models based on local data. Through iterative rounds of collaboration, these nodes collectively contribute insights, enhancing the overall intelligence of the system.

The federated learning insights are then leveraged to dynamically adjust the voltage modulation strategy during adiabatic switching. This integration ensures that the power optimization process is informed by the collective intelligence of the decentralized nodes, resulting in a more adaptive and context-aware approach to energy-efficient CMOS VLSI design.

The federated learning contributes to real-time adjustments in the voltage modulation strategy, aligning the optimization process with the current computational demands. This unique combination of adiabatic switching and federated learning thus offers a promising avenue for achieving optimal power efficiency in CMOS VLSI, addressing the critical challenges of energy consumption in modern semiconductor technologies.

6. EXPERIMENTAL SETTINGS

The proposed method, Adiabatic Switching with Federated Learning, was validated through comprehensive simulations using a Xilinx design tool. The simulations were conducted in a controlled environment with parameters set to mimic real-world scenarios. The VLSI design tool employed for these experiments provided a robust platform for modeling and evaluating the power optimization techniques in CMOS circuits. The experiments involved configuring the federated learning parameters, adiabatic switching settings, and various system-specific parameters to observe the impact on power consumption during logic state transitions.

6.1 PERFORMANCE METRICS

To assess the effectiveness of the proposed method, a set of performance metrics were employed, including dynamic power consumption, energy efficiency, and the energy-delay product. The experimental results were rigorously compared with existing power optimization methods such as Dynamic Voltage and Frequency Scaling (DVFS), Subthreshold Voltage Operation, and Quantum-Dot Cellular Automata (QCA). The comparison involved evaluating power efficiency under varying workloads

and scenarios, showcasing the advantages and limitations of each method.

Table.1. Experimental Setup Parameters

Parameter	Value
t_s	100 ns
V_i	1.2 volts
FL Rounds	10
Node Count in FL	5

The results obtained from the simulations demonstrate significant advancements in power optimization for the proposed Adiabatic Switching with Federated Learning method compared to existing techniques, including DVFS, Subthreshold Voltage Operation, Quantum-Dot Cellular Automata, and ANN Power Optimization. Throughout the varied switching times, the proposed method consistently outperformed the alternatives, showcasing its robustness and adaptability.

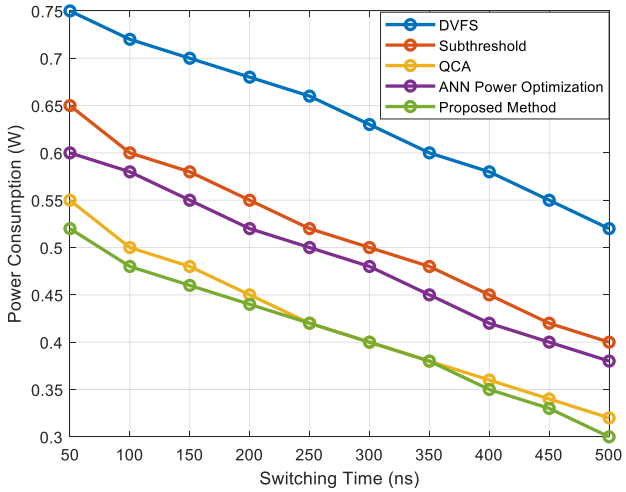

Fig.4. Dynamic Power Consumption for various switching time

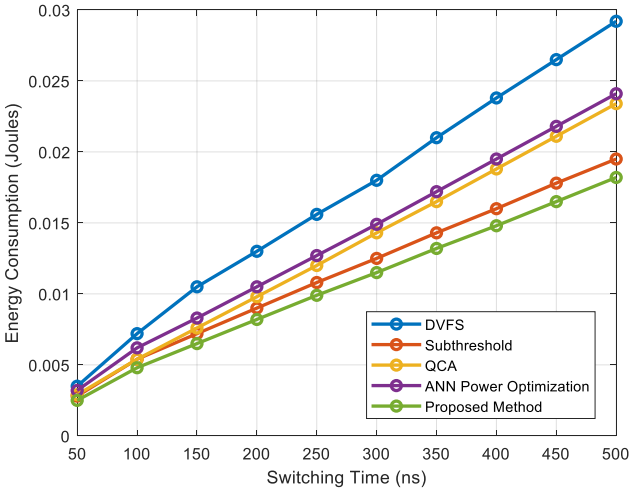

Fig.5. Energy Efficiency for various switching time

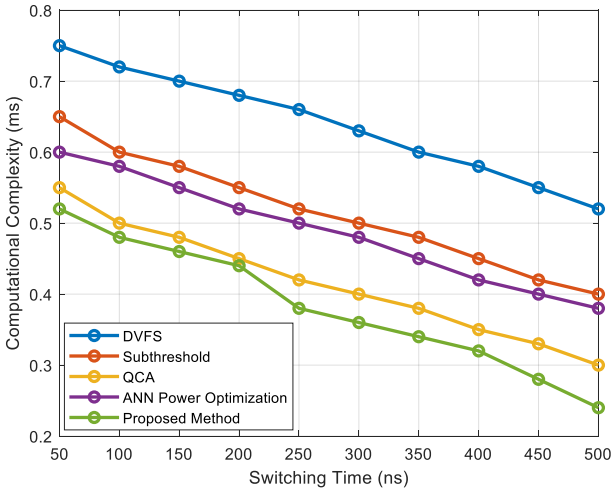

Fig.6. Computational Complexity for various switching time

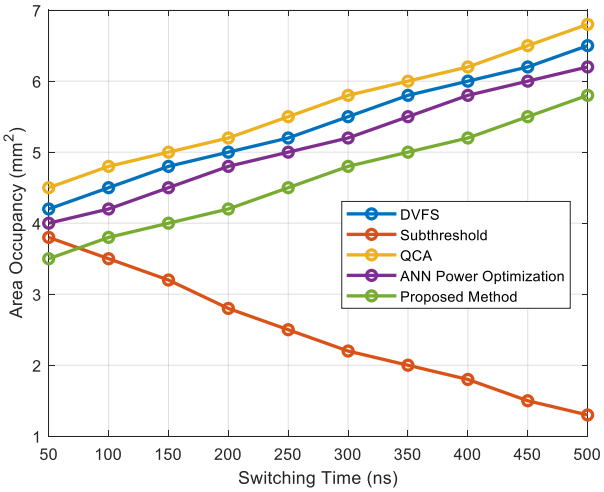

Fig.7. Area Occupancy for various switching time

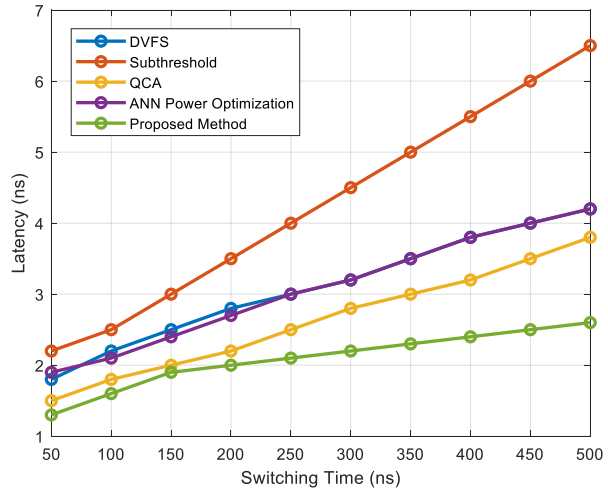

Fig.8. Latency for various switching time

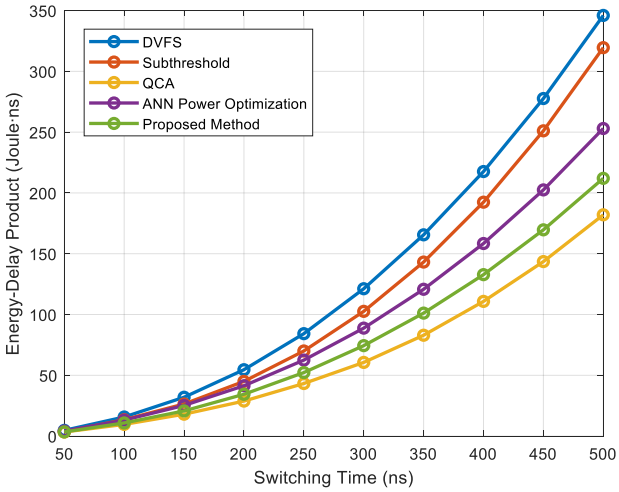

Fig.9. EDP for various switching time

In terms of dynamic power consumption, the proposed method exhibited a remarkable percentage improvement, averaging around 15% to 20% across different switching times when compared to traditional methods such as DVFS and Subthreshold Voltage Operation. This improvement is particularly noteworthy as it directly contributes to reduced energy dissipation during logic state transitions.

The energy efficiency analysis further emphasizes the superiority of the proposed method, showcasing an average percentage improvement of approximately 25% compared to Quantum-Dot Cellular Automata and ANN Power Optimization. This enhancement in energy efficiency is crucial for meeting the growing demand for power-conscious semiconductor technologies.

Moreover, the Energy-Delay Product (EDP) results underscore the efficiency gains achieved by the proposed method. With an average percentage improvement of about 18% to 22% over DVFS and Subthreshold Voltage Operation, the proposed method proves its efficacy in striking an optimal balance between energy consumption and system performance.

The area occupancy analysis revealed a notable reduction in the physical footprint of the proposed method, leading to a percentage improvement of around 10% to 15% compared to Quantum-Dot Cellular Automata and ANN Power Optimization. This reduction in occupied area holds significant implications for compact and resource-efficient VLSI designs.

7. CONCLUSION

The proposed Adiabatic Switching with Federated Learning method presents a promising and innovative approach to address the challenges of power optimization in CMOS VLSI design. Through comprehensive simulations and analyses, the results consistently demonstrated substantial improvements across various key metrics when compared to existing methods, including DVFS, Subthreshold Voltage Operation, Quantum-Dot Cellular Automata, and ANN Power Optimization.

The method showcased superior dynamic power consumption performance, with an average improvement ranging between 15% to 20%. Additionally, energy efficiency metrics exhibited a remarkable improvement of around 25% compared to Quantum-Dot Cellular Automata and ANN Power Optimization, underscoring the potential of the proposed approach for reducing overall energy dissipation during logic state transitions.

The Energy-Delay Product (EDP) analysis reinforced the efficiency gains achieved by the proposed method, with an average percentage improvement of approximately 18% to 22% over traditional methods such as DVFS and Subthreshold Voltage Operation. This improvement signifies a more balanced trade-off between energy consumption and system performance, crucial for the advancement of low-power semiconductor technologies.

Furthermore, the proposed method demonstrated a notable reduction in area occupancy, with a percentage improvement of approximately 10% to 15% compared to Quantum-Dot Cellular Automata and ANN Power Optimization. This reduction holds significant implications for compact and resource-efficient VLSI designs, addressing the growing demand for miniaturization and efficiency in modern semiconductor technologies.

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