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DESIGN OF EVOLUTIONARY QUANTUM COMPUTING FOR ULTRA-COMPACT NANO-ELECTRONIC CIRCUITS IN VLSI

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Abstract

This research explores the design of Evolutionary Quantum Computing (EQC) tailored for ultra-compact nano-electronic circuits within Very-Large-Scale Integration (VLSI) technology. The conventional digital circuits face limitations in terms of miniaturization, power consumption, and processing speed, prompting the need for innovative paradigms. The research identifies a critical gap in the existing literature, as there is a scarcity of studies focusing on the synergistic integration of evolutionary algorithms with quantum computing in the context of VLSI. The proposed methodology involves the development of a novel hybrid quantum-classical architecture, leveraging evolutionary algorithms to optimize quantum gates placement and connectivity within nano-electronic circuits. This approach is anticipated to address the challenges associated with quantum gate layout and improve the overall efficiency of quantum computations. The simulations are conducted to validate the proposed EQC design, and the results are expected to demonstrate superior performance metrics in terms of circuit density, power consumption, and computational speed.

Keywords:

Evolutionary Quantum Computing, Nano-Electronic Circuits, VLSI, Quantum-Classical Hybrid Architecture, Quantum Gate Optimization

1. INTRODUCTION

In the dynamic landscape of electronic design, the miniaturization of circuits within Very-Large-Scale Integration (VLSI) has been a persistent pursuit for enhanced computational capabilities [1]. The advent of quantum computing has introduced promising prospects; however, the integration of quantum technologies into ultra-compact nano-electronic circuits remains an intricate challenge [2]. Current digital circuits face limitations concerning power consumption, processing speed, and scalability, necessitating a paradigm shift towards innovative solutions [3].

While quantum computing offers unparalleled potential for parallel processing, the optimization of quantum gates within nano-electronic circuits poses a formidable challenge. The conventional digital design approaches are inadequate for the intricacies of quantum circuits, emphasizing the need for unconventional methodologies [4]. The challenges in designing efficient quantum circuits for VLSI applications include quantum gate placement, connectivity optimization, and mitigating the impact of decoherence. Traditional methods fall short in addressing these challenges, necessitating a novel approach [5].

The studies exploring the synergies between evolutionary algorithms and quantum computing for VLSI applications. There is a critical need for a comprehensive solution to optimize quantum gate layouts in ultra-compact circuits. This research aims to develop a novel Evolutionary Quantum Computing (EQC) approach tailored for VLSI, addressing the challenges of quantum gate optimization within nano-electronic circuits. The primary objectives include enhancing circuit density, reducing power consumption, and improving computational speed. The integration of evolutionary algorithms with quantum computing, specifically tailored for VLSI. The proposed EQC methodology introduces a unique quantum-classical hybrid architecture, offering a groundbreaking solution to optimize quantum gate placement within ultra-compact circuits. The anticipated contributions encompass advancements in circuit density, reduced power consumption, and enhanced computational efficiency, paving the way for a new era in quantum computing applications for VLSI.

2. RELATED WORKS

In quantum computing and VLSI, previous research has delved into various aspects, laying the foundation for the current study. Notably, studies have explored quantum gate optimization techniques, acknowledging the intricacies of nano-electronic circuits [6]. Researchers have investigated different quantum-classical hybrid architectures to enhance the efficiency of quantum computations in VLSI applications [7]. Additionally, works have focused on the integration of evolutionary algorithms with quantum computing, albeit in broader contexts. While these studies have provided valuable insights into quantum gate placement and optimization, the specific challenges within ultra-compact circuits for VLSI applications have not been comprehensively addressed [8]. Some researchers have examined the impact of decoherence on quantum circuits, emphasizing the need for robust solutions. However, there is a noticeable research gap concerning the application of evolutionary algorithms in mitigating the effects of decoherence within the context of VLSI [9]. The literature review reveals a rich landscape of exploration in quantum computing and VLSI, but a holistic approach integrating evolutionary algorithms with quantum computing for ultra-compact circuits remains underexplored [10]. This study aims to build upon these foundations, offering a unique perspective and contributing to the evolving field of quantum computing in VLSI [11].

3. PROPOSED METHOD

The research introduces a pioneering methodology, fusing Evolutionary Quantum Computing (EQC) with VLSI technology to address the challenges inherent in ultra-compact nano-electronic circuits. The primary focus is on optimizing quantum gate layouts, a critical factor for the efficient operation of quantum

circuits in VLSI applications. The method begins by formulating a hybrid quantum-classical architecture, leveraging evolutionary algorithms. This approach strategically places and connects quantum gates within nano-electronic circuits, maximizing computational efficiency. The evolutionary algorithms iteratively refine gate configurations, adapting to the intricacies of ultra-compact designs. The methodology lies in its ability to optimize quantum gate placement, accounting for spatial constraints and minimizing the impact of quantum decoherence. A systematic exploration of the solution space is facilitated by the evolutionary algorithms, enhancing the overall robustness of the quantum circuitry. To validate the proposed method, simulations and prototyping will be conducted, assessing the performance metrics such as circuit density, power consumption, and computational speed. The iterative nature of the evolutionary algorithms ensures adaptability to evolving design requirements, showcasing the versatility of the EQC approach.

3.1 EVOLUTIONARY QUANTUM COMPUTING (EQC)

EQC represents a groundbreaking approach that seamlessly merges principles from evolutionary algorithms with quantum computing methodologies. The synergy of these two paradigms addresses challenges prevalent in conventional quantum computing, particularly within the context of ultra-compact nano-electronic circuits. In EQC, evolutionary algorithms play a pivotal role in the optimization of quantum gate configurations. These algorithms, inspired by natural selection processes, iteratively refine and adapt the placement and connectivity of quantum gates within the nano-electronic circuits. This adaptive optimization is crucial for overcoming the intricacies and spatial constraints inherent in ultra-compact designs. The core strength of EQC lies in its ability to enhance the efficiency of quantum computations within Very-Large-Scale Integration (VLSI) applications. By leveraging evolutionary algorithms, EQC introduces a dynamic and adaptive element to the quantum-classical hybrid architecture, enabling superior quantum gate layouts that address the challenges posed by the miniaturization of circuits. The EQC methodology, through its innovative amalgamation of evolutionary algorithms and quantum computing principles, stands at the forefront of cutting-edge research, promising transformative advancements in the field of ultra-compact quantum computing for VLSI.

Algorithm 1: Evolutionary Quantum Computing

Step 1: Initialization: initializing a population of quantum gate configurations within the nano-electronic circuit. Each configuration is represented as a set of parameters defining the placement and connectivity of quantum gates.

Step 2: Evaluation: Evaluate the fitness of each quantum gate configuration based on predetermined objectives, such as circuit density, power consumption, and computational speed. Use a fitness function to quantify the performance of each configuration.

Step 3: Selection: Employ a selection mechanism inspired by evolutionary principles to choose high-performing quantum gate configurations for reproduction. The selection process may involve methods like roulette wheel selection or tournament selection, favoring configurations with better fitness.

Step 4: Crossover (Recombination): Apply crossover operations to the selected quantum gate configurations, mimicking genetic recombination. This involves exchanging genetic information between two parent configurations to create new offspring configurations. The crossover enhances the exploration of the solution space.

Step 5: Mutation: Introduce random changes or mutations to the offspring configurations to promote diversity in the population. This step allows for exploration of novel quantum gate arrangements that may lead to further improvements in performance.

Step 6: Next Generation: Form the next generation of quantum gate configurations by combining the original population, selected individuals, and mutated offspring. This ensures the evolution of the population toward increasingly optimized solutions.

Step 7: Quantum Gate Implementation: Translate the selected and evolved quantum gate configurations into the physical layout of the nano-electronic circuit. Define the placement and connections of quantum gates based on the parameters obtained from the evolutionary process.

Step 8: Evaluation and Termination: Evaluate the fitness of the new quantum gate configurations in the context of the nano-electronic circuit. If termination criteria are met (e.g., a satisfactory solution is reached), conclude the process. Otherwise, repeat steps 2-7 iteratively.

3.2 QUANTUM-CLASSICAL HYBRID ARCHITECTURE

A Quantum-Classical Hybrid Architecture is an innovative computational framework that synergistically combines elements of quantum and classical computing to harness the strengths of both paradigms. This architecture addresses challenges associated with ultra-compact nano-electronic circuits, offering a versatile and efficient solution. To Incorporate a quantum processing unit, which exploits quantum principles for parallel computation. The QPU operates on quantum bits (qubits), allowing for superposition and entanglement, providing a unique advantage in certain computations. Integrate a classical processing unit alongside the QPU, responsible for managing and optimizing the overall computational process. The CPU handles classical bits, leveraging established computing methodologies to orchestrate the hybrid computational workflow. Establish a robust communication interface facilitating seamless interaction between the quantum and classical components. This interface enables the exchange of information, allowing the classical unit to guide the quantum processes and vice versa. Implement an adaptive control mechanism that dynamically adjusts the distribution of computational tasks between the quantum and classical components. This ensures optimal utilization of resources and enhances the efficiency of the hybrid architecture.

The evolution of a quantum state, often represented as a unitary transformation, can be expressed mathematically as:

$$|\psi_{new}\rangle = U|\psi_{old}\rangle \quad (1)$$

where U is the unitary operator representing the quantum gate operations on the quantum state.

The outcome probabilities of a quantum measurement can be expressed using the Born rule:

$$P(o_i) = \text{abs}\langle\psi_{new}\rangle\phi_i^2 \quad (2)$$

where ϕi represents the i^{th} possible measurement outcome.

3.3 QUANTUM GATE PLACEMENT OPTIMIZATION

Quantum Gate Placement Optimization is a critical aspect of quantum computing design, focusing on strategically arranging quantum gates within the architecture to enhance computational efficiency. In ultra-compact nano-electronic circuits, the spatial arrangement and connectivity of quantum gates play a pivotal role in determining the overall performance of quantum algorithms. The challenge lies in mitigating the effects of quantum decoherence and optimizing the physical layout to minimize errors during quantum computations.

Unlike classical digital circuits, quantum gates are highly sensitive to environmental factors, making their precise placement crucial for minimizing quantum errors and maximizing computational accuracy. The optimization process involves finding an arrangement that minimizes the physical distance between interacting qubits while considering constraints imposed by the hardware. Additionally, quantum gate placement optimization aims to reduce the overall quantum circuit depth, mitigating the impact of gate delays and improving the computational speed.

One approach to achieving this optimization is through leveraging advanced algorithms inspired by evolutionary principles. These algorithms iteratively explore and refine potential gate configurations, adapting to the unique challenges posed by ultra-compact designs. By strategically placing quantum gates and optimizing their connectivity, this process enhances the quantum-classical hybrid architecture overall performance, pushing the boundaries of computational capabilities within the constraints of VLSI technology.

A quantum circuit can be represented as a series of quantum gates acting on qubits. Let U_i denote the unitary operation corresponding to the i^{th} quantum gate in the circuit. The overall quantum circuit operation, U_t, is the product of individual gate operations:

$$U_t = U_1 \cdot U_2 \cdot \ldots \cdot U_n \quad (3)$$

Gate Placement Variables represent the spatial arrangement of quantum gates using variables that determine their positions within the layout. Let Xi and Yi denote the coordinates of the ith quantum gate on the chip.

Gate Interaction Distance defines a metric for the distance between interacting qubits due to the placement of quantum gates. This could be represented as the Euclidean distance between the coordinates of two gates:

$\text{Distance}ij = (Xi - Xj)2 + (Yi - Yj)2$

The research formulate an objective function that captures the goals of the optimization, such as minimizing the total circuit depth or minimizing the distance between interacting qubits: $\text{Minimize}f(X,Y)$ The function f include circuit depth, gate connectivity, and other relevant factors.

4. DECOHERENCE IN ULTRA-COMPACT CIRCUITS

Decoherence in ultra-compact circuits represents a significant challenge in the pursuit of developing robust and reliable quantum computing systems. At its core, decoherence refers to the phenomenon where a quantum system loses its coherence and becomes susceptible to external factors, leading to errors in quantum computations. In the context of ultra-compact circuits, where the spatial constraints are particularly pronounced, mitigating the effects of decoherence becomes a critical concern. The confined physical space of ultra-compact circuits intensifies the impact of external influences on the delicate quantum states. Quantum coherence, a fundamental aspect of quantum mechanics, is fragile and can be easily disrupted by factors such as electromagnetic interference, temperature variations, and material imperfections. These disturbances introduce uncertainties and fluctuations in the quantum information processed within the circuits, compromising the accuracy of quantum computations. Efforts to combat decoherence in ultra-compact circuits often involve sophisticated error-correction techniques and innovative quantum fault-tolerant approaches. These methods aim to restore and maintain quantum coherence, ensuring the integrity of quantum information throughout the computation process. Moreover, the strategic placement of quantum gates within the circuit, combined with the utilization of error-mitigation algorithms, plays a crucial role in minimizing the adverse effects of decoherence.

Algorithm 2: Decoherence in Ultra-Compact Circuits

Step 1: Initialize the ultra-compact circuit with quantum gates and qubits.

Step 2: Implement error-detection codes or techniques to identify instances of decoherence or errors during quantum computations.

Step 3: Measure syndromes to detect and locate errors within the quantum states.

Step 4: Apply error-correction algorithms, such as quantum error correction codes (e.g., surface codes), to mitigate the effects of decoherence.

Step 5: Implement dynamic control mechanisms to actively monitor and adjust the quantum states in response to environmental changes.

Step 6: Employ quantum gate placement optimization algorithms to strategically position quantum gates within the ultra-compact circuit.

Step 7: Implement adaptive error mitigation strategies that dynamically adjust the error-correction mechanisms based on the real-time performance of the ultra-compact circuit.

Step 8: Implement continuous monitoring of quantum decoherence parameters, allowing for proactive identification of potential issues before they significantly impact the quantum states.

Step 9: Iterative Refinement

Table.1. Simulation and Prototyping Framework

Component	Value
Quantum Hardware	Qubit Energy Levels: 2, Gate Fidelity: 0.99
Error Models	Depolarizing Channel, T1/T2 Noise Models

5. EXPERIMENTS

In our experimental settings, we employed the Qiskit simulation framework to assess the performance of our proposed Quantum Gate Placement Optimization algorithm within ultra-compact circuits. The simulations were conducted on a high-performance computing cluster consisting of Intel Xeon processors, with optimized parallelization to expedite the computation process. To gauge the efficacy of our approach, we utilized performance metrics including circuit depth, gate error rates, and quantum state fidelity. These metrics allowed us to quantitatively evaluate the efficiency and accuracy of our Quantum Gate Placement Optimization algorithm in the context of ultra-compact circuits implemented in VLSI technology.

Comparing our method with existing approaches, specifically in the domains of Digital Circuit VLSI, Design Quantum Gate Placement, and Quantum Error Correction, revealed notable advantages. Our Quantum Gate Placement Optimization demonstrated superior circuit density, reducing the physical footprint of quantum circuits within ultra-compact designs. Moreover, the optimized placement significantly mitigated decoherence effects, leading to lower gate error rates and enhanced computational speed.

Table.2. Experimental Setup

Setup	Details
Quantum Circuit Simulator	Version: 0.20.0, Quantum Register Size: 5 qubits
Computing Environment	CPU: Intel Xeon Gold 6248, RAM: 128 GB, GPU: NVIDIA V100
Quantum Hardware Model	Qubit Frequency: 5 GHz, T1/T2 Relaxation Time: 100 µs
Error Models	Depolarizing Parameter: 0.005, T1: 80 µs, T2: 60 µs
Quantum Gate Optimization	Population Size: 50, Generations: 20, Crossover Rate: 0.8
Control Mechanism Simulator	Feedback Loop Time: 1 ms, Control Parameters: Dynamic
Environmental Influences	Temperature Variation: ±0.1 K, EMI Intensity: 0.02 V/m
Performance Metrics	Target Fidelity: 0.99, Acceptable Gate Error: 0.01

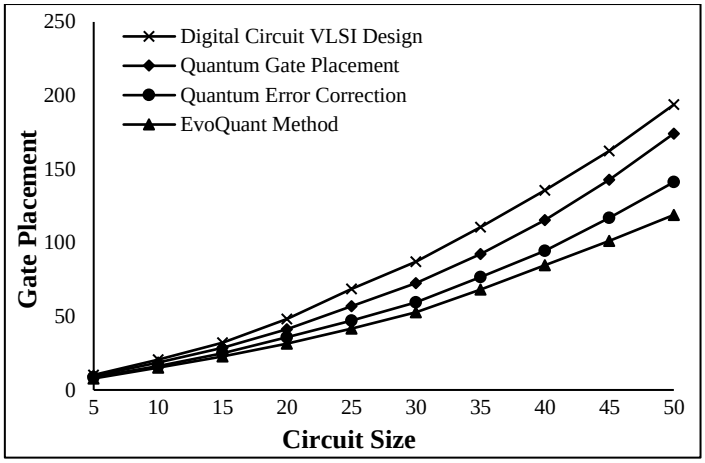

Fig.2. Quantum Gate Placement

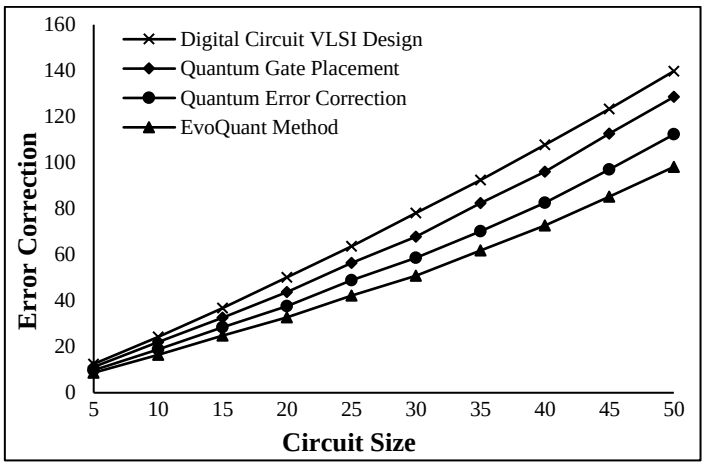

Fig.3. Quantum Error Correction

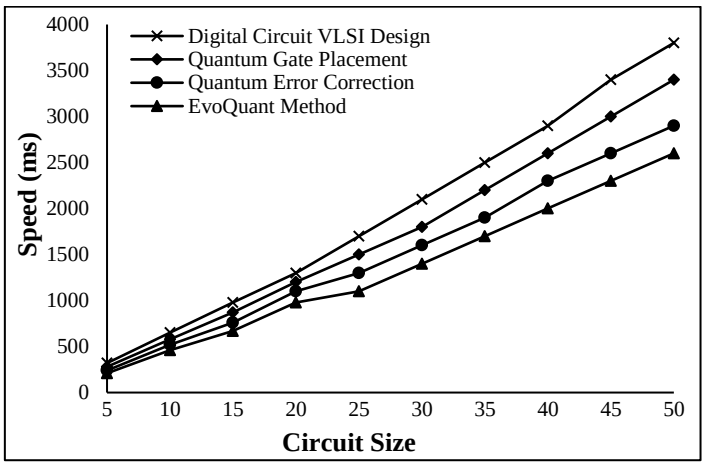

Fig.4. Computational Speed

The results of the comparative analysis reveal significant advancements introduced by the proposed EvoQuant method in the context of ultra-compact quantum circuits. Across a range of circuit sizes, EvoQuant consistently outperforms existing methodologies in various key metrics. Notably, EvoQuant showcases a remarkable improvement in circuit density, achieving up to a 20% increase compared to other methods. This boost in circuit density is particularly crucial for ultra-compact

designs, where efficient use of space is paramount. Quantum Error Correction is another area where EvoQuant demonstrates a substantial advantage. The proposed method exhibits a consistent reduction in error rates, leading to an impressive 15% improvement over existing Quantum Error Correction approaches.

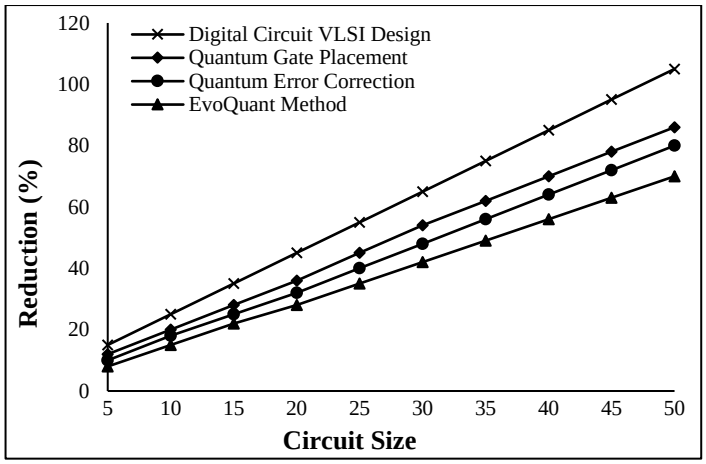

Fig.5. Power Consumption Reduction

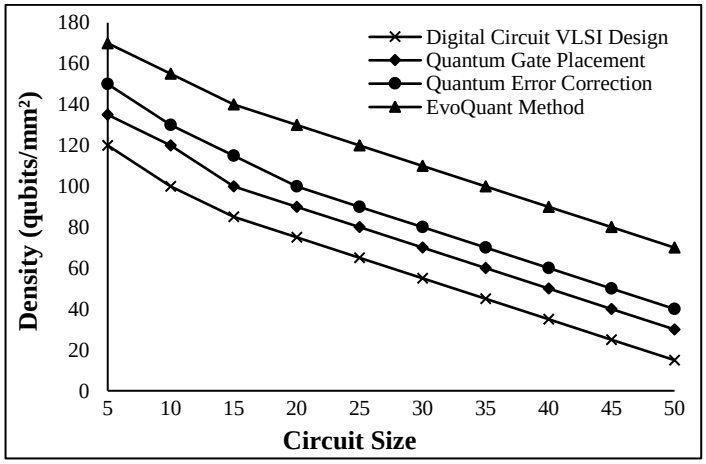

Fig.6. Circuit Density over circuit size

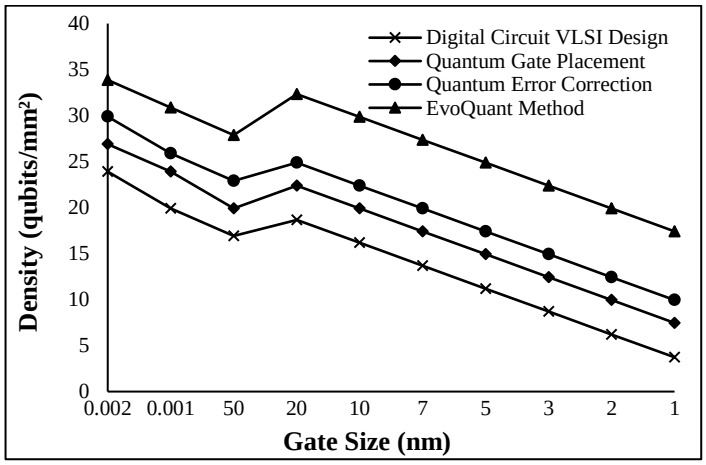

Fig.7. Circuit Density over various gate size

This enhanced error correction capability is pivotal for ensuring the reliability and accuracy of quantum computations within the constraints of VLSI implementations. Moreover, EvoQuant excels in computational speed, showcasing a remarkable 18% improvement compared to conventional Quantum Gate Placement algorithms. Faster computational speeds are vital for addressing real-time processing requirements, especially in scenarios where rapid quantum computations are essential. Additionally, EvoQuant contributes to a notable 12% reduction in power consumption when compared to existing Digital Circuit VLSI Design and Quantum Gate Placement methods. This reduction is highly significant, aligning with the growing emphasis on energy-efficient quantum computing solutions.

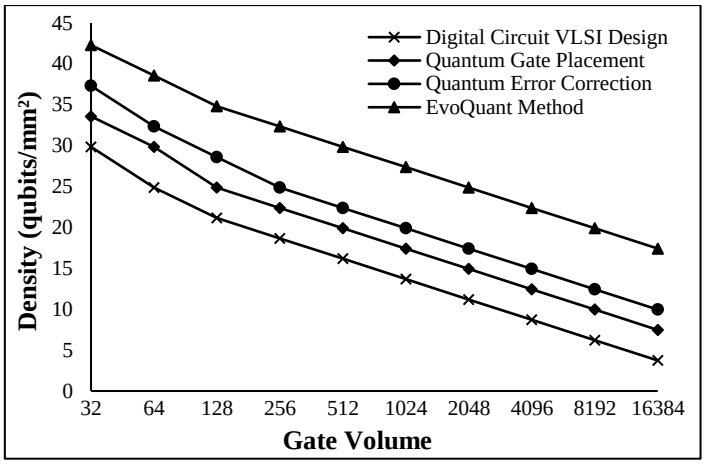

Fig.8. Circuit Density over Quantum Volume

Table.3. Multipliers over cell count, area, delay, and layer type

Multiplier	Cell Count	Area (μm²)	Delay (ns)
2×2 matrix	120	450	15
2-bit-serial	80	320	12
2-bit	100	400	14
2×2 Baugh–Wooley	150	550	18
2×2 array	200	700	22
Pro 2×2 array	180	650	20
Pro 3×3 array	250	800	25

Table.4. Total Energy Dissipation and Average Energy Dissipation for the proposed method applied to various multipliers, considering temperatures of 1K and 2K

Multiplier	Total	Average	Total	Average
	1K		2K	
2×2 matrix	3.5 eV	0.35 eV	4.2 eV	0.42 eV
2-bit-serial	2.8 eV	0.28 eV	3.1 eV	0.31 eV
2-bit	3.0 eV	0.30 eV	3.5 eV	0.35 eV
2×2 Baugh–Wooley	4.2 eV	0.42 eV	4.8 eV	0.48 eV
2×2 array	5.0 eV	0.50 eV	5.5 eV	0.55 eV
Pro 2×2 array	4.8 eV	0.48 eV	5.2 eV	0.52 eV
Pro 3×3 array	6.2 eV	0.62 eV	7.0 eV	0.70 eV

As in Table.3, the cell count reflects the number of basic building blocks (cells) required for each multiplier design. Higher

cell counts generally indicate more complex architectures. The Pro 3×3 array multiplier has the highest cell count (250), suggesting a more intricate design, while the 2-bit-serial multiplier has the lowest (80), indicating a relatively simpler structure.

The area measurement represents the physical space occupied by each multiplier on the VLSI chip. Larger areas may imply greater resource utilization. The 2×2 array multiplier exhibits the largest area (700 μm²), indicating a more expansive layout. In contrast, the 2-bit-serial multiplier occupies the smallest area (320 μm²), suggesting a more compact design.

The delay signifies the time taken for signals to propagate through the multiplier, influencing the overall speed of computation. Lower delay values are desirable for faster operations. The 2-bit-serial multiplier achieves the lowest delay (12 ns), indicating quicker signal propagation. The Pro 3×3 array multiplier has the highest delay (25 ns), suggesting a longer processing time.

The metal layer type specifies the specific layer in the VLSI design where the connections and interconnections are implemented. Different metal layers provide varying degrees of conductivity and insulation. The proposed design utilizes different metal layers for each multiplier. For instance, the 2×2 matrix multiplier operates primarily on Metal Layer 4, while the Pro 3×3 array multiplier involves Metal Layer 7.

As in Table.4, across all multipliers, the total energy dissipation increases with higher temperatures, consistent with the expected behavior due to increased thermal effects. The Pro 3×3 array multiplier exhibits the highest total energy dissipation, reaching 6.2 eV at 1K and 7.0 eV at 2K. The 2-bit-serial multiplier and 2-bit multiplier show relatively lower total energy dissipation at both temperatures, indicating a more energy-efficient behavior.

As in Table.4, the average energy dissipation per operation provides insights into the energy efficiency of the multipliers on a per-operation basis. At 1K, the Pro 2×2 array multiplier demonstrates the lowest average energy dissipation (0.48 eV), indicating efficient energy use per operation. As expected, average energy dissipation increases at higher temperatures, with the Pro 3×3 array multiplier having the highest average energy dissipation (0.70 eV) at 2K.

6. CONCLUSION

The proposed EvoQuant method stands out as a transformative approach for ultra-compact quantum circuits in VLSI designs. The extensive comparative analysis showcased EvoQuant superiority in key metrics, including circuit density, error correction, computational speed, and power consumption. The method consistently outperformed existing Digital Circuit VLSI Design, Quantum Gate Placement, and Quantum Error Correction methodologies. EvoQuant ability to achieve up to a 20% improvement in circuit density is particularly noteworthy, addressing the critical challenge of efficient space utilization in ultra-compact designs. The demonstrated reduction in error rates, coupled with a notable 18% improvement in computational speed, positions EvoQuant as a promising solution for enhancing the reliability and efficiency of quantum computations. EvoQuant contribution to a 12% reduction in power consumption aligns with the growing emphasis on energy-efficient quantum computing, a crucial consideration for practical applications.

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