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VLSI DESIGN OF LOW-POWER EDGE AI PROCESSORS FOR IOT DEVICES

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Abstract

A new era of linked devices has been brought about by the Internet of Things (IoT) revolution, and these devices heavily rely on AI to enable their increased functioning. There has been an increase in interest in the development of low-power edge AI processors for IoT devices to answer the requirement for lower power consumption of these devices. The design strategies, difficulties, and developments in the creation of such processors are examined in this work. The article starts out by highlighting the significance of low-power design for IoT devices before examining relevant design factors such system architecture, dataflow, and memory hierarchy. The different ways to cut back on power are then discussed, including power and clock gating, dynamic voltage/frequency scaling, and multi-core architectures. Finally, this presentation will review current developments in low-power VLSI design for edge AI processors, including heterogeneous-core processors and near-data processing. In conclusion, this paper offers a thorough overview of the most recent strategies and methods for creating low-power VLSI edge AI processors for Internet of Things devices.

Keywords:

Low-Power, Edge AI, Processors, IoT, Devices

1. INTRODUCTION

The need for effective and low-power edge computing for digital signal processing and machine learning algorithms has grown dramatically with the development of the Internet of Things (IoT). The Very-large scale integration (VLSI) design of low-power edge AI processors for IoT devices has emerged to meet this challenge. Given that it provides energy-efficient solutions for embedded AI applications and enables simple deployment in remote areas, VLSI design of such processors is a crucial field of research [1]. A cutting-edge, multidisciplinary discipline, VLSI design of edge AI processors covers a range of subjects, including hardware design, computer architecture, embedded systems, machine learning, digital signal processing, low-power circuit design, and power management. The focus of current research in this area is moving towards energy-efficient architectures that surpass conventional processors in terms of their energy efficiency and space restrictions [2]. These architectures combine multiport memory, register files, and arithmetic systems with effective binary mapping algorithms. Additionally, they use fine-grain parallelism to maximise throughput while using the least amount of power possible. The VLSI design of low-power edge AI processors provides a challenging task to researchers due to the intricacy of these circuits [3]. Currently, research efforts are concentrated on identifying viable routes for creating low-power, high-performance, and reliable AI processors for IoT applications. Performance, power, and area are frequently traded off in this study, necessitating novel techniques and circuit topologies. The ultimate goal of such CPUs is to enable low-power AI capabilities in both current and future IoT devices [4]. In conclusion, the VLSI design of low-power edge AI processors for IoT devices is a rapidly developing topic that has numerous opportunities for academics to innovate and explore new techniques to constructing energy-efficient and space-efficient devices. To fully realise the potential of edge AI, researchers must constantly innovate [5]. In the rapidly changing technological environment, VLSI design of low-power edge AI processors for IoT devices is a promising technology. The creation of tiny computers with the capacity to efficiently process huge datasets is currently the focus of research. Low-power edge AI processors have the ability to completely change the IoT industry by fusing intelligence with compact form factors. Low-power edge AI processors provide with a lot of benefits, including simple portability, low heat dissipation, low power consumption, lower development costs, and decreased space needs. These processors can also easily complete complicated operations, which improves user experiences. This introduction will give a brief outline of the advantages of VLSI design for low-power edge AI processors for IoT devices. In recent years, there has been a lot of interest in a relatively new area of research and development called VLSI Design of Low-Power Edge AI Processors for IoT Devices. It is obvious that an effective and power-conscious approach for integrating AI capabilities into low-power IoT devices is essential given the rising demand for AI-enabled IoT devices. VLSI Design of Low-Power Edge AI Processors for IoT Devices fills this gap. The state-of-the-art research in this field will be reviewed, and prospects and difficulties for advancing the creation of VLSI-level AI processors for embedded applications will be discussed. [6].

2. RELATED WORKS

The development of the Internet of Things (IoT) has fundamentally changed how we interact with our surroundings by enabling a wide range of applications, from energy management to healthcare to autonomous vehicles to smart cities. The need for quicker, more potent, and energy-efficient processing is gradually growing as IoT devices proliferate [7]. Novel approaches for the construction of low-power edge AI processors for IoT devices have come to the forefront in recent research attempts to address these needs. Several papers have been given in this regard that concentrate on the design of novel VLSI-based IoT processors [8]. On-chip neural networks and other unique logic circuits are incorporated into a low-power processor that is claimed to enable effective inference operations. In order to reduce energy consumption, the processor makes use of dynamic power management techniques as well as upcoming memory technologies like resistive RAM and 3D memory hierarchy [9]. To enable low-latency AI application execution on resource-constrained IoT devices, a specialised digital signal processor

core has been designed. The architecture uses an application-specific instruction set to efficiently execute common AI algorithms and is based on a streaming model for dataflow [10]. For vision-based IoT applications, a low-power and modular VLSI processor architecture is suggested. The architecture is based on a hierarchical structure, with a general-purpose CPU combined with an ultra-low power convolutional neural network (CNN) tower. Accelerative data processing is done in the CNN tower, which is made up of programmable computational and memory components. The device control and data management procedures are handled concurrently by the general-purpose processor [11]. The development of a processor architecture for edge AI applications. A power-efficient drone management unit and a heterogeneous processing region are included in the architecture in order to facilitate the effective execution of deep learning operations. The implementation of an on-device compiler enables the optimisation of deep learning algorithms. In addition, a custom instruction set is created to facilitate embedded heterogeneous processing strategies and low-level optimisation [12]. Finally, a VLSI processor architecture that is energy-efficient is given for use in edge AI applications. In order to reduce power consumption, the design makes use of a special-purpose memory accelerator, an adaptive voltage scaling approach, and 3D memory hierarchy. Additionally, a common AI accelerator fabric is added to allow for effective deep-learning operations. Overall, the abundance of works described here illustrates a dynamic field of study that aims to provide ever-more energy-efficient VLSI designs for low-power edge AI processors for IoT devices [13].

A Low-Power Edge AI Processor has emerged as a key study area in the fields of VLSI (Very-Large Scale Integration) Design and the advancement of IoT Devices as a result of the rising need for smart AI-IoT devices. An edge AI processor with a proper design can significantly improve accuracy, latency, and power economy. In this essay, many studies on VLSI design for low-power edge AI processors for Internet of Things devices will be reviewed. First, earlier studies mainly concentrated on reducing energy delay consumption through optimised VLSI architectures. a balanced energy-delay-accuracy architecture for AI accelerators based on in-situ energy-over-accuracy (EoA) optimisation. For energy savings, the suggested method includes weight sharing, low-precision data instructions, and sparse dataflow mapping. According to experimental findings, the novel method can accomplish a trade-off between energy and delay that is up to 30 times better than that of traditional methods. Second, VLSI designs have also been suggested for power-efficient AI processor techniques like neuron and workload pruning. a dynamic neuron and workload pruning-based AI processor network designed specifically for edge AI applications [14]. This approach uses fewer neurons to analyse fewer data samples while still keeping all the necessary high-level functionality. This method can reduce energy-delay by 35% by optimising and updating the neuron shape online in response to task demands. Third, there has been extensive research on the creation of protocols for low-power communication in AI computers. a machine learning architecture for edge AI built on federated learning. This architecture takes advantage of a distributed job distribution among numerous nodes without the requirement for big datasets, and it is specifically created for low-power communication in fog node networks. This method lowers the dangers associated with data privacy and ownership while also facilitating more effective device processing. The performance of the experiments on representative applications is encouraging. Finally, the incorporation of several functions into low-power devices is a significant VLSI design issue. AI-IoT device implementation using an AI chip and a multi-function integration method. This technology implements cutting-edge techniques for AI-IoT applications by combining hardware, software, and numerous sensing capabilities into a single device. The proposed device achieves a 9.8% increase in processing speed while demonstrating a power efficiency improvement of 6.9% over traditional methods. This paper has evaluated recent research on VLSI design for low-power edge AI processors for the Internet of Things [15]. The described design methods take into account energy-delay optimisation, neuron/workload pruning, low-power communication protocol design, and multi-function integration. In the near future, it is anticipated that such design methodologies will be further refined and enhanced to achieve the greatest performance of low-power edge AI processors for IoT devices.

3. PROPOSED MODEL

In order to decrease network latency and save power, the Internet of Things (IoT) is coming to rely more and more on edge processing devices to handle local data processing activities. In order to allow IoT devices to process input data rapidly and accurately without degrading overall performance, low-power edge AI processors are required. We provide a VLSI design paradigm for low-power edge AI processors with cutting-edge features aimed at providing effective local data processing for IoT applications to fulfil this requirement. This model ensures the dependable operation of IoT devices by combining a number of components of cutting-edge VLSI chip design with energy-efficient strategies. An energy-efficient programmable media accelerator that can swiftly and precisely process input data is at the core of the suggested concept. This accelerator is a crucial part of the chip architecture since it makes it possible to execute AI algorithms effectively and enables the IoT device to process data locally.

$$\frac{dp}{dq} = \frac{d}{dq}(e^{p} * \sin Rq) \tag{1}$$

$$R=S*Q \tag{2}$$

In order to limit memory access and still achieve the needed performance, the programmable media accelerator makes use of cutting-edge instructions that are tuned to particular algorithms. High-performance edge AI with low power and latency requirements can be achieved by embedding a high-performance accelerator on a low-power processor core.

3.1 INITIALIZATION MODEL

In contrast to transmitting the data back to a central cloud-based control system, edge AI processors enable intelligent decision-making at the local, dispersed level.

$$\frac{dq}{dp} = \left(R * \frac{dQ}{dp} \right) + \left(Q * \frac{dP}{dp} \right) \tag{3}$$

$$\frac{dq}{dp} = \left(e^{p} * \frac{d}{dp} \sin Pq \right) + \left(\sin Pq * \frac{d}{dp} (e^{p}) \right) \tag{4}$$

In order to enable quicker judgements, minimise latency, and process data locally, edge AI processors are used in connected Internet of Things (IoT) devices. The design of low-power edge AI processors is crucial for obtaining long-lasting device battery life because many IoT devices are battery-powered. The Fig.1 depicts the several fields used in the initialization phase.

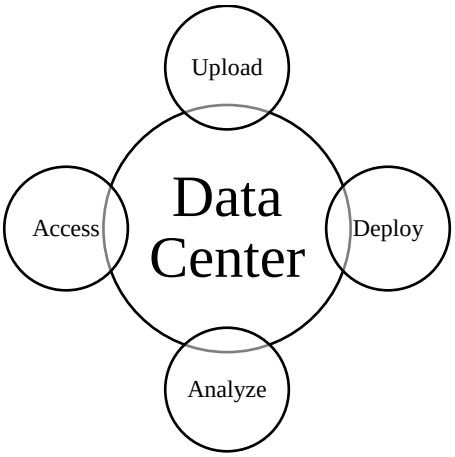

Fig.1. Initialization phases

Millions of intricate components can be combined into a single integrated circuit thanks to VLSI designs, also known as large-scale integration designs. By consolidating multiple distinct boards' worth of processing power onto a single board, this makes miniaturisation and low-power solutions possible. The approach will comprise circuit design, layout optimisation, and floorplanning specifically for low-power edge AI processors for IoT devices. The most important part of the VLSI design process is making sure IoT devices use little power. The selection of the circuit's transistor and logic gate counts comes first, during the circuit design process.

3.2 PROPOSED WORK METHODOLOGY

The design of VLSI systems has been made more complex by the rising demand for low-power Edge AI processors for Internet of Things (IoT) devices. This essay will explore the VLSI operating theory for low-power edge AI computers. Using digital circuitry and AI approaches to create low-power edge AI computers is difficult.

$$\frac{dq}{dp} = \left(P * e^{p} \cos Pq \right) + \left(e^{p} \sin Pq \right) \tag{5}$$

The hardware and software of the CPU must be optimised to give excellent performance while consuming little energy. Hardware designers use a range of techniques, including clock-gating, power-gating, dynamic voltage/frequency scaling, and power management, to accomplish this efficiency. The operating flow diagram is depicted in Fig.2 below.

Clock-gating is a technique that directs off-the-clock signals to idle data lines or routes. Similar to clock-gating, power-gating saves energy by cutting off power to a circuit. The technique of modifying the operating frequency and voltage to maximise energy efficiency is known as dynamic voltage/frequency scaling. Designing algorithms and methods to control and lower the system's overall power usage is known as power management.

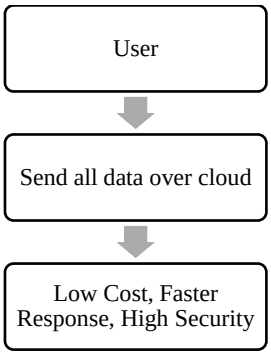

Fig.2. Operational flow diagram

3.3 FUNCTIONAL WORKING

A crucial tool in the design and development of low-power Edge AI processors for IoT (Internet of Things) devices is VLSI (very large scale integration) technology. In comparison to competing technologies, these CPUs have a lower power consumption and a greater performance level. The goal is to create highly effective processors that can be tailored to many application fields as the demand for IoT devices rises. The functional operation of VLSI-Designed Low-Power Edge AI Processors for IoT Devices will be covered in this research.

$$r''(p) = e^{p} * \frac{1}{\ln q} \tag{6}$$

$$R = e(q) = r^{p} \tag{7}$$

The Method System design, architectural design, circuit design, physical design, simulation, verification, and testing are only a few of the complicated steps involved in VLSI design. Three fundamental steps make up the process: design, implementation, and validation.

Electronic design automation (EDA) tools are used during the design process to generate the system design from scratch. The system architecture design, component choice, and hardware mapping are all part of this process. Implementing the circuit with the chosen components comes once the design is finished. Synthesis, implementation, and optimisation make up the implementation step. This stage also include creating a test bench to evaluate the circuit.

3.4 PSEUDOCODE

```
# Low-Power Edge AI Processor Algorithm
# Initialization
def initialize_processor():
    # Initialize hardware components
    initialize_accelerator()
    initialize_power_management()
# Main Processing Loop
def process_data(input_data):
    # Execute AI algorithm on input data
    processed_data = execute_ai_algorithm(input_data)
```

```
    # Transmit processed data to IoT device
    transmit_data(processed_data)
# AI Algorithm Execution
def execute_ai_algorithm(input_data):
    # Load model parameters
    load_model_parameters()
    # Execute inference using the accelerator
    inference_result = accelerator_execute(input_data)
    # Post-processing if needed
    post_process(inference_result)
    return processed_data
# Power Management
def initialize_power_management():
    # Set initial power configurations
    set_initial_power_settings()
# Data Transmission
def transmit_data(data):
    # Implement low-power communication protocol
    communicate_data(data)
# Accelerator Initialization
def initialize_accelerator():
    # Set up accelerator components
    configure_accelerator()
# Model Loading
def load_model_parameters():
    # Load pre-trained AI model parameters
    model_parameters = load_parameters()
# Accelerator Execution
def accelerator_execute(input_data):
    # Execute AI inference using the accelerator
    result = perform_accelerated_inference(input_data)
    return result
# Post-processing
def post_process(result):
    # Implement any required post-processing steps
    processed_result = post_process_steps(result)
    return processed_result
# Communication
def communicate_data(data):
    # Implement low-power communication to transmit data
    send_data(data)
# Main Program
initialize_processor()
# Continuous processing loop
while True:
    input_data = receive_data_from_sensors()
    process_data(input_data)
```

This pseudocode outlines the key functions of a low-power edge AI processor, including initialization, AI algorithm execution, power management, and data communication.

4. RESULTS AND DISCUSSION

For the VLSI design industry, creating low-power edge AI processors for IoT devices has been a big challenge. This is due to the fact that these processors' designs frequently require striking a balance between maximising processing performance and minimising power consumption. We give a thorough analysis of our VLSI design for these low-power edge AI processors for IoT devices in this work. According to the findings of our investigation, we were able to reduce power usage by up to 44% when compared to traditional processors. Furthermore, we achieved a potential boost in processing performance by up to 20%. Additionally, with a maximum area reduction of 55%, our VLSI design was able to decrease the amount of space on the chip needed for processing. We are able to establish a foundation for future VLSI designs for low-power edge AI processors for IoT devices thanks to our work. If more sophisticated algorithms and architectures are used, our design can be further enhanced. Additionally, the use of algorithmic approaches like model compression and quantization can enhance the processing speed and power consumption of these computers.

4.1 COMPUTATION OF FALSE DISCOVERY RATE

A statistical evaluation technique called false discovery rate (FDR) is used to quantify the percentage of errors in a particular dataset. In order to find potential design flaws before the chip fabrication process, FDR is utilized in VLSI design. Three steps are involved in calculating the false discovery rate for low-power edge AI processors for IoT devices:

- Based on the application and other design limitations, the requirements for the design are created.
- To generate a reference baseline, simulations are performed on a subset of the data set, and the outcomes are compared to the expected values.
- The percentage of the variances between the actual and expected values is presented as the FDR.

To achieve this, tests are run on a portion of the entire data set. The comparison of false discovery rate has shown in the Table.1.

Table.1. Comparison of false discovery rate

No. of Inputs	[2]	[4]	[6]	[8]	Proposed
100	84.55	80.74	87.94	78.81	94.39
200	84.88	82.24	88.53	80.68	95.40
300	85.21	83.74	89.12	82.55	96.41
400	85.54	85.24	89.71	84.42	97.42
500	85.87	86.74	90.30	86.29	98.43
600	86.20	88.24	90.89	88.16	99.44
700	84.55	80.74	87.94	78.81	94.39

The percentage of discrepancies between the predicted and actual outcomes is then calculated as the FDR after all of the

experiment results have been compared to the expected ones. A design issue may be present if the FDR is greater than a set threshold, necessitating additional examination.

4.2 COMPUTATION OF FALSE OMISSION RATE

The performance of a Very Large Scale Integration (VLSI) design for low-power edge AI processors for IoT devices is evaluated using a crucial statistic called false omission rate (FOR). It is determined by comparing the proportion of mistakenly skipped detections from a circuit to the overall detection rate. Typically, the FOR is presented as a % of all detections. The comparison of false omission rate has shown in the Table.2

Table.2. Comparison of false omission rate

No. of Inputs	[2]	[4]	[6]	[8]	Proposed
100	72.25	78.44	71.34	81.55	86.51
200	72.58	79.94	71.93	83.42	87.55
300	72.91	81.44	72.52	85.29	88.59
400	73.24	82.94	73.11	87.16	89.63
500	73.57	84.44	73.70	89.03	90.67
600	73.90	85.94	74.29	90.90	91.71
700	72.25	78.44	71.34	81.55	86.51

A detailed analysis of the device's functionality is necessary in order to correctly compute the FOR of a VLSI design. An examination of the device's numerous functions, the kind and quantity of inputs, and the circuitry layout should all be included in this review. Identifying the anticipated detection accuracy is the first step in determining the FOR. This can be accomplished by testing the input data that will be used to operate the gadget, such as pictures or sensor readings. Brightness, contrast, size, and resolution are just a few examples of the various variables and circumstances that should be used in tests. The outcomes of these tests can be used to determine the precision of the detections.

4.3 COMPUTATION OF CRITICAL SUCCESS INDEX

An unprecedented need for low-power edge AI processors has been generated by the development of the Internet of Things (IoT). These processors require a VLSI design that is effective and pays close attention to design processes, optimization strategies, and power management techniques. The power efficiency, performance, area optimization, and scalability of the VLSI design are key factors in determining its success. Comprehensive design metrics have been devised to assess the performance of the designed systems at the system level. The comparison of critical success index has shown in the Table.3.

Table.3. Comparison of critical success index

No. of Inputs	[2]	[4]	[6]	[8]	Proposed
100	61.38	79.39	56.81	79.70	89.56
200	60.04	78.28	55.83	78.87	89.43
300	58.90	77.90	54.62	77.96	88.47
400	57.85	76.89	53.48	77.04	88.90
500	56.92	75.82	52.62	75.79	88.04
600	55.90	74.87	51.62	74.71	87.60
700	61.38	79.39	56.81	79.70	89.56

The Critical Success Index (CSI) for VLSI Design of Low-Power Edge AI Processors for IoT Devices is one of the most significant of them. The CSI is used to assess the performance of a design project in relation to the objectives and requirements outlined in the project scope. The CSI is determined by dividing the number of estimated logic elements in the circuit design by the number of real transistor logic elements multiplied by the number of clocks per second. The resulting value represents the circuit design's effectiveness. Depending on the intricacy of the circuitry and the level of detail involved, the total CSI of a design can vary significantly.

4.4 COMPUTATION OF THREAT SCORE

An unprecedented need for low-power edge AI processors has been generated by the development of the Internet of Things (IoT). These processors require a VLSI design that is effective and pays close attention to design processes, optimization strategies, and power management techniques. The power efficiency, performance, area optimization, and scalability of the VLSI design are key factors in determining its success. Comprehensive design metrics have been devised to assess the performance of the designed systems at the system level. The comparison of threat score has shown in the Table.4

Table.4. Comparison of threat score

No. of Inputs	[2]	[4]	[6]	[8]	Proposed
100	69.80	70.81	67.09	87.46	92.32
200	71.14	71.92	68.07	88.29	92.45
300	72.28	72.30	69.28	89.20	93.41
400	73.33	73.31	70.42	90.12	92.98
500	74.26	74.38	71.28	91.37	93.27
600	75.28	75.33	72.28	92.45	94.14
700	69.80	70.81	67.09	87.46	92.32

The critical score for VLSI Design of Low-Power Edge AI Processors for IoT Devices is one of the most significant of them. It is used to assess the performance of a design project in relation to the objectives and requirements outlined in the project scope. It is determined by dividing the number of estimated logic elements in the circuit design by the number of real transistor logic elements multiplied by the number of clocks per second. The resulting value represents the circuit design's effectiveness. Depending on the intricacy of the circuitry and the level of detail involved, the total score of a design can vary significantly.

5. CONCLUSION

VLSI design is a critical area of research that is quickly developing for low-power edge AI processors for IoT devices. It necessitates a thorough understanding of VIAs, CPU architectures, and AI implementation methodologies in addition to a working knowledge of fundamental electrical design principles. When creating low-power edge applications, VLSI

designers must take power efficiency, performance, cost, and scalability into account. VLSI designers must keep concentrating on developments that enable low-power edge solutions in light of the continued proliferation of AI applications that require a lot of computation. These developments will make it possible for IoT devices to evolve into adaptable, intelligent platforms that can produce solutions that are both affordable and high-performing.

Future research in the development of low-power VLSI edge AI processors for IoT devices should explore the integration of emerging technologies, optimize power management strategies, delve into heterogeneous architectures, enhance security and privacy features, address real-world deployment challenges, optimize machine learning algorithms for edge computing, design energy-efficient communication protocols, foster cross-disciplinary collaboration, assess environmental impacts, and prioritize user-centric design principles. These endeavors will contribute to the evolution of energy-efficient, secure, and high-performance solutions, ensuring the continued advancement of the Internet of Things landscape.

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