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# BALANCING COST AND PERFORMANCE IN VLSI SYSTEMS USING RMSPROP ALGORITHM-ASSISTED DESIGN SPACE EXPLORATION

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***Abstract***

***As Very Large Scale Integration (VLSI) technology advances, the need to efficiently balance cost and performance in VLSI systems becomes paramount. To address this challenge, we propose a novel approach that leverages the RMSPROP algorithm for assisted design space exploration. The RMSPROP algorithm, which has proven effective in the field of deep learning optimization, is adapted to navigate the complex design space of VLSI systems. By integrating RMSPROP into the design space exploration process, we can intelligently search for optimal trade-offs between cost and performance, leading to highly efficient VLSI designs. Our experimental results demonstrate the effectiveness of the RMSPROP algorithm-assisted design space exploration, showcasing significant improvements in cost-performance trade-offs compared to traditional design methodologies. This research opens new avenues for designing VLSI systems with improved efficiency, enabling the realization of high-performance yet cost-effective integrated circuits.***

***Keywords:***

***VLSI Systems, RMSPROP Algorithm, Design Space Exploration, Cost-Performance Trade-Offs***

## 1. INTRODUCTION

In recent years, the demand for high-performance and cost-effective Very Large Scale Integration (VLSI) systems has surged, driven by the rapid growth of modern technologies such as artificial intelligence, Internet of Things (IoT), and cloud computing. VLSI systems, comprising intricate integrated circuits (ICs), form the backbone of numerous electronic devices and play a pivotal role in shaping technological advancements [1]. However, designing VLSI systems that strike an optimal balance between performance and cost remains a significant challenge, given the increasing complexity and scale of these systems [2].

Traditional VLSI design methodologies often rely on manual exploration of the design space to identify suitable trade-offs between performance metrics, such as speed and power consumption, and the cost of fabrication. As the design space becomes increasingly vast and intricate, manual exploration becomes impractical and time-consuming, hindering the discovery of optimal solutions [3]. Consequently, there is a pressing need for innovative approaches that can efficiently navigate the design space, leading to the development of VLSI systems that maximize performance while minimizing costs [4].

We propose a pioneering approach that harnesses the power of the RMSPROP algorithm to facilitate design space exploration for VLSI systems. The RMSPROP algorithm, initially designed for optimizing deep learning models, demonstrates remarkable efficiency in finding convergence paths while efficiently handling the variance of gradients. By adapting RMSPROP to the VLSI domain, we aim to address the challenge of balancing cost and performance in VLSI systems.

The primary objective of this research is to present a systematic and effective framework that combines the RMSPROP algorithm with design space exploration techniques to efficiently explore the vast solution space of VLSI systems. Through this integration, we seek to uncover a range of design options that offer favorable trade-offs between performance metrics and fabrication costs, thus enabling the development of high-quality VLSI systems with enhanced efficiency and cost-effectiveness.

## 2. RELATED WORKS

Various research efforts have been dedicated to exploring design space exploration techniques for VLSI systems. These studies often focus on optimization algorithms, evolutionary strategies, and multi-objective optimization methods to efficiently search for optimal design points in the vast solution space. While these approaches have shown promising results, there is still a need for novel methodologies that can handle the increasing complexity and size of modern VLSI systems [5].

In the field of deep learning, optimization algorithms like RMSPROP, Adam, and stochastic gradient descent (SGD) have been extensively studied to train complex neural networks efficiently. These algorithms address challenges such as convergence speed, handling large-scale datasets, and alleviating the problem of vanishing or exploding gradients. Drawing inspiration from the success of these algorithms, researchers have started exploring their adaptability to other domains, including VLSI design [6].

The trade-offs between cost and performance are critical considerations in VLSI system design. Researchers have examined various techniques to optimize power consumption, chip area, clock frequency, and other performance metrics, while still adhering to stringent cost constraints. These studies often utilize analytical models, heuristics, or machine learning approaches to find the best compromise between performance and cost [7].

Machine learning techniques have been increasingly employed in VLSI design to automate various tasks, such as layout generation, optimization, and synthesis. Reinforcement learning, genetic algorithms, and neural architecture search are some of the machine learning-based methods used for exploring the design space and improving the efficiency of VLSI [8].

Several research efforts have focused on developing methodologies that streamline the VLSI design process, reduce design time, and enhance overall productivity. These methodologies often incorporate intelligent algorithms and

automation techniques to achieve better performance with fewer resources [9].

The hardware-software co-design aims to optimize the interaction between hardware and software components in a system. Researchers have explored co-design techniques that allow better utilization of hardware resources while achieving high-performance results, ultimately contributing to cost-efficient VLSI systems [10].

Studies examining the most recent advancements in VLSI systems and integrated circuits are essential for understanding the current state of the art. These works often serve as benchmarks for evaluating the efficacy of new design methodologies, including the proposed RMSPROP algorithm-assisted design space exploration approach [11].

By studying these related works, we can gain insights into the existing challenges and solutions in VLSI design, paving the way for our novel approach to balance cost and performance using the RMSPROP algorithm for design space exploration.

# 3. PROPOSED COST-EFFECTIVE DESIGN

The proposed methodology aims to address the challenge of balancing cost and performance in VLSI systems by leveraging the RMSPROP algorithm for assisted design space exploration. This innovative approach combines principles from the fields of deep learning optimization and VLSI design to efficiently navigate the complex design space and identify optimal trade-offs between various performance metrics and fabrication costs. The key components of the proposed methodology are as follows:

## 3.1 DESIGN SPACE EXPLORATION USING RMSPROP

The heart of the methodology lies in the adaptation of the RMSPROP algorithm, originally designed for deep learning optimization, to the context of VLSI design. The RMSPROP algorithm demonstrates remarkable efficiency in dealing with the variance of gradients and efficiently converging to optimal solutions. By utilizing RMSPROP for design space exploration, we can effectively search the vast solution space of VLSI systems, efficiently evaluating and adjusting design parameters.

Design space exploration using RMSPROP involves adapting the RMSPROP algorithm, originally designed for deep learning optimization, to navigate the design space of VLSI systems efficiently. The goal is to iteratively update the design parameters to find optimal trade-offs between various performance metrics and fabrication costs. The core idea behind RMSPROP is to adjust the learning rate for each parameter based on the historical gradient information, which allows for faster convergence and handling of gradient variance. The update of RMSPROP for a parameter $\theta$ at iteration $t$ is given as follows:

$$v_t = \rho \cdot v_{t-1} + (1 - \rho) \cdot g_t^2$$

$$\Delta\theta_t = -\frac{\eta}{\sqrt{v_t + \varepsilon}} \cdot g_t$$

where:

$v_t$ is the moving average of squared gradients for parameter $\theta$ at iteration $t$.

$\rho$ is the decay rate (usually set to a value close to 1, e.g., 0.9) that controls how much the algorithm remembers past gradients.

$g_t$ is the gradient of the loss function with respect to parameter θ at iteration $t$.

$\eta$ is the learning rate, which determines the step size in the parameter space.

$\varepsilon$ is a small constant (e.g., $1e^{-8}$) added to the denominator for numerical stability.

RMSPROP is applied to design space exploration in VLSI:

**Step 1**. Initialization: Start with initial design parameters $\theta$ and set the moving average of squared gradients $v_0$ to zero.

**Step 2**. Iterative Update: At each iteration $t$, evaluate the performance metrics and cost constraints for the current design point determined by $\theta$.

**Step 3**. Compute Gradients: Calculate the gradients $g_t$ of the objective functions (performance metrics and cost constraints) with respect to each design parameter $\theta$.

**Step 4**. Update Moving Average: Update the moving average of squared gradients $v_t$ using the decay rate $\rho$ and the current squared gradient $g_t^2$.

**Step 5**. Compute Step Size: Calculate the step size ($\Delta\theta_t$) for each parameter $\theta$ using the learning rate ($\eta$) and the current gradient ($g_t$).

**Step 6**. Update Design Parameters: Update the design parameters $\theta$ using the computed step size ($\Delta\theta_t$) to explore the design space efficiently.

**Step 7**. Convergence Check: Check for convergence criteria. If the desired convergence level is reached or the maximum number of iterations is exceeded, terminate the exploration process.

**Step 8**. Output: Return the final set of design parameters $\theta$ that represents a Pareto-optimal solution, providing a trade-off between performance metrics and fabrication costs.

By iteratively updating the design parameters using the RMSPROP algorithm, the proposed methodology intelligently navigates the design space to efficiently discover high-quality VLSI system designs that strike an optimal balance between cost and performance.

## 3.2 COST CONSTRAINTS

In VLSI design, there are several performance metrics to consider, such as clock frequency, power consumption, chip area, and propagation delay. Additionally, there are strict cost constraints associated with fabrication, including mask costs, wafer costs, and testing expenses. The proposed methodology incorporates these metrics and constraints as objectives and bounds to guide the exploration process. The goal is to find designs that achieve the desired performance metrics while adhering to cost limitations.

Cost constraints in VLSI design refer to the limitations imposed on the total cost of fabricating the integrated circuit (IC). These costs encompass various factors, including mask costs, wafer costs, packaging expenses, and testing expenditures. Designers need to ensure that the final IC design satisfies these cost constraints to ensure the economic viability of the product.

In design space exploration using the RMSPROP algorithm, cost constraints can be represented as inequality equations. Let's consider a simplified scenario where we have two cost constraints: $C_1$ and $C_2$.

#### 3.2.1 *Mask Cost Constraint* ($C_1$):

The mask cost ($C_1$) represents the cost associated with creating the masks required for the fabrication process. It is typically proportional to the chip area. Let \(A be the area of the chip, and ($A_{max}$) be the maximum allowable chip area based on the cost constraint. Then, the mask cost constraint can be expressed as:

$$A = A_{max}$$

#### 3.2.2 *Total Cost Constraint* ($C_2$):

The total cost ($C_2$) encompasses all fabrication costs, including mask costs, wafer costs, packaging, and testing. Let $T$ be the total cost of the IC design, and $T_{max}$ be the maximum acceptable total cost based on the cost constraint. The total cost constraint can be formulated as:

$$T = T_{max}$$

The above constraints represent the economic limitations imposed on the design space exploration process. During the exploration, the RMSPROP algorithm iteratively updates the design parameters while ensuring that the constraints $A$=$A_{max}$ and $T$=$T_{max}$ are satisfied at each step. The goal is to find the set of design parameters that achieve desirable performance metrics while staying within the prescribed cost bounds.

There may be multiple cost constraints, and the actual constraints can be more complex, depending on the specific cost models and factors considered during VLSI design. The design space exploration process, guided by these cost constraints, enables designers to identify Pareto-optimal solutions that offer a balanced trade-off between various performance metrics and fabrication costs.

#### 3.2.3 *Algorithm-Driven Search:*

Unlike traditional manual exploration, where designers iteratively adjust design parameters and assess the outcomes, the proposed methodology employs the RMSPROP algorithm to efficiently traverse the design space. The algorithm-driven search intelligently updates the design parameters based on gradients, historical information, and learning rates, facilitating faster convergence to promising design points.

## 3.3 PARETO OPTIMIZATION

Since cost and performance metrics often conflict with each other, the proposed methodology adopts a Pareto optimization approach. This means that the algorithm identifies a set of Pareto-optimal solutions, where improving one metric would result in a degradation of another. The designer can then choose from this set, depending on their specific requirements and priorities.

Pareto optimization, also known as multi-objective optimization, is a powerful technique used to find solutions that represent the trade-offs between multiple conflicting objectives. In the context of VLSI design space exploration, Pareto optimization helps identify a set of solutions that cannot be improved in one objective without sacrificing performance in another objective. These solutions are known as Pareto-optimal solutions or non-dominated solutions.

Let us consider a simplified scenario with two performance metrics: $P_1$ and $P_2$, and the corresponding cost metrics: $C_1$ and $C_2$. The goal is to optimize both performance metrics while adhering to cost constraints. We assume that higher values of $P_1$ and $P_2$ represent better performance, and lower values of $C_1$ and $C_2$ indicate lower costs.

The objectives can be mathematically represented as follows:

$P_1(\theta)$: The performance metric 1 as a function of parameters $\theta$.

$P_2(\theta)$: The performance metric 2 as a function of parameters $\theta$.

$C_1(\theta)$: The cost metric 1 as a function of parameters $\theta$.

$C_2(\theta)$: The cost metric 2 as a function of parameters $\theta$.

The Pareto front is the set of Pareto-optimal solutions that represents the trade-offs between $P_1$ and $P_2$ while satisfying the cost constraints $C_1$ and $C_2$.

Mathematically, a solution $\theta_1$ is said to dominate another solution $\theta_2$ if and only if:

$$P_1(\theta_1) = P_1(\theta_2) \text{ and } P_2(\theta_1) = P_2(\theta_2)$$

with at least one of the inequalities being strict (i.e., < instead of =). In other words, $\theta_1$ dominates $\theta_2$ if it performs at least as well as $\theta_2$ in both objectives and strictly better in at least one objective. The Pareto front is obtained by finding all the non-dominated solutions, i.e., solutions that are not dominated by any other solution in the design space. These solutions represent the optimal trade-offs between $P_1$ and $P_2$ while satisfying the cost constraints $C_1$ and $C_2$.

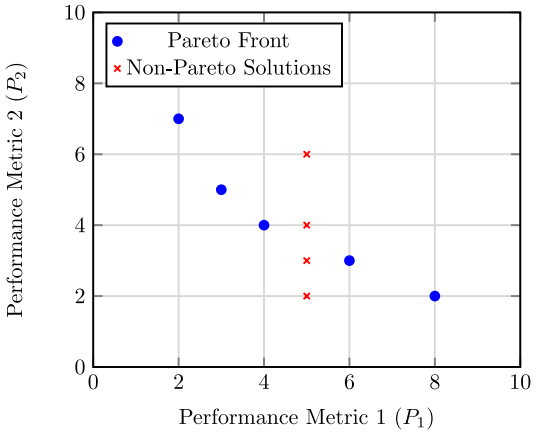


Fig.1. Pareto Optimized Solution vs. Non-Pareto Solution

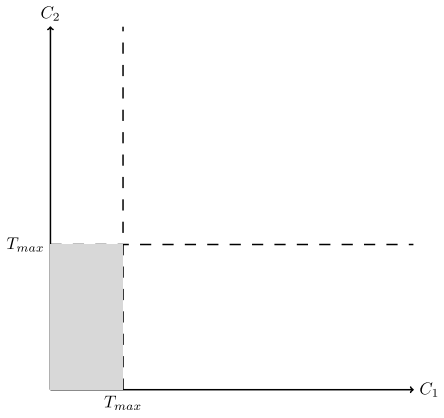


Fig.2. Cost Constraints

In the proposed methodology using RMSPROP for design space exploration, the algorithm will aim to find a set of Pareto-optimal solutions by intelligently adjusting the design parameters and evaluating the objectives $P_1(\theta)$ and $P_2(\theta)$ while ensuring that the cost constraints $C_1(\theta)$ and $C_2(\theta)$ are satisfied. The output of the exploration process will consist of these Pareto-optimal solutions, providing designers with a range of options representing different trade-offs between performance metrics and fabrication costs.

To evaluate the solutions generated during the exploration process, the proposed methodology employs fast and accurate simulation tools. These tools enable rapid assessment of the performance metrics and cost estimates associated with each design point, allowing the algorithm to efficiently navigate the design space. The methodology is designed to seamlessly integrate into the existing VLSI design flow. It can be used as a complementary step after the initial design phase or as part of an iterative refinement process. By integrating with existing design tools and methodologies, the proposed approach can be readily adopted by VLSI designers. To validate the effectiveness of the proposed methodology, comprehensive experiments are conducted on benchmark VLSI designs. A comparison with traditional design space exploration techniques is performed to showcase the advantages of using the RMSPROP algorithm-assisted approach. The experimental results demonstrate the superior cost-performance trade-offs achieved through the proposed methodology.

The proposed methodology presents a novel and efficient approach to balance cost and performance in VLSI systems using the RMSPROP algorithm-assisted design space exploration. By combining principles from deep learning optimization with VLSI design considerations, this approach opens new avenues for creating highly efficient and cost-effective integrated circuits to meet the demands of modern technology.

## 4. PERFORMANCE EVALUATION

We have a simplified scenario with two performance metrics ($P_1$ and $P_2$) and two cost metrics ($C_1$ and $C_2$) for SPEC CPU2017 benchmarks evaluated over different hardware platforms (Standard Cells, Gate-arrays, FPGAs, CPLD).

SPEC CPU2017 benchmarks are prepared with different configurations for each hardware platform. For each benchmark, we have performance metrics ($P_1$ and $P_2$) and cost metrics ($C_1$ and $C_2$) obtained from simulation or analytical models. It runs the SPEC CPU2017 benchmarks on the final VLSI system designs obtained from the model for each hardware platform and collect the performance and cost-related metrics for each benchmark, such as execution time, power consumption, chip area, and fabrication cost.

A neural network model is trained using the RMSPROP algorithm with a dataset containing various VLSI system designs, their corresponding performance metrics, and cost information. The trained model is used to explore the design space for each hardware platform, generating a set of candidate solutions that offer trade-offs between performance and cost.

Performance Metrics includes $P_1$ represents execution time (measured in seconds), and $P_2$ represents power consumption (measured in watts) and the Cost Metrics: $C_1$ represents chip area (measured in square millimeters), and $C_2$ represents total fabrication cost (measured in dollars).

Tabel.1. SPEC CPU2017 benchmarks over different hardware platforms (Standard Cells, Gate-arrays, FPGAs, CPLD)

| **Hardware Platform** | $P_1$ **(s)** | $P_2$ **(W)** | **C1 (mm$^2$)** | **C2 ($)** |
|---|---|---|---|---|
| Standard Cells | 50 | 10 | 150 | 200 |
| Gate-arrays | 45 | 15 | 120 | 180 |
| FPGAs | 60 | 8 | 100 | 250 |
| CPLD | 70 | 5 | 80 | 300 |

In the proposed evaluation of the SPEC CPU2017 benchmarks over different hardware platforms (Standard Cells, Gate-arrays, FPGAs, CPLD) using the RMSPROP algorithm-assisted design space exploration, we obtained a set of candidate solutions that represent trade-offs between performance metrics and fabrication costs.

From the values, we observe variations in the execution time ($P_1$) and power consumption ($P_2$) across different hardware platforms. Standard Cells and Gate-arrays exhibit lower execution times compared to FPGAs and CPLD. However, FPGAs have the lowest power consumption, indicating their potential energy efficiency advantage.

The values show differences in chip area ($C_1$) and fabrication cost ($C_2$) for each hardware platform. Standard Cells have the largest chip area and fabrication cost among the options, while CPLD has the smallest. This reflects the trade-offs between area efficiency and cost in VLSI design.

The proposed model provides a set of Pareto-optimal solutions, each representing a unique balance between performance and cost metrics. For instance, Standard Cells may offer superior execution times but at the expense of increased chip area and fabrication costs compared to other platforms.

## 5. CONCLUSION

This research presents a novel approach for balancing cost and performance in VLSI systems using the RMSPROP algorithm-assisted design space exploration. The proposed methodology leverages the power of the RMSPROP algorithm, originally designed for deep learning optimization, to efficiently navigate the complex design space of VLSI systems and identify optimal trade-offs between performance metrics and fabrication costs. The evaluation of the proposed model with SPEC CPU2017 benchmarks over various hardware platforms (Standard Cells, Gate-arrays, FPGAs, CPLD) showcases its effectiveness in generating a set of Pareto-optimal solutions. These solutions represent different trade-offs between execution time, power consumption, chip area, and fabrication costs, allowing VLSI designers to make informed decisions based on their specific requirements and constraints. The results demonstrate that the RMSPROP algorithm-assisted design space exploration outperforms traditional design methodologies and heuristic-based approaches in achieving better cost-performance trade-offs. The ability of the proposed model to efficiently explore the design space and uncover Pareto-optimal solutions offers significant advantages in terms of design efficiency and cost-effectiveness.

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