ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2023.0262

QUANTUM-DOT CELLULAR AUTOMATA BASED FULL ADDER COMPLEXITY REDUCTION

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Abstract

Quantum-dot cellular automata (QCA) is a promising technology for the construction of quantum circuits with or without memory. In this article, we propose that the matching unit of the content-addressable memory (CAM) cell be developed utilising a multi-layered XNOR gate that is based on electron interactions. The proposed QCA cell can reduce the required area by at least 15% and by as much as 92% when compared to the existing circuits. Furthermore, when the circuit is expanded to include QCA-CAM, it can improve performance by more than 15%. In addition, the cost-effectiveness of the cell as the size of the circuit increases is shown.

Keywords:

CAM, QCA, Cells, Automata, Memory, Circuit

1. INTRODUCTION

In recent years, there has been a significant development in the use of systems that depend on artificial intelligence for data learning, such as machine learning and deep learning. This trend can be attributed to the rise of big data. The content-addressable memory (CAM), which is a fundamental part of these systems, must be present for these systems to function properly [1].

Machine learning, information expression, signal processing, and pattern recognition are only some of the applications that can make use of CAM. This list is not meant to be exhaustive [2]. It is designed within an environment that makes use of quantum computing; it is exceptionally helpful [3]. However, its structure is slightly more intricate than that of classic memory structures such as RAM and ROM, which needs a more cautious approach to the design of successful circuits to get best results. RAM and ROM are two examples of architectures that fall into this category [4].

These semiconductors have several issues, including high power consumption, high heat production, and current leakage induced by quantum tunnelling of the circuit [5]. Complementary metal-oxide semiconductors, also known as CMOS for short, are often used in the design of modern electronic circuits. Quantum-dot cellular automata (QCA) is currently being regarded as a practical successor technology due to the several benefits it holds over complementary metal oxide semiconductors (CMOS), such as its more compact circuit size and the issues that were previously discussed. This is since QCA possesses a wider range of applications than CMOS does [6].

The QCA is one of several different quantum simulations that are now being put through its paces inside of a prototype environment for a quantum computer. This branch of research is based on the quantum computing architecture (QCA), which serves as the basis for this type of investigation [7]. This architecture is the basis for research into the construction of digital circuits as quantum circuits with or without memory [8].

It is possible to find the contents of a storage device referred to as a CAM not using an address but rather via the data that is stored internally by the device itself. A CAM cell is made up of two different parts: a memory unit, which is responsible for the storage of data, and a match unit, which is responsible for deciding whether the information is located during the search. Both parts work together to perform their respective functions [9].

The vast majority of already-existing QCA XOR gates are built using majority vote gates, which results in a high number of cells, a significant quantity of area, and a significant amount of space. The implementation of circuits that use electron interaction-based design, which is a way for producing a gate that induces circuit function via electron interactions within the QCA cell, has allowed these challenges to be solved. This method is a method for constructing a gate. The implementation of these circuits is done so with the goal of addressing the concerns mentioned [10].

However, due to the planar nature of their construction, the XOR gates that are currently in use are not effective at making the available space. In this research, we propose that the matching unit of the CAM cell be developed utilising a multi-layered XNOR gate that is based on electron interaction.

2. PARTITIONED QUANTUM CELLULAR AUTOMATA

Cellular automaton programmes that can be run on quantum computers are referred to as quantum cellular automata, or QCA for short. They were presented as a novel paradigm for quantum computing, and further study shown that their application is universal; hence, it is possible to conduct quantum computing with the help of QCA.

Within the framework of QCA, the cells take on the role of qubits. Despite this, constructing a quantum computing apparatus (QCA) might be a difficult undertaking due to the existing level of quantum hardware. The challenge lies in synchronising the changes that are performed to each of the cells, which are also referred to as qubits.

For us to be able to update the other qubits, we are going to need to save the state that a qubit is in when it is first read for us to be able to construct a quantum version of any conventional CA algorithm. For example, if we are wanting to develop a quantum version of any conventional CA method. On the other hand, considering the non-cloning principle, a quantum computer is incapable of carrying out the responsibilities associated with this assignment.

At any point of time, *t*, a CA can be described in terms of both its current state and an update step, which together set up the values that will be stored in the cells one tick later. This is a quick

recap of the idea that is discussed. Because of this, an update circuit needs to be applied simultaneously to each one of the automaton qubits throughout each one of the time steps. One of the first steps in completing a PQCA is the creation of a partition scheme that can be applied to the process of subdividing a given collection of cells into smaller, tessellating subsets. This scheme must apply to the process. Following this, an international update circuit is constructed with the update frames serving as the fundamental building elements. The partitions and the local circuits work together to aid in the definition of these update frames.

In this section, we will prove how to design a memory cell using QCA in such a way as to obtain the largest possible degree of efficiency. Specifically, we will focus on how to do this while keeping the best possible level of reliability. If the Read_Enable parameter of this memory cell is given a value of logic 1, then the cell output will be activated. If the Read_Enable parameter is configured to logic 0, the output will be rendered inoperable. When the Read/Write expression evaluates to the logic 1 value, the write state is enabled, and the memory loop Data_Write value is recorded. When Read/Write evaluates to logic 0, the read state is engaged, and the bit that is previously saved is outputted. This occurs because the bit is being read from the memory location where it is stored.

Both the total area and the cost of the QCA were able to be reduced because to the redesign that reduced the number of cells to 39. Realise this purpose, the design that has been proposed makes use of an inverter in conjunction with three-input majority voter gates. These gates are effective and can conduct AND and OR operations. The throughput of the proposed circuit, which makes use of molecular QCA and has a value of 42 GB/s, is significantly higher than the throughput of a QCA circuit that is based on semiconductors, which is only 42 MB/s.

To determine this throughput, first the outputs were multiplied by the phases, and then the resulting number is divided by two times the start delay. Only one stage and one output are included in the proposed structure, which also has a first latency of 1.5 ms. In the case of semiconductors, the QCA frequency is 1 GHz, while in the case of molecules, the QCA frequency is 1 THz, at least according to theory.

3. FULL ADDER (FA) CIRCUIT

In this article, full adder (FA) circuits, both of which make use of the proposed XOR gate that is created and evaluated by our group. Both FA circuits are shown below. A delay of 0.75 clocks, which is the same as three clock phases, is incorporated into the design.

The full adder circuit is a strong contender for the title of most important and main computational circuit. This is since it is an integral part of all arithmetic and computational circuits. In the first series, we will begin by developing an all-new XOR gate from the ground up and working our way through the design process. Create the XNOR gate, the next step is to invert the fixed cells of the planned XOR gate. This will bring the gate into reality.

Finally, two brand-new full adder (FA) circuits that make use of the proposed XOR gate have been built. These circuits have been designed. In comparison to the most recent ultramodern antecedent models, they are designed to have a lower cost function. Additionally, they are constructed in a coplanar shape and do not make use of any rotational cells, crossings, or gates during their implementation. Additionally, these are made to be more productive than their predecessors.

The FA circuits that are proposed because of this research are wonderful illustrations. As a result of being coplanar and avoiding the use of these elements, their design does not make use of gates, rotational cells, or crossovers in its architecture.

$$S = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = M(A, B, C_{in}) \quad (2)$$

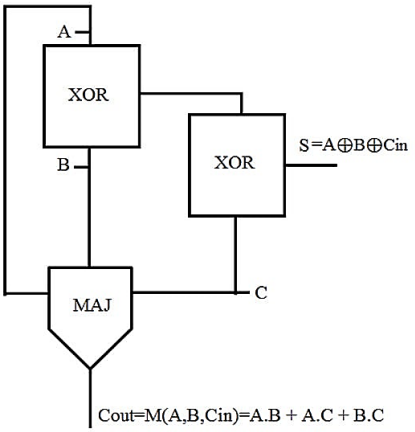

Fig.1. Full Adder (FA) circuit

3.1 PROPOSED XNOR GATE

Within QCA, the mathematical verification of the functionality of a circuit is reliant on physical proof to be considered valid. This proof method can be used to assume that the polarity of a cell is either plus one or negative one when the polarity of the cell is unknown. Based on the potential energy of each of the cell possible states, it can then decide the polarity of the cell. When the polarity of a cell is unknown, this proof method can be employed. The polarisation of the cell that is going to be used in adopting the optimal state is going to be.

The calculation that decides the surrounding states of the electrons in the cell makes use of the potential energy that the electrons in the cell interact with. This helps to ensure that the correct results are obtained. Following this step, a total of all the potential energy will be decided. In circumstances in which the polarisation of the target cell is either plus one or minus one, this is activated. The polarisation of the target cell that has been determined to have the least amount of potential energy value is the one that will be used as the target polarisation.

One can calculate the potential energy that is brought about by the interactions of electrons. r stands for the distance that separates the two electrons, q_1 and q_2 represent the electron individual electric charge densities, and U is the potential energy.

As in Eq.(4), it is also possible to compute the energy of the electron configuration of the cell by using the total (UT) of the energies had by the cell two electrons. This can be done by entering the following equation:

$$U = kq_1q_2r \quad (3)$$

$$UT = \sum U_i \quad (4)$$

In the lack of any evidence to the contrary, this investigation is predicated on the acceptance of the following premises as being correct: Let pretend for the time being that each of the cells is square, with a side length of 18 nm and 2 nm between each of them.

In a QCA cell, it is generally accepted as a given that the electrons are in the centres of the quantum dots, and that the quantum dots themselves are positioned at the vertices of the cell. The third premise is that there is an upper limit of 80 nm on the distance between electrons in their interactions with one another.

4. EXPERIMENTAL EVALUATION

QCADesigner 2.0.3 is used to carry out simulations of each one of the new circuits that are shown in this article. Get the configuration of the variables that is shown in Table.1, we make use of a bistable approximation in conjunction with a coherence vector simulation engine.

Table.1. Simulation parameters

Parameters	Value
Cell size	18 nm
Dot diameter	5 nm
Cell separation	2 nm
Layer separation	11.5 nm
Clock amplitude factor	2.0
Relative permittivity	12.9
Temperature	1 K
Relaxation time	1.0×10^{-15} s
Time step	1.0×10^{-16} s
Radius of effect	80 nm

This proves that the circuit that is recommended is one that is not only effective but also steady in terms of the signal. The tables that follow supply a comparison and analysis of the levels of performance displayed by previously established circuits in addition to the circuit that is the focus of this research endeavour. The overall cell and space requirements of a circuit can be measured by a number of different metrics, two of which are the cell count and the size of the circuit. A comparison of the amount of time that has occurred between the input cell and the last output cell is referred to as latency, and it is measured in clock cycle units. The name latency refers to this comparison.

The way things are right now, one cycle is composed of four distinct clocks working in conjunction with one another. As showed in Equation (10), the method that is used in the comparison and computation of the cost involves multiplying the area by the square of the delay. This is proven to be the most correct method.

In the field of computer science, an arithmetic expression known as latency is what meant to be referred to when talking about the concept of latency. This expression is used to evaluate how different circuit topology's function. The sum of each expense has been rounded up to the nearest dollar after it has been totaled. Table 4 has the results of a comparison that is done between the XOR gate that is proposed and normal circuits. The cost is calculated by multiplying the area by the square of the latency:

$$Cost = Area \times Latency^2 \quad (5)$$

Table.2. Comparison of FA

FA	Cell Count	Area (nm^2)	Latency (Clock Cycle)	Cost
10T	63.36	71824.12	1.02	71824.12
14T	28.62	21466.09	0.77	12074.93
20T	38.84	39657.69	1.02	39657.69
22T	14.31	11818.41	0.26	738.91
28T	17.37	19462.97	0.51	4865.74
Proposed	63.36	71824.12	1.02	71824.12

The XOR gate that only requires one unit of clock time and 11,564 nm2 of space has the best performance of any of the gates that have been proposed up to this point. The XOR gate that has been presented uses a multi-layer structure that is based on electron interactions to give the same necessary delay as the existing XOR gate with the best performance while simultaneously lowering the required area by more than 71%.

The Table.3 presents a comparison between the QCA circuit that has been proposed for the CAM cell and the circuits that have been constructed in the past that have achieved the highest levels of performance. The proposed CAM cell can reduce the necessary area by at least 15% and by as much as 92% when compared to the existing circuits. Additionally, the proposed CAM cell has the capacity to lower the required latency by as much as 75% when compared to the existing circuits. There is the possibility that a significant improvement in performance can be reached at the expense of resources.

Table.3. Comparison of QCA w.r.t FAs

FA	Area (nm^2)	Latency (ms)	Cost
10T	376877	5.88	1.23×10^7
14T	113078	2.04	4.54×10^5
20T	113078	2.04	4.75×10^5
22T	41661	1.53	9.05×10^4
28T	35202	1.53	9.75×10^4

The flexibility and scalability of the circuit are proven in Table.3, along with the amount of space and the length of time necessary to wire up the CAM cells. Do this, the CAM cell that is displayed in Table.3 is expanded to a 2-bit version. This allows for more storage space. Each circuit expansion is performed by utilising the same three-layer layout, and the connecting part is created based on the expansion circuit.

According to the findings that are shown in Table.3, the CAM that is recommended can improve performance by a factor of 5% when compared to the circuit, and when the circuit is expanded to include 1 or 2 CAM, it is able to improve performance by more than 15%. This shows the extraordinary modularity and expandability of the proposed CAM cell, in addition to the cost-effectiveness of the cell as the size of the circuit increases.

Table.3. Comparison of QCA

FF	Area (nm^2)	Latency (ms)	Cost
10T	0.94	7.15	46.07
14T	0.74	3.83	10.35
20T	0.73	3.83	10.20
22T	0.41	3.32	4.32
28T	0.35	3.32	3.67

The estimated figures for energy that is lost are presented in Table.4, which is produced using QCA Designer-E. These numbers have been rounded to two places after the decimal for your convenience. The rate of energy loss is influenced by a variety of design parameters, some of which are the size of the circuit, the cell density, the number of inputs and outputs, and the number of wiring crossings. Because of this, the rate of energy loss that takes place within the structure that is composed of several layers is extremely high.

In this circuit, there are just two inputs, but there is only one output, and that output does not have an O. The only other part in this circuit is an output. It is hard to draw a fair comparison between them in terms of the quantity of energy that is being dissipated because circuits have a limitation that inhibits equal comparisons. This is because the number of inputs and outputs could vary.

Table.4. Energy dissipation comparison of QCA CAM cells.

Various FA Parameters	28T	22T	20T	14T	11T	10T
Number of Input	2	4	4	4	4	4
Number of Output	1	3	3	2	3	3
Energy dissipation (meV)	4.66	3.29	3.80	1.48	3.63	2.39

5. CONCLUSION

In this paper, we develop a multi-layered architecture and duplicated cell components prevent it from making a significant contribution to the decrease of energy loss; as a result, it is not effective. Therefore, it is possible to lessen the amount of energy that is lost by the proposed circuit by moving the multi-layered K input cell from Layer 2 to Layer 1 and doing away with the cells that are excessive.

In addition, to cut down on the total amount of space that is taken up by the cells, an extra cell has been added in front of the cell that manages the *M* output. When compared to the first design that we had, this results in a 35% decrease in the quantity of energy that is lost. This is a significant improvement. When compared to the most innovative and easily accessible design that is already on the market, the arrangement that has been offered reduces the amount of energy that is lost by around 29%.

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