DOI: 10.21917/ijme.2022.0245

IMPLEMENTATION AND ANALYSIS OF DAC'S STATIC AND FUNCTIONAL TESTING WITH MULTI-FREQUENCY

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Abstract

In this paper, the authors propose a system for testing and verification of DAC's static parameters. The parameters considered for testing are Gain, Offset, Differential Non-Linearity, and Integral Non-Linearity errors. The Loopback method is employed to verify the functionality of both DAC and ADC with multiple frequencies. The existing DAC's linearity testing approaches include signal conditioning circuits, but the proposed system does not use any additional circuit components for testing. So, the access time of DAC and ADC can be reduced, it is demonstrated by doing experimentation on 12-bit serial Octal DAC (AD5328) IC, and 12-bit serial Dual ADC (AD7266) using Altera FPGA Kit with Quartus Prime Software through Verilog. The detailed analysis of test results concludes that the static characteristics of DAC are met with its specifications. The power consumption for DAC_ADC Functionality test module is 0.143Watts, (Pstatic – 0.097W, Logic – 0.001W, Inputs/Outputs – 0.039W, Clocks – 0.006W). The minimum testing time for the DAC_ADC functionality test for single data is 0.66µs.

Keywords:

Functional testing, Differential Non-Linearity, Integral Non-Linearity, Static Testing, Digital to Analog Converter

1. INTRODUCTION

Data Converters (DAC and ADC) are the prime components in the field of modern communication and real-time embedded systems since both devices act as an intermediate layer between the analog world and digital signal processing (DSP) devices [1]. Today each electronic device demands more requirements on huge data processing with high speed, good quality, and also more accuracy as they integrate more and more features in design [2]. The advantages of digital processing like better stability, high reliability with ease of up-gradation lead to the contribution towards huge applications of digital electronics [3]. Every integrated circuit's (ICs) specification must be tested before shipping to the customer's place [4]. As the testing time of advanced data converters with high resolution increases exponentially, this leads to an increase in test cost. Thus, it is crucial to test ADCs and DACs at a low cost which leads to a reduction in the overall cost of the design. So, the testing approach of DAC and ADC performances becomes critical.

DAC testing is generally divided into two categories. One category is static linearity specifications, which involve measuring gain, offset, differential non-linearity (DNL), and integral non-linearity (INL). The second category is measuring the dynamic performance of the DAC, which includes Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), etc. It is necessary to measure both functional and parametric characteristics of converters to say that it's complete and trustworthy testing [5]. The testing of ADCs and DACs can be implemented in different ways. One way is to use discrete components, namely analog sources and voltmeters for ADC testing, digital sources, and oscilloscopes for DAC testing. To obtain static and dynamic parameters of converters different computations are applied to the measured data. Since most of the real-time applications contain both converters, the loopback testing method is suitable for testing by sending inputs to DAC and receiving output from ADC so testing each other becomes a promising solution to automatic test equipment (ATE) cost reduction [6]. Our work focuses on efficient testing of static linearity specifications of DAC and functional test of both DAC and ADC using loopback testing technique, which is demonstrated using commercial ICs AD5328 and AD7266 respectively.

The paper is organized as follows. Section 2 discusses the static characteristics of DAC. Section 3 presents the design and DAC testing with the loopback method for a commercial IC. In section 4, the paper demonstrates simulation, hardware implementation, and result analysis made. Section, 5 represents the conclusion of the paper.

2. STATIC CHARACTERISTICS OF DAC

In practice, DAC's performances will be affected due to its non-ideal nature of transfer characteristics. The DAC's static and dynamic characteristics are determined by finding the differences between its ideal and actual behavior. This work is focused on the most commonly used static parameters, namely full-scale range, offset and gain errors, INL (Integral Non-Linearity), and DNL (Differential Non-Linearity) errors [7].

2.1 FSR (FULL SCALE RANGE)

Full-scale range (V_{FSR}) is defined as given in equation (1), which is the difference among the voltages produced by the DAC with its maximum and minimum input values. This is achieved by measuring the DAC's positive full-scale voltage, V_{FS+}, and DAC's negative full-scale voltage, V_{FS-}.

$$V_{FSR} = V_{FS+} - V_{FS-} \quad (1)$$

2.2 GAIN AND OFFSET

To determine gain and offset, there are two methods, first one is the endpoint method. In this method, minimum scale and full-scale points are used to find gain, and offset is calculated based on the intercept of the line. The second method is the best-fit line, here both gain and offsets parameters are determined by taking the minimum mean squared error from line to sample value. For example, $S(i)$ is the sample set, where 'i' varies from 0 to N-1 and N represents the number of samples in the sample set. The gain and offset equations are derived from various techniques. One technique that minimizes the partial derivatives with respect to gain and offset of the squared errors between the sample set S and

the best-fit line. The following equations are derived from the partial derivative technique [8].

$$Gain = \frac{NK_4 - K_1K_2}{NK_3 - K_1^2} \quad (2)$$

$$offset = \frac{K_2}{N} - gain\frac{K_1}{N} \quad (3)$$

where,

$$K_1 = \sum_{i=0}^{N-1} i, K_2 = \sum_{i=0}^{N-1} S(i), K_3 = \sum_{i=0}^{N-1} i^2, K_4 = \sum_{i=0}^{N-1} iS(i)$$

ΔG represents a Gain error, which is expressed as a percent, defined as –

$$\Lambda G = \left(\frac{G_{Actual}}{G_{Ideal}} - 1\right) * 100\% \quad (4)$$

The offset error can be calculated by subtracting ideal voltage at DAC input as zero code from DAC's offset voltage, which is given as follows-

DAC offset error = DAC offset - ideal offset *(5)*

2.3 DIFFERENTIAL NON-LINEARITY (DNL) ERROR

Differential Non-Linearity (DNL) is about defining the uniformity of the LSB step sizes among the successive DAC codes and equation of DNL is given as-

$$DNL(i) = \left(\frac{s(i+1) - S(i)}{V_{LSB}}\right) - 1 \quad (6)$$

2.4 INTEGRAL NON-LINEARITY (INL) ERROR

The integral nonlinearity curve is the difference between the actual DAC's behavior and the best-fit line of the DAC. 'INL' can be calculated as follows, where the Offset value represents the value of DAC output with input value as 0, V_{ref} - reference voltage, and D- represents the decimal value of DAC input.

$$INL(i) = \left(2^N * \left(\frac{S(i) - Offset\ value}{V_{ref}}\right)\right) - D \quad (7)$$

3. DAC TESTING WITH LOOP-BACK METHOD

The work proposes hardware implementation and analyzes the functional and static characteristics of DAC using loop-back output responses with help of ADC. The advantages of a loop-back setup are there is no additional hardware required for functional testing and more flexibility due to software-based test control. Since both the input stimulus and output responses are digital, FPGA is the most suitable device for controlling the testing of mixed-signal devices. FPGA based loopback test setup is shown in Fig.1.

3.1 CASE STUDY FOR LOOPBACK METHOD

The loopback test method is implemented by using a 12-bit Octal DAC – IC (AD5328), 12-bit Dual ADC (AD7266), and Altera Cyclone FPGA kit. FPGA is the main controller for testing DAC and ADC devices. The block diagram of the FPGA design for testing DAC and ADC is shown in Fig.2. It consists of an FSM for DAC and ADC serial interfaces, generation of DAC data is done by using the counter, ADC output is compared with DAC input data and displays the results. To drive the FSM and display modules, a clock will be used which is generated by the clock division module. The testing initiation and termination for the DAC_ADC pair is controlled by input switches, the speed of the test is based on the clock set through clock division module.

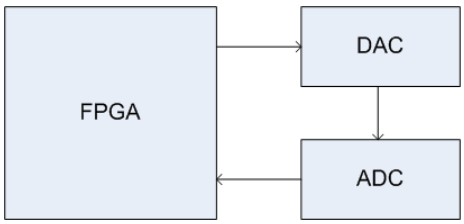

Fig.1. DAC-ADC Loopback test setup

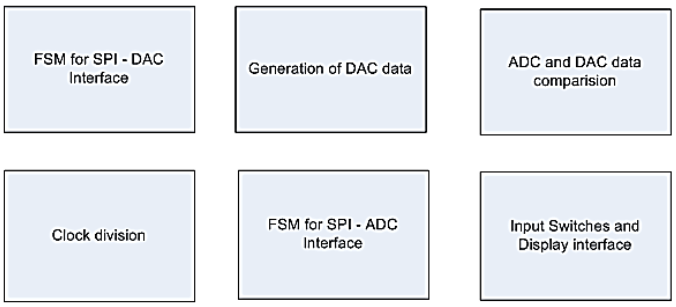

Fig.2. Block Diagram for testing DAC and ADC

In the FSM diagram shown in Fig.3, default values of DAC namely DAC selection, gain, and reference bits are set before the start of the testing process, this setting is controlled by a reset signal. Once the testing process starts, a temporary register is assigned with the required command or data. Then SPI protocol is enabled and 12-bit DAC data will be sent serially to the device under test (DAC – AD5328). This process continues until the last data is sent to the DAC device. Similarly, one more FSM is designed for ADC interface. Fig.4 shows the flow diagram for the SPI interface. This SPI protocol works with a frequency of 1.565MHz generated by a frequency division module with a system clock 50MHz.

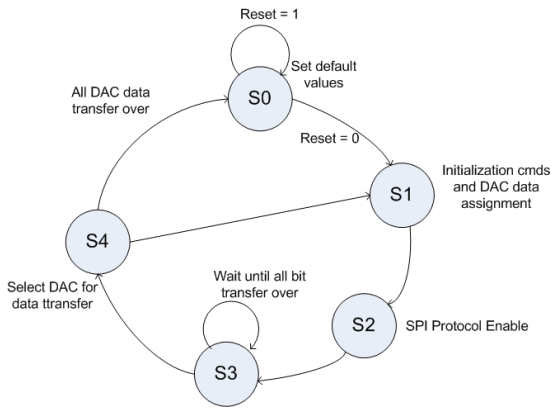

Fig.3. FSM for DAC Control

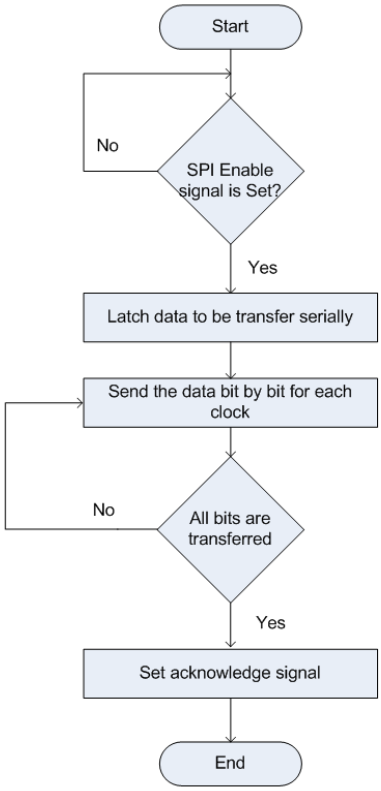

Fig.4. Flowchart for SPI interface

4. RESULTS AND ANALYSIS

4.1 SIMULATION RESULTS

The simulation results of SPI protocol realization are proved with the transmission of DAC commands and data respectively using Xilinx ISE 14.3 tool. In Fig.5, DAC data bits are transferred serially through signal 'spi_sdo' with help of clock pulse 'spi_clk' signal. In Fig.6, the values 0x800d, 0xa000, and 0xc000 represent the DAC commands for gain and reference, DAC output acknowledge signal, and power down settings of DAC respectively. The values 0x0000, 0x1aaa, 0x2555 and 0x3fff represents the DAC data to test quad channels for 0V, 2V, 1V and 3.3V outputs respectively.

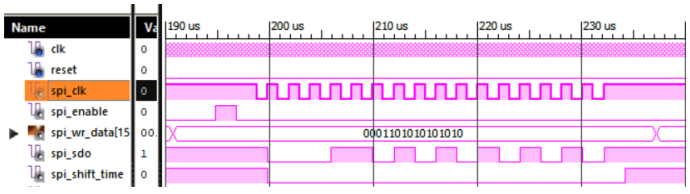

Fig.5. Simulation of SPI protocol

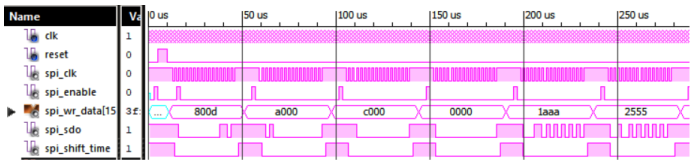

Fig.6. Simulation of DAC commands and data transmission

4.2 IMPLEMENTATION RESULTS

All the designed RTL modules are implemented on Cyclone – II FPGA. Generated DAC data is sent to DAC IC and outputs are sent to ADC IC. The hardware setup developed for testing the DAC and ADC is given the Fig.7. There are two kinds of tests, first one is the testing of static characteristics. In this work, the static test is carried out for the range 0 to 1023 values with a step size of one and monitored these values through a high-end 6 and half digit multimeter.

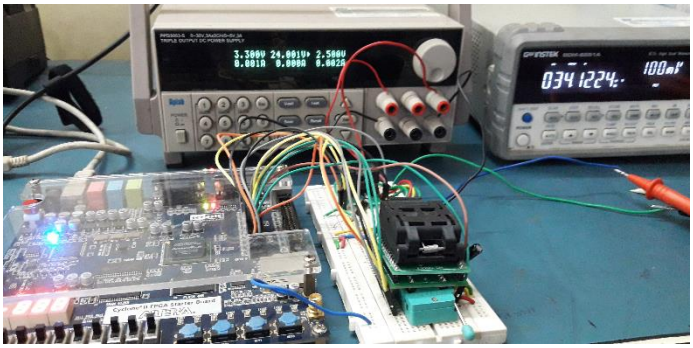

Fig.7. Hardware setup for DAC and ADC testing

DAC's functionality test is observed on the oscilloscope by generating ramp signal through RTL module in FPGA which is shown in Fig.8.

Fig.8 DAC's functionality test using ramp signal

DAC output values are analyzed by using equations 1 to 7. DAC output is calculated by using Eq.(8), where D – the decimal equivalent of input binary value, N – represents the number of DAC bits.

$$V_{out} = \frac{V_{ref} * D}{2^N} \tag{7}$$

All DAC results are plotted as graphs shown in Fig.9(a) and 9(b). In FPGA, RTL code generates binary values through a 10-bit counter which will be fed to DAC through SPI protocol. In graph 9(a), the horizontal axis shows DAC inputs which are represented with the decimal equivalent of corresponding binary values in the range 0 to 31 and the vertical axis gives DAC outputs which are measured through a six-digit multimeter in the mV range. With DAC input as binary 0x000, the actual output voltage is 3.2139mV. For DAC input 31 (decimal value), the expected output is 24.9756mV and the actual output is 26.0657mV. The difference between expected and actual output is 1.0901 mV. Similarly, graph 9(b) shows overall DAC results to decimal input

with a range from 0 to 1023 values, for the last DAC input value i.e.,1023, the expected voltage is 824.1943mV and actual DAC output is 818.8041mV, the difference is -5.3902mV.

DNL and INL test results are shown in Fig.10(a) and 10 (b) respectively. DNL results are calculated using equation (6). The horizontal axis shows the decimal equivalent of DAC input and the vertical axis shows DNL values in LSB. The DNL value is calculated for each DAC input and plotted as a graph. +1 LSB and -1 LSB lines indicate the variation range of DNL value for AD5328 as per its datasheet. The expected DNL value is 0.00708 LSB for the full range from 0 to 1023, the actual DNL value is varying from -0.8646 to 0.9565 LSB but most of the values are between ±0.25 LSB which is much within the specified range. INL values are calculated using equation (7). For DAC input 0x000, INL value is 3.9878 LSB and with last decimal input 1023, INL value is -6.6904 LSB. The DAC results shown in the below figures will be analyzed in section 4.4.

4.3 ADC AND DAC FUNCTIONALITY TEST RESULTS

ADC (AD7266) IC is tested for its functionality with reference to DAC input. ADC is tested for 0V, 0.5V, 1.0V, 1.5V, 2.0V, 2.5V input values which are generated by DAC. ADC is tested for each input with 100 iterations, output data is captured, and an average of all obtained values is calculated. All the results are plotted through graphs as shown in Fig.11. In the following figures, the x-axis represents a number of ADC readings taken for fixed DAC input and the y-axis indicates ADC output values in mV with respect to iteration number, and the Offset value at DAC output is 25.5263mV. In Fig.11, the first figure shows ADC output for fixed DAC input 0x000 and the first iteration value of ADC output in equivalent voltage is 30.5mV (after conversion from decimal value to voltage) for ADC input of 28.3737mV. DAC output (ADC input) varies from 28.3737 to 32.4875mV for successive iterations. The average value of all the ADC outputs is 34.0624mV. Similarly, ADC outputs are measured for various inputs as mentioned above.

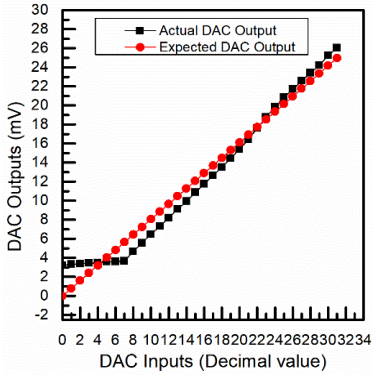

Fig.9. DAC Transfer characteristics (a) For DAC input - 0 to 31decimal values

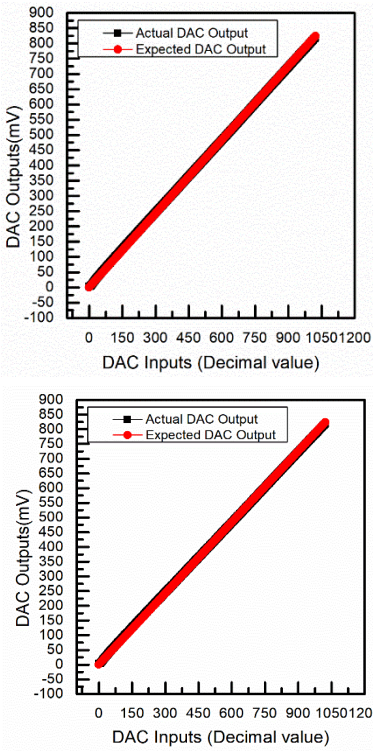

Fig.9. DAC Transfer characteristics (b) For DAC input - 0 to 1023 decimal values

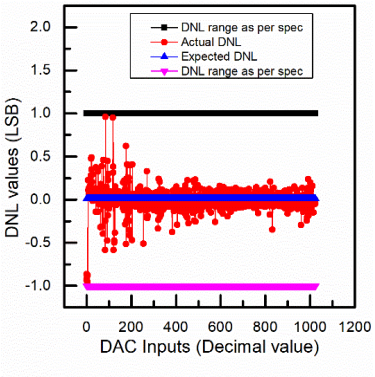

Fig.10(a). DAC DNL results

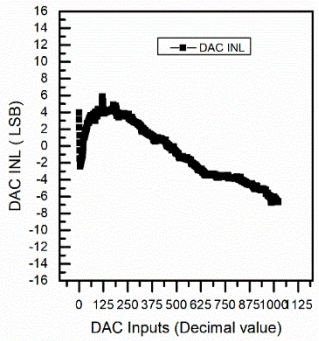

Fig.10(b). DAC INL results

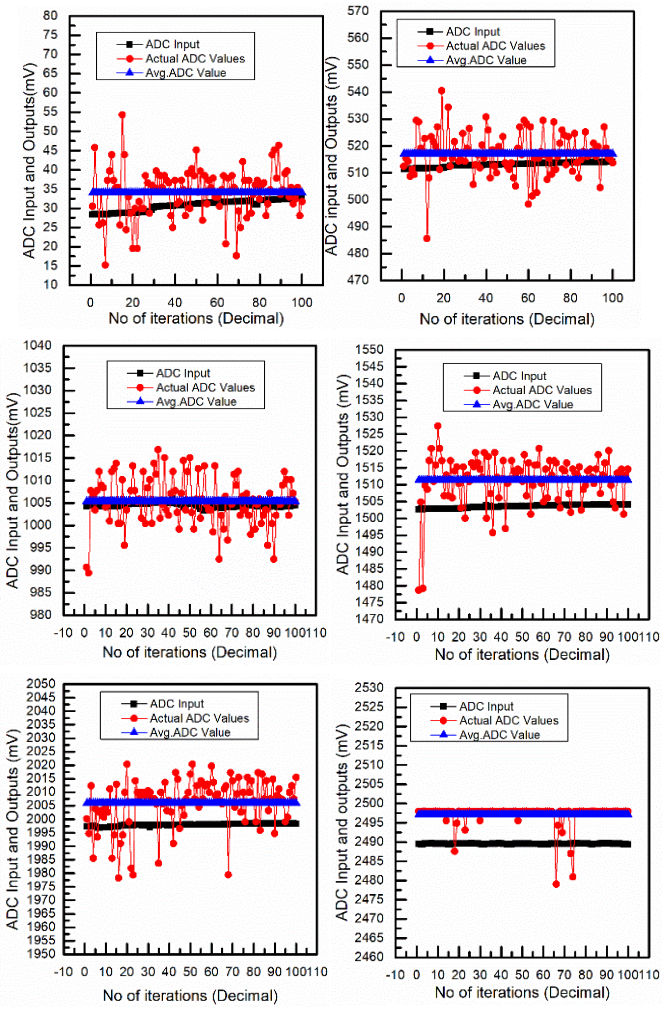

Fig.11. ADC Outputs for inputs 0V, 0.5V, 1V, 1.5V, 2V and 2.5V respectively

4.4. RESULT ANALYSIS

DAC (AD5328) is tested with3.3V reference voltage supplied by an external voltage source, the offset value at DAC output is 21.2919mV, and the step size is 0.8mV. Expected DAC outputs are calculated using equation (8). DAC's performance is tested by considering the input range from 0 to 1023 decimal values (10-bit maximum value). By observing the results obtained as shown in Fig.9(a) and 9(b), the difference between actual and expected results lies in the range of around ±5mV. These graphs are drawn by nullifying the offset value from both expected and actual values. To evaluate the difference between expected and actual values and also step size values, INL and DNL errors are calculated and shown in Fig.10(a) and 10(b). The obtained DNL and INL values lie within the specified range with respect to the device's datasheet. The gain and offset errors are calculated using the equations mentioned in section 2. Calculated values for gain and offset are 0.7969mV and 25.2533mV respectively. The offset value is 21.2929mV, So the offset error is 3.9614mV and the gain error is -0.387%. All these values match exactly with the specifications given in the datasheet of DAC IC. The comparison chart between actual values and datasheet values has been in given Table.1. After analyzing all these values, it is clear that DAC (AD5328) IC is performing its functionality properly and meeting its requirements.

ADC (AD7266) is tested for its functionality through DAC input for different values ranging from 0 to 2.5V with 1.565MHz, 1MHz, and 50KHz multiple frequencies. In this proposed testing setup, no signal conditioning circuit or elements is used for ADC testing as the focus is on functionality testing rather than performance, and DAC and ADC reference voltages are set for 2.5V. In ADC results graphs, the offset value is 25.5263mV. The difference between average ADC outputs and expected values is around ±10mV by considering all the graphs. As ADC is a more sensitive device compared to DAC and testing devices are not mounted on PCB, with a ±10mV difference it can be declared that ADC is tested for its functionality for the full-scale range (0 to 2.5V). So, ADC IC can be tested using DAC for its functionality using the proposed setup without any additional circuit.

Table.1. Comparison chart between DAC actual values and Datasheet values

Parameter	DAC test Values from Proposed Test Setup	Datasheet Values
Gain Error	-0.387%	± 0.3 %
Offset Error	3.9614mV	Range - ± 5 to ± 60mV
DNL Error	Within ± 1 LSB	± 1 LSB
INL Error	± 6 LSB for 1024 values	± 16 LSB

5. CONCLUSION

In this paper, a simple and efficient loopback testing method is implemented on FPGA based test platform for testing mixed-signal devices DAC and ADC. The main focus of the work is to test static characteristics of DAC by considering parameters like gain, offset, DNL, and INL errors and functionality tests of DAC and ADC. This paper has analyzed the static characteristics of commercial IC- AD5328(DAC) and AD7266 (ADC) functional testing with the loopback technique. After analyzing the DAC results, it is concluded that the proposed test platform meets the specifications of DAC as per its datasheet. One of the major advantages of this work is that it supports the testing of many other data converters with the same test platform by making small changes in the RTL module based on their resolution and settings of parameters. No need to make any hardware changes as it doesn't have any signal conditioning circuits or PCBs. The power consumption and testing time are calculated for DAC_ADC testing. Power consumption for DAC_ADC Functionality test module is calculated based on FPGA device (Cyclone-II) spreadsheet analysis is 0.143Watts, which is divided into Pstatic – 0.097W, Logic – 0.001W, Inputs/Outputs – 0.039W, Clocks – 0.006W. The minimum time requirement for the DAC_ADC Functionality test for single data is 0.66µs, calculated based on the FSM design for data sending to DAC and receiving ADC output in a looping fashion. The proposed test platform can be enhanced further to support ADC and DAC devices with serial interfaces like QSPI, I2C, etc.

REFERENCES

[1] Xuan-Lun Huang and Jiun-Lang Huang, "ADC/DAC Loopback Linearity Testing by DAC Output Offsetting and

Scaling", *IEEE Transactions on VLSI Systems*, Vol. 19, No. 10, pp. 1-14, 2011.

[2] Martin Sekerak, Linus Michaeli, Jan Saliga and Marek Godla, "Dynamic DAC Testing by Registration of the Input Code Word in Equality when the DAC Output Matches a Reference Signal", *Acta Electrotechnica Et Informatica*, Vol. 11, No. 3, pp. 31-35, 2011.

[3] Mingrui Zhang, Yao Han, Fei Geng, Chenghui Zhang and Bin Duan, "Research on High-speed ADC Test and Evaluation System", *Chinese Automation Congress*, Vol. 14, No. 2, pp. 1-14, 2017.

[4] Shravan K. Chaganti, Abalhassan Sheikh, Sumit Dubey, Frank Ankapong, Nitin Agarwal and Degang Chen, "Fast and Accurate Linearity Test for DACs with Various Architectures using Segmented Models", *Proceedings of International Conference on Test*, pp. 1-4, 2018.

[5] Sevada Arabyan, Vladimir Shuvalov, Leonid Kessarinskiy, Alexey Shirin and Dmitry Boychenko, "Simultaneous Parametric and Functional Testing of Digital VLSI During Radiation Experiments", *Proceedings of International Siberian Conference on Control and Communications*, pp. 1-8, 2021.

[6] Hak-Soo Yu, Jacob A. Abraham, Sungbae Hwang and Jeongjin Roh, "Efficient Loop-Back Testing of On-Chip ADCs and DACs", *Proceedings of International Conference on Design Automation*, pp. 24-29, 2003.

[7] E. Balestrieri, S. Moisa and S. Rapuano, "DAC Static Parameter Specifications - Some Critical Notes", *Proceedings of International Conference on Automation Testing*, pp. 1-14, 2005.

[8] Gordon Roberts, Friedrich Taenzler and Mark Burns, "*An Introduction to Mixed-Signal IC Test and Measurement*", The Oxford series in Electrical and Computer Engineering, 2012.

[9] V. Kerzerho, P. Cauvet, S. Bernard and O. Chakib, "ADC Production Test Technique Using Low-Resolution Arbitrary Waveform Generator", *Proceedings of International Conference on VLSI Design*, pp. 1-11, 2008.

[10] Aldo Baccigalupi, Mauro D'Arco, Annalisa Liccardo and Michele Vadursi, "Test Equipment for DAC's Performance Assessment: Design and Characterization ", *IEEE Transactions on Instrumentation and Measurement*, Vol. 59, No. 5, pp. 1-15, 2010.

[11] Yuming Zhuangand Degang Chen, "Cost-Effective Accurate DAC-ADC Co-Testing and DAC Linearization", *Proceedings of International Conference on Instrumentation and Measurement Society*, pp. 14-17, 2018.