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HIGH SPEED MODIFIED WILSON CURRENT MIRROR BASED LEVEL SHIFTER FOR MIXED SIGNAL SYSTEMS

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Abstract

Scaling the voltage in contemporary digital and mixed-signal systems has shown to be a successful method for lowering both the dynamic power and the leakage power. This has been demonstrated through extensive research. One way that is helpful in the building of ultra-low-power systems is the decrease of the supply voltage to levels that are either close to or below the threshold voltage. This is one method that can be used. However, operation near or below the threshold slows down digital circuits and diminishes their efficiency, neither of which are properties that are desired in digital circuits. It is required to make use of more than one supply voltage in order to accommodate the various components of the system, which work at different speeds. This article presents the development of a high speed modified wilson current mirror based level shifter for mixed signal systems.

Keywords:

High Speed, Wilson Current Mirror, Level Shifter, Mixed Signal Systems

1. INTRODUCTION

The compromise that must be struck between power and delay might be more easily managed with the assistance of novel multi-supply voltage design (MSVD). Through the use of the MSVD methodology, the design is segmented into a large number of voltage domains, and each of these voltage domains is provided with its very own dedicated supply voltage in accordance with the particular time limitations that are associated with it. [1]-[2]. As a direct result of this, level shifting circuits are utilized very frequently in MSVD systems in order to bridge the gap that exists between the various voltage levels. This is done in order to ensure that the system is able to function properly.

Level shifters (LSs), which are responsible for transforming low voltage level (VDDL) to high voltage level, have become a vital component of many systems as a direct result of this development (VDDH). Because of this need, LSs need to be substantially more agile and lower in stature than they were previously required to be. In addition to this, they should be able to convert input voltages that are very low while using a very little amount of power. A feasible alternative has been proposed in the form of LSs that have a low power consumption, a minimal latency, and huge conversion ranges. [3] The great majority of LSs use either current mirrors (CM) or differential cascode voltage switches (DCVS) for their switching elements. DCVS stands for differential cascode voltage switches.

Because of the pass transistor (MN2), the voltage at node n3 quickly drops to zero volts (ground), which, in turn, boosts the voltage at node n1 by means of the transistors MP1, MP3, and MP6. This takes place whenever there is a shift from a high to a low value at the input (A). This mechanism stimulates MN3, which, as a result, results in a more rapid transition to the falling state. This is accomplished by producing a voltage swing at node n1 of at least 1V in magnitude, which then activates the mechanism. It is possible to get a much faster fall transition in output by applying the split-control driver [4] in the SMLS. This compensation for a limitation demonstrated by the MLS during this phase makes it possible to achieve a much faster fall transition in output. MP4 is being degraded by input-controlled MP5, which implies that the current in MP1 is not being correctly reflected in MP2; this is occurring at the same time as the previous sentence. As a result of this, the contention problem is reduced as a consequence of the low switching current of 5.3 A that it creates during the transition from rise to fall.

This is because of the fact that this occurs as a consequence of this. Since the input (A) goes from being low to being high, the voltage at node n1 is abruptly pulled down to ground, which leads in a low switching current. This is because the input was previously low. When node n2 begins to discharge, it triggers a sufficient quantity of MP7 to ensure that the output node, which is node Z, is charged to VDDH. This is accomplished by activating a sufficient amount of MP7. In order to make up for the smaller voltage swing that is generated by the MLS [5]-[8], the node Z output voltage has been increased to its full range in order to compensate for this. Since MP4 is not being used, the amount of current that is going through MP2 has also decreased. This is because MP4 is not being used. On the other hand, when there is a rise in the voltage at node n3, MP3's capacity to carry an electric current decrease as a result of the change. As a direct result of this, the switching current at the rising edge was reduced to 2.4 A.

Because of this, the voltage that is measured at location n2 vacillates between the values of VDDH and VTHP in a direct and immediate manner. Both of these events take place while the output node Z is being charged. Both of these occurrences take place at the same time. When the edge is falling, a charge is also applied in the direction of VDDH to node n1, which triggers node MN3 to become active. Concurrently, as the voltage at node n2 rises higher than VDDH-VTHP, the transistor MP7 begins to function in the sub-threshold zone and weakly conducts current. This occurs because the conductivity is below the threshold for the system. Because of the limited voltage change that takes place at node n2, MP7 has a shorter reaction time throughout both shifts. This is a direct effect of the minimal voltage change. Because of the split-control output driver, the proposed LS has a shorter propagation delay than the MLS does. This is because of the way the driver works. Additionally, the suggested LS uses less power than the MLS does since diode-connected and input-controlled PMOS devices give a lower switching current. This is one of the reasons why the suggested LS is superior.

2. WCMLS

The amount of static current that flows through the WCMLS in order to manage the amount of static current that flows through

the WCMLS during the Low-to-High (LH) transition is depicted in Fig.1 with the symbol MP3. Node A has picked up an input with a low logic value (0 V), and it has done so. This results in the voltage of Node n1 and Node n2 increasing to a level that is quite close to the high voltage (VDDH = 1.8 V). This occurs because the LH transition of the input signal is a left-hand transition. This is done in order to ensure that the voltage at node n3 may be brought up to VDDH=1.8 V. After that, there will be no further restrictions placed on the flow of current through MP2 (MP1 and MP2 form a current mirror).

The device MP3 will turn off the static current in the input branch if it detects that the voltage at node n3 has reached a predetermined threshold (MN1 and MP1). Because of this, it brings the amount of power that the WCMLS consumes while it is not being actively used down to a more manageable level. In this way of operation, the voltage at node n3 triggers a buffer stage made up of I2 and I3 to transmit a logic high signal to node Z. When the input signal goes from being high to being low, MN1 and MN2 will flip between being off and on (HL; 0.4 V to 0 V). This results in the voltage at output node Z falling to a lower level and causes node n3 to be discharged to ground (0 V).

Whenever the value of the input (A) changes from low to high, the feedback device MP3 is disabled. This decreases the amount of current that flows through the circuit. The outcome of this is a reduced voltage swing (RVS), which can be seen in Fig.1. This implies that node n3 does not fully acquire VDDH. Because node n3 does not completely acquire VDDH, this is the situation that has arisen. The output inverter, which is designated by the letter I2, is subjected to a greater static current flow as a direct result of the RVS problem. The reduced voltage swing at node n3 is 0.4 volts less than VDDH when the WCMLS is built with technology of 180 nm, which is smaller than the standard. The Fig.1 illustrates this point further. Additionally, the rising edge exhibits a delay of roughly 4.6 nanoseconds when compared to the falling edge.

On the falling edge of the input signal, activating MN2 and MP3 will cause Node n3 to be discharged to ground, which will ultimately result in the circuit being finished (A). Since of this, current travels through MP2 because nodes n1 and n2 share charges, which causes current to flow through MP2. This results in an occurrence of current contention (CC) between MP2 and MN2, which is a direct consequence of the fact that node n3 is pulled upwards toward VDDH. As a direct result of this, there is a considerable lag during the shift from summer to fall. A delay in the falling edge is seen in Fig.1b that is approximately 25 ns longer than the delays shown in the previous figures.

Using longer MP1 channels is one way to get around the limitations that have been discussed previously. Despite this, it increases the amount of time required for the rise and fall of the voltage as well as the quantity of power that is required. Alternate pull-up structures can be employed to offset the drawbacks of WCMLS. Some examples of these structures include low-voltage current mirrors, mixed threshold CM-based LSs, and reduced swing buffers at node n3. These solutions, however, come at a larger cost than others, both in terms of the amount of electricity that they consume and the amount of space that they require physically. By utilizing an input-controlled diode chain in conjunction with a hybrid buffer topology, the RVS problem that was present in the WCMLS was successfully resolved. Another way that helps ease RVS and CC difficulties is changing the structure of the WCMLS with the use of a split-control output driver. This method can be used in conjunction with other methods. The LSs that are now on the market have problems with circuit complexity, high switching energy, and considerable delays; however, the MLS that has been designed overcomes all of these problems. The output voltage of this device is able to fully swing, in contrast to the WCMLS's limited range.

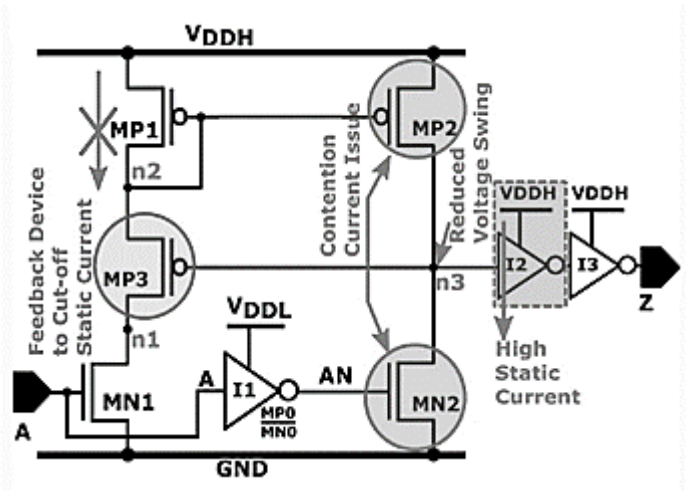

Fig.1. WCMLS

3. PROPOSED MLS

Because it is a complementing pull-up and pull-down network, its standby power usage is practically nonexistent. This can be ascribed to the fact that it has both of these networks. The most major disadvantage is the fierce competition that occurs between pull-up networks and pull-down networks while switching. This competition takes place during the process. At the threshold voltages for IN and VDDL, the pull-down transistors (M1, M2) are rendered ineffective due to the presence of the pull-up transistors (M3, M4). The status of the output does not shift as a direct result of this fact because it does not change. It is feasible to enhance the power of pull-down transistors by increasing the size of the transistors that make up the device.

Since this is not possible, pull-down transistors cannot be used for whatever it is that you're trying to perform. When working with low-power transistors, pull-down circuits are utilized, but pull-up circuits are utilized when working with high-power transistors. Pull-up circuits are yet another option that can be utilized. On the other hand, this does not have a substantial impact due to the fact that the voltage difference between VDDL and VDDH is noticeably greater than that which exists between high and low. Because of this, the pull-down transistors still need to be a great deal bigger than they were before. This, in turn, brings about a considerable rise in both the area and the load capacitance, which, in turn, brings about an increase in the amount of power that is required and limits the reduction in latency.

The aforementioned shifters were utilized in the aforementioned shifters. Despite the fact that these techniques significantly increase switching energy and complexity, they make it feasible to convert voltage over a wide range of potential values. This is a benefit of the techniques. The pull-up network is also going through a gradual but consistent reduction at the same

time. Since of this, they are not suitable for use with DVS because there is a problem with the scalability of the delay when the supply voltage is increased or decreased. It has been proposed that multi-stage level shifters be used, and that the supply voltages for these level shifters should be set at intermediate levels. In addition, it has been suggested that these level shifters be used in conjunction with an intermediate level. This would make the conversion of voltages over such a wide range of conceivable values practicable. There is a rise in the amount of power that is consumed, as well as an increase in the physical footprint that is left behind, as a result of the increased number of circuits that are necessary to provide the intermediate supply voltage. One can avoid the need for additional circuitry that creates voltage if they combine a diode with an NMOS. This makes it possible to eliminate the necessity. The presence of the diode is responsible for the inability to scale the delay because of the constant voltage across the diode, which is caused by the diode. The amount of delay that is introduced by multi-stage level shifters is also noticeably longer than that which is introduced by single-stage devices. The transition time can be greatly reduced by applying a forward body bias to the pull-down transistors in order to achieve the desired effect. The body-bias control leads to an increase in both the amount of power that is required and the level of complexity, despite the fact that the designs lead to increased performance.

As a potential solution to this problem, there have been a few other Type II level shifters that have had their designs tweaked in some way that have been put forward [10]. When the output has been pushed up to its maximum level, MLS will utilize a feedback transistor to turn off the static current. This will occur when the output has been raised to its maximum level. To put it in the simplest terms possible, the outcome of this is a significant reduction in the amount of power that was consumed by the device even while it was functioning normally and doing nothing. The delay and power usage are not as efficient as they may be due to a variety of problems, including a reduction in output voltage and less-than-optimal feedback management. Despite these challenges, the potential for efficiency remains. Through the utilization of logic error correcting, the type II level shifter [9] has the capacity to modify the levels that are present within a circuit.

Detecting the logic fault that takes place between the input and the output enables one to exercise control on the present mirror. Because of this, it is possible for the current to be enabled during switching and then disabled once the cycle of the output has been finished. When it is in standby mode, the device uses a noticeably smaller quantity of electricity than when it is actively being used. Nevertheless, the operation of the logic defect repair circuits causes the system to experience an increased amount of delay as well as switching energy.

It [11] provides a hybrid buffer that operates as a level shifter and uses a modified version of the Wilson current mirror. This buffer also serves as a level shifter. It does this by employing a delay balancing channel and a NOR gate, which work together to make the time difference between the rise of the voltage and its subsequent fall the same. This allows it to be utilized for voltage conversion at close range. In spite of the fact that the MOS devices that make up the NOR gate are capable of being turned off, the gate is still necessary to make use of some standby power because of the static current that is generated by the MOS devices. This will cause the average delay to grow. Because of this, the typical wait time will be significantly increased.

After considering the advantages and disadvantages of ultra-low VLSs of Type I and Type II, we have come to the conclusion that the architecture for the level shifter that we are proposing should be of Type II. This is because Type II has less congestion than Type I does, which means it has the potential to achieve short delays, low switching energy, and scalability in latency. The reason for this is due to the fact that Type II was designed after Type I. Because of its low standby power consumption and incredibly tiny size, MLS was selected as the starting point for this work.

4. WILSON CURRENT-MIRROR LEVEL BASED SHIFTER

After the switching, a feedback PMOS in MLS will turn off the static current that was flowing via M1 and M3, so the problem will be solved. Because of this modification, the normal power consumption of type II level shifters while they are in standby mode has been reduced. The pull-up intensity is decreased, which ultimately results in a lower voltage being measured at node A. On the other hand, because the source current is no longer flowing through M4, the mirror current that was previously flowing through M4 has experienced a considerable reduction in its flow. The voltage drop causes the source current to increase within a feedback loop; however, the increase in source current is not sufficient to restore VDDH at node A. The feedback loop that is being discussed here is a positive feedback loop. When the output of the level shifter stabilizes below VDDH, the output buffer, which has a high standby power consumption and consumes a lot of static current, leads the level shifter to take a lot of power overall. This is because the output buffer has a high power consumption. In order to conduct a more in-depth investigation into this topic, we have re-created the MLS with technology that is 0.18 CMOS.

When the voltage is maintained at node A, there is a drop in that voltage that is more than 250 mV. The voltage drop is plotted against the VDDH values in Fig.4, which shows the relationship between the two. It also contains a plot of the standby power in the output buffer, which reaches a maximum of around 4 nW when the VDDH is 1.8 V and reaches its lowest point when it is 1.7 V. When the supply voltage is exceedingly low, the delay grows at an exponential rate that is proportional to the square of the supply voltage. As a result, the clock period grows to be unusually long during these conditions. Because of this, the level shifter's standby energy consumption can be rather high and makes up the vast bulk of its total energy usage.

The simulations indicate that the pull-up strength will improve if we raise M4 in MLS, and the severity of the voltage drop at node A will be reduced. Because M4 is a multiplier for the MLS, this is the result. Despite this, there is only a limited amount of voltage loss that can be decreased using this method. In addition to this, it causes a large rise in the amount of energy that is required for switching. The switching energy is raised by about a factor of three when the width of the transistor is increased from 0.2 to 1 despite the fact that the voltage loss is reduced to approximately 50 mV.

Because the feedback control activates M5 during the output fall transition, charge is distributed between nodes B and C. This is the cause of the phenomenon known as charge sharing. Another potential problem that may appear with MLS is this one. Because the feedback control cut off the source current after the rising transition, there is a decrease in voltage at the MLS node A. This is the effect of the rising transition. This decrease in voltage is due to the fact that node C, which is situated at ground level, functions as a pull-down on the voltage at node B. This causes the reduction in voltage. Because of this, there is a sudden increase in the fall delay. Because of the voltage drop that occurred at node A, VDDH rose, which led to an increase in the amount of standby power that the output buffer of MLS consumed. The MLS is capable of converting voltages ranging from 0.3 V to 1.8 V. As a result of charge sharing, an additional delay in the system of around 60 ns can be seen. This delay can be detected. Additionally, as a result of this, a considerable quantity of switching current is generated.

Additionally, the feedback control that was coming from node A was able to cut off the source current. On the other hand, it considerably slowed down the upward transition that was happening at node A. This is as a result of the source current being reduced, which caused the charging of node A to become weaker and weaker. The transition will be delayed even further as a result of the influence that the feedback has on the load capacitance at A. The rise transition at A is noticeably slowed down as a result of the feedback, which leads to a significant rise delay as well as a significant switching current. Both of these effects are brought about by the feedback.

5. RESULTS AND DISCUSSION

In order to ascertain whether or not the proposed model is successful, it has been put through an implementation in a 0.18 m CMOS process with the use of tools developed by Cadence. This was accomplished without the use of any CMOS components with multiple thresholds. In addition, the functionality of the SPECTRE simulator is verified by transmitting an input signal of 400 millivolts at a frequency of one megahertz for a length of one nanosecond for the rise and fall of the signal. We are going to work with the assumption that the low supply voltage is equal to 0.4 V and that the high supply voltage is equal to 1.8 V. These voltages are going to emerge from the power supply in their respective forms.

By outperforming WCMLS, the proposed LS is able to boost the input voltage from 0.4 V to the requisite high output voltage of 1.8 V. This may be accomplished in an efficient manner. Because of this, it is possible to generate such a high output voltage. The layout of the suggested LS makes use of transistors of an appropriate size in order to cut down on the amount of leakage current that would otherwise be present. With the exception of MP5 transistors, which have a width of 0.8 millimeters, all other transistors are required to have a width of at least 0.4 millimeters.

As it comes closer to low values for VDDL, the suggested LS will result in a delay that will reduce and get closer to 600 mV. In spite of this, it has been discovered that the delay performance of the MLS is quite consistent throughout all three scenarios.

The Fig.2 shows the energy consumption profile by employing three different PVT scenarios and values of VDDL. This was done so that the profile could be visualized. The worst-case and nominal energy performance is significantly variable for VDDL values that are less than 500 mV, whereas it only slightly lowers for VDDL values that are greater than 500 mV. This is because the voltage drop across the device is smaller for higher VDDL values.

On the other hand, the energy performance for VDDL variation is believed to be smooth and practically constant in the ideal case scenario. This is the case in the best-case scenario. The link between the static power usage and the variation in VDDL for the same three PVT circumstances is depicted in Fig.2.

The minimum amount of static power that the MLS needs is 0.82 nW, while the maximum amount that it is capable of demanding is 299 nW. However, the amount of static power that it consumes is only 20 pW, so this is something that should be taken into consideration. In Fig.2, you'll notice that the delay, energy, and static power performance of the MLS is quite resistant to changes in PVT.

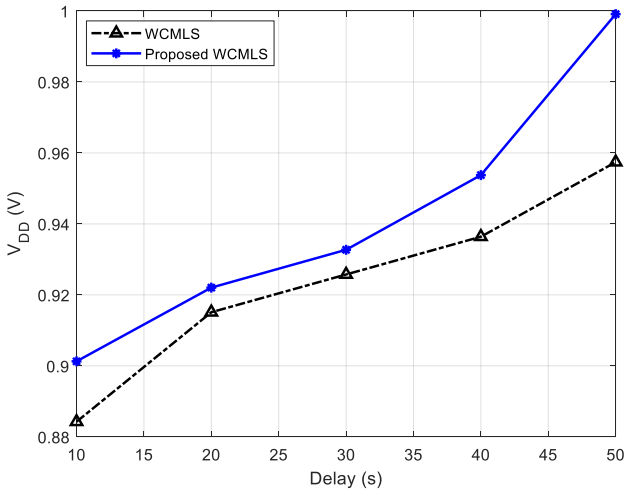

Fig.2. Delay

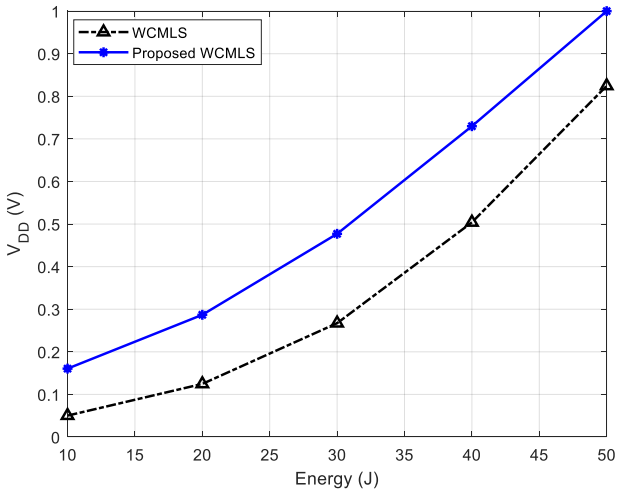

Fig.3. Energy

6. CONCLUSION

The Capacitive Load (CL) analysis makes predictions on the drive strength of the MLS for a variety of load configurations that are coupled to the Z node of the output. These predictions are made for a number of various load configurations. An increase in CL results in an improvement in both the delay performance and the energy performance of the proposed LS, which was the aim the entire time. It is also hypothesized that the MLS will exhibit some modest variation in terms of both its latency and its energy performance. This particular variation is relevant to the CL. In addition to this, research into the impact of capacitive load variation on the total average power is carried out. This is done so in order to better understand the situation. It has come to light that the MLS has a total average power usage that is comparable to that of energy and transition.

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