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AREA EFFICIENT DUAL EDGE TRIGGERED FLIP FLOP

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Abstract

Authors implement area efficient high speed dual edge triggered flip flop circuit with low power technique. PTL and CMOS technique are introduced with 45nm, 90nm technology on cadence virtuoso 16.1 gpdk model library. A comparative study of average power and delay at room temperature at .5V, .8V and 1Vhas been done. Pass transistor logic enhancing switching activity and dynamic signal driving schemes help in power consumption. By reducing number of transistor, components and clock loads performance of proposed circuit has been improved.

Keywords:

PTL Scheme, DSD Strategy, Edge Triggered Flip Flop, Clock Distribution System

1. INTRODUCTION

In this era, there is a huge demand of fast switching activity and low area implementation design circuits for memory component. This can utilize in a vast sector of VLSI, ASIC and microelectronic. In [1] [2] design of circuit have very low switching activity caused high delay dynamic power consumption. In [3] design structure number of transistors are reduced from 21 to 19. In DDFF [5] it is based on fully static operation which is modified in this paper. This design uses a very high layout area. In [6], in these paper earliest technique are, where clock gate techniques are used and it can used a large level of energy consumption. In this design power leakage is the major problem.

A theoretical approach [7] in sample test for clock gating scheme. This circuit design consist of 14 transistors and 4 inverters. This design influence the inverters to drive the input. This circuit consumes a high level of power consumption due to internal gate capacitance, wiring capacitance and also parasitic capacitance so they are extracted in layout part. This circuit contains a very large area.

A unique model structure has been introduced in [11] [12] circuit designs, BDD technique is used in [13] and SAT technique described in [14] but in these designs so many transistors are used so there is a large area generated.

Here [15] [16] is described, which mainly focused on reducing switching activity by implementation of CMOS technique. There is 1N-2P architecture (three transistor structure) mainly used. This paper used 3 C-elements which is connected to each other. In this methodology, we can use inverting and non inverting C-elements but in this paper only inverting configuration is used.

Now we reached another flip flop [17] glitch resistance flip flop which mainly worked to reduces glitches in the circuit. This circuit made by 16 transistor with one input data and one clk signal. To achieve glitch free result this circuit worked on two cases. In the first case, at node B either the glitch filter out or propagate to node Q and in the second case if the glitch is passed to the output node then it is filtered out from the feedback path. So we are starting from the initial stages, we consider 0 values for A and B and 1 values for C and D so if clk is 0 then Q is the output which is 1. now we are focusing at node A if any glitch is present at there then node A value will be changed to 1 from 0. So the new value of A is 1 and clk have previous value 0 then the output of C is 0 and if clk is 1 with the same value of A then the output D is 0. C-element circuit output B is 0 So the resulting output Q is 1. Again we assume the value of A and B is 0 and value of C, D is 1 here resulting output Q is 0 and clk is also 0. Node A value will be changed from 1 to 0 if there exist any fault. So in the 1P-2N structure there output C is 1. In another phase of 1P-2N structure A becomes 0 and clk is 1, here output deals with high impedance state therefore it follow previous state D have low value. So C-element also deals with high impedance therefore B is 1 and Q becomes 0. This paper, voltage scaling results are not valid.

For enhancing performance of power consumption [19] TSPC-DETFF is used which provides dual phase result by using fully static operation in the circuit. When clk is 1, M1-M8 acts as a buffer which is passing the value to SNP through D, in this position the output of top branch set to Q with high impedance factor and that's why transistor M17 cuts off the pull up. When clk is 0, M7 start to cutoff the pull down and M2 also cutoff the same pull down to DBP. Transistor M6 is disabled. It takes so much time which affect circuit switching activity.

Above problem is solved in [21] Conditional pass logic which is based on two types static and dynamic DFF. In static Flip Flop operation, internal node X1 is controlled by input and feedback path from another node X2 after initial triggering. But in dynamic FF operation node X1 is controlled by input only. Another node X2 is connected to pmos transistor P2. So their value is maintained by P2 and similarly Y2 is connected to nmos transistor N2. So by changing the values of N2, Y2 values are maintained. It can prevent charge sharing in both the stages. It uses positive phase and also negative phase of the clk signal. Area of this circuit structure is so high.

For reducing high area complexity we work on dual edge triggered flip flop circuit with two different ways. In first way, we apply Pass transistor logic and in second way, we apply CMOS logic with DSD strategy. Both circuits are beneficial for reducing excessive load problem, high power consumption and it enhance circuit switching activity. A very low number of transistors are used in this circuit so it would become an area efficient circuit. PTL logic helps to reduce delay between input signal and output signal which provides fast switching activity. Dynamic signal driving strategy helps to reduce power consumption of the circuit.

2. MATERIALS AND METHODS

In proposed circuit we are using PTL circuitry which is very efficient for circuit performance parameters.

1) NMOS passes strong 0 signal and weak 1 signal.

If gate terminal g is high signal (1) and input signal is low signal (0) then the output signal is strong 0.

If gate terminal g is high signal (1) and input signal is low signal (0) then the output signal is weak 1.

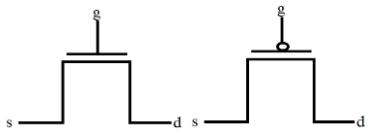

Fig.1. PTL Logic

2) PMOS passes strong 1 signal and weak 0 signal.

If gate terminal g is low signal (0) and input signal is low signal (0) then output is weak 0.

If gate terminal g is low signal (0) and input signal is high signal (1) then output is weak 1.

3. PROPOSED CIRCUIT 1

In this circuit we have designed an efficient concept of pass transistor logic. In PTL design, data can propagate simultaneously because of the complementary nature of data input and output. It will yield the performance results high in the design process. In this circuit at every rising edge of the circuit input is transferred to the output and at every falling edges same process will continue. Hence pass transistor is mainly used to minimize the consumption of power. Here at the rising edge and at the falling edge, clock power is reduced, however data is triggered at both the edges simultaneously. In most of the flip flop circuit, the distribution of clock always be a big problem hence we preferred this technique.

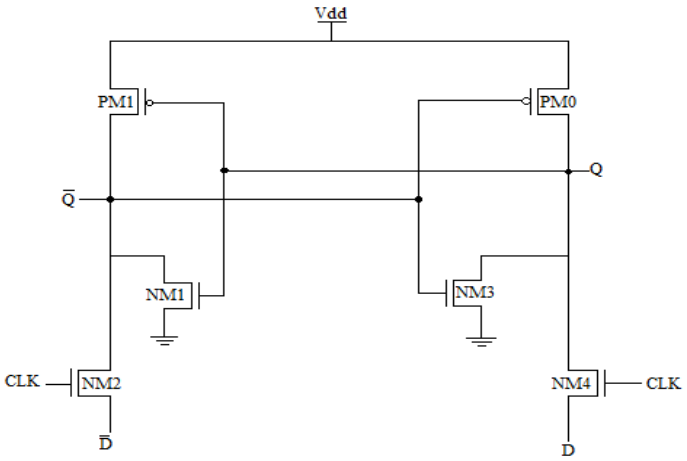

Fig.2. Schematic Diagram of Proposed Circuit 1

This design gives high performance in comparison to single-edge triggered flip flop circuit. In proposed circuit 1 we are using NMOS pass transistors. According to the logic NMOS passes strong 0 signal and weak 1 signal. When gate terminal g is high signal value (1) and input signal is low signal value (0) then the output signal is strong 0. When gate terminal g is high signal value (1) and input signal is low signal value (0) then the output signal is weak 1. This flip flop circuit used dual edge triggered flip flop which reduced delay and leads to higher operating speed. Here the proposed circuit 1 reduces area by using dual edge triggered flip flop because it triggering both positive and negative edges simultaneously. It also reduces sensitivity to pulse noise. In this flip flop circuit, we use inverters instead of CMOS gate. The input and clock both are given to the NMOS on both sides. When the input is given it starts to triggering the inverter and it triggers the data on both rising edge and falling edge. This is the reason when the clock is given the data transfer become faster. In this design we use inverters which reduces the discharging path when the data is transmitted from 1 to 0 and 0.

In this circuit, data will be sampled either data positioned at high signal or low signal i.e., at rising or falling edge of the clock. In this design, at the same operating time two data are propagated and this will reduced the operating frequency. Here we are using only six no. of transistors which affects on area optimization. So by using a very less numbers of clocked transistors, this design uses only two clocked transistors and the number of clock pulse generation transistors are significantly reduced, and it leads to power reduction.

3.1.1 Performance Analysis:

Performance parameters of proposed circuit 1 are shown below in Table.1, schematic circuit, waveform, avg. Power and layout diagram shown below in Fig.8-Fig.10.

Table.1. Parameter of Proposed Circuit 1 in 45nm at 0.5V

Parameters	Result
No. of transistors	6
No. of clocked transistors	2
Triggering mode	dual
Avg. power	1.128(µw)
D-Q delay	4.072(ps)
PDP	4.5932(fj)
Width	2.55(µm)
length	3.255(µm)
Area	8.3(µm²)

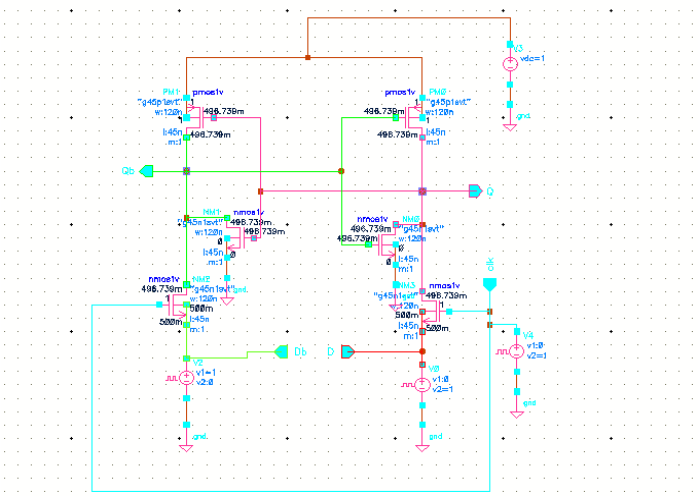

Fig.3. Schematic Circuit of Proposed Circuit 1

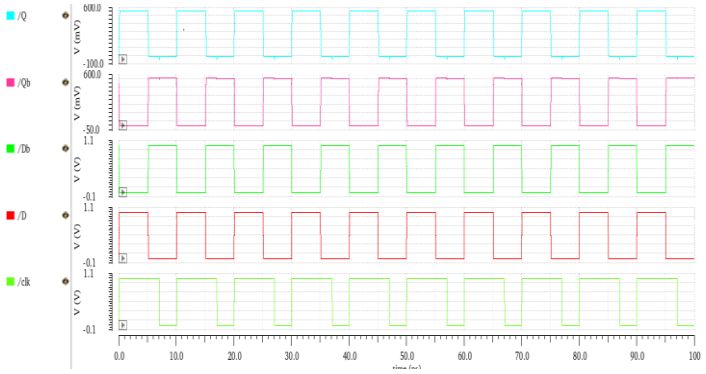

Fig.4. Waveform of Proposed Circuit 1

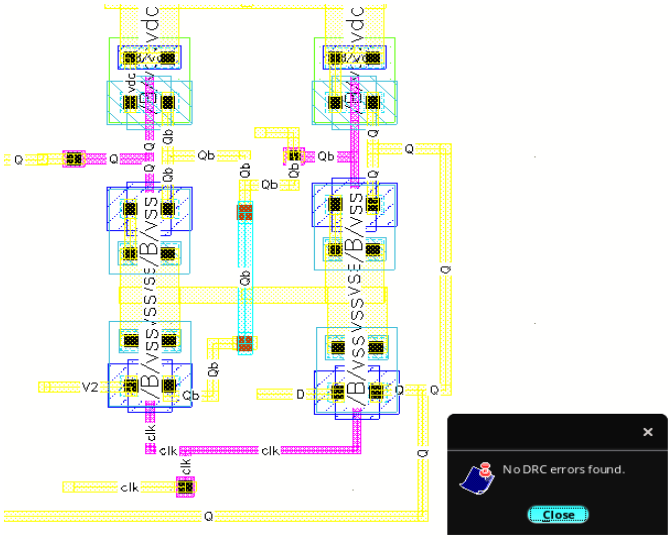

Fig.5. Simulation Result of Proposed circuit 1

Table.2. Simulation Result of Proposed Circuit 1 at 90nm and 45nm Technology

Parameters	Proposed circuit 1	Proposed circuit 1	Proposed circuit 1	Proposed circuit 1
Process Technology	90nm	90nm	45nm	45nm
Supply voltage	1V	0.8V	1V	0.5V
Avg. Power	129.8(µw)	11.83(µw)	7.86(µw)	1.128(µw)
Delay	18.94(ps)	6.76(ps)	18.43(ps)	4.072(ps)

3.2 PROPOSED CIRCUIT 2

Proposed circuit 2 consist of two states, based on dynamic signal driving scheme. The first state is latching stage and the another state is pulse generating state. In the first state we consider latching state, in this there are 4 transistor are used and one input and one clock is also used. In the second state of latching is pulse generation where two transistors, one inverter and one input driven is used. The pulse generator is used for producing ultra low pulses for both of the edges at rising edge and falling edge in the conventional based FF design which is based on CMOS design structure. This pulse generator is used to help in decreasing setup and hold time of FF circuit.

A flip flop shown in the Fig.11. Firstly we can talk about latching stage. There are two stages of latching and in the first stage of latching, in this stage there are one clock pulse clk and one input signal D. It provides two nmos in lower side and two pmos in upper side transistors where the transistor N1, P2 is used for capturing the input information and clock has been provided to the N2 and P1 for allocating the clock signal to the latching section. Clock is attached itself in the latching section, to create clock allocation tree.

For capturing the input signal, latching stage depends on the clock input data. It takes more time to capture the data. Here this design is used for reducing the delay time. This technique is advantageous for dynamic signal driving pulse of the trigger system.

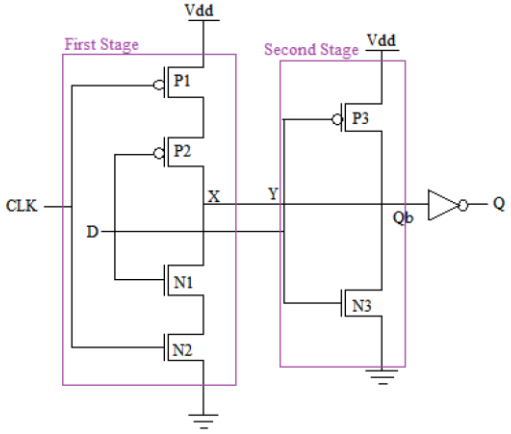

Fig.6. Schematic Diagram of Proposed Circuit 2

In the second stage we have two transistors N3 and P3 and one input data D. Here input D is used to driven transistors N3 and P3. There is a node between P2 and N1, this node denoted by X which is located at the first stage and connected to node Y in the second stage. So in this way there is no any floating node problem because of reducing the internal clock.

There are four mode of operation to perform working of circuit to work as flip flop.

In the first mode when input D goes to high is implemented and we have taken a high clock i.e. positive edge triggering is considered the PMOS transistor P1,P2 and the first stage NMOS transistors N1,N2 are in off stage and on stages respectively. This will pull down the node X to logic low. Because of the input D is high so the value D is 1, the PMOS transistor P3 gets off, and NMOS transistor N3 gets on and this will pull down the output node Y to the ground which results Qb low and Q gets high. This will result output Q is high and Qb is low.

In second mode input D is low and clock is taken to high is implemented, the transistor N1 is turned off and P2 gets on and transistor P1 is gets off and transistor N2 is in on position. Because of input have low value, node X gets also low value through transistor P2 is on state and the transistor N3, P3 goes on and off in a respective way. The output node Y gets charged through the supply voltage Vdd because of on state of P3 transistor and it will happened Qb gets high and Q gets low.

In third mode we have consider D as high input signal and the clock pulse is falling edge signal. So the transistor N1, P1 gets on and the transistors N2 and P2 gets off. Because of the high value

of the input D is 1 the PMOS transistor P2 becomes off and N1 gets on. This will makes node X will become high value signal. Due to the logical high value of the input signal D the NMOS transistor N1 becomes on and PMOS transistor P2 becomes off. This will turn node X as high signal. The transistor N3 gets on and the transistor P3 gets off because of the logical high input signal D. the output node Y pulls down into logical low by the transistor N3. This will result Q=1 and Qb=0.

In fourth mode we consider that a low input signal D is logical low value signal. The clock signal considering as logical low. Then it will become N1,N2 gets off and P1,P2 gets on. Here the node X has been charged to Vdd because of PMOS transistor P1and P2 have on state. Here is logical low input signal D which will makes N3 gets off and P3 gets on because of that the output node Y charges to Vdd through transistor P3 is in on state. This will gives the result Q gets logic signal low and Qb gets logic signal high.

3.2.1 Performance Analysis:

In performance parameters of proposed circuit 2 are shown below in Table.3 and schematic circuit, waveform are shown below Fig.7- Fig.9 respectively.

Table.3. Performance Parameters of Proposed Circuit 2

Parameter	Result
No. of transistors	8
No. of clocked transistors	1
Triggering mode	dual
Avg. power	47.45(nw)
D-Q delay	38.94(ps)
PDP	1.847(fj)
Width (Area)	4.25(µm)
Length (Area)	3.67(µm)
Area	15.59(µm²)

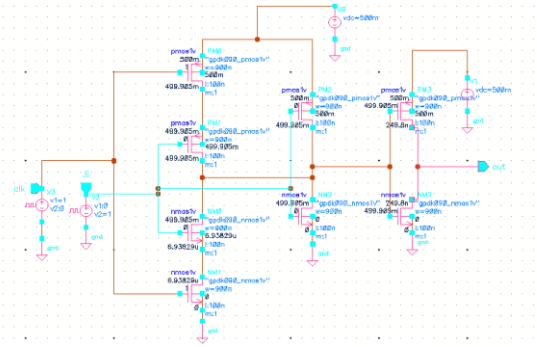

Fig.7. Schematic Circuit of Proposed Circuit 2

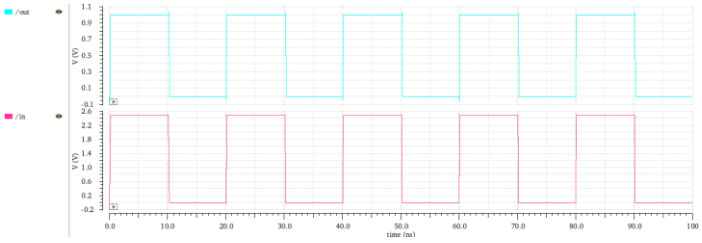

Fig.8. Transient Analysis of Proposed Circuit 2

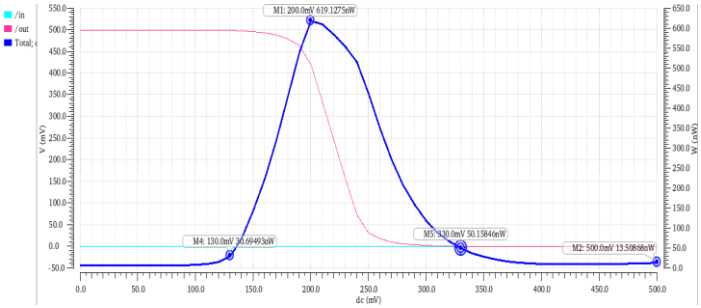

Fig.9. DC Analysis of Proposed Circuit 2

Table.4. Simulation Result of Proposed Circuit 2 at 90nm and 45nm

Parameters	Proposed Circuit 2	Proposed Circuit 2	Proposed Circuit 2	Proposed Circuit 2
Process Technology	90nm	90nm	45nm	45nm
Supply voltage	1V	0.8V	1V	0.5V
Avg. Power	81.56(nw)	30.63(nw)	47.45(nw)	15.24(nw)
Delay	50.503(ps)	134.5(ps)	38.94(ps)	554.4(ps)

Table.5. Comparison of different Circuit Results with Proposed Circuits shown below

Parameter	DSD-DETFF	CDMFF	DDFF	TSPC	Proposed Circuit 1	Proposed Circuit 2
Technology	90nm	14nm	40nm	40nm	45nm	45nm
Supply voltage	1V	1.8V	0.5V	0.5V	**0.5V**	1V
Avg. Power (µw)	7.41 (µw)	10.27 (µw)	9.72 (µw)	449.9 (nw)	3.14 (µw)	**60.98 (nw)**
Delay (ps)	51	178	166	149.9	**4.072**	38.94
No. of Transistor	6	22	19	38	**6**	8
Area (µm²)	176	429	299	High	**8.3**	10.25

Table.6. Comparison Result of Proposed circuit 1 and Proposed Circuit 2

Parameter	Technology	Supply voltage	Proposed Circuit 1	Proposed Circuit 2
Avg. Power	90	1	129.8(µw)	81.56(nw)
Avg. Power	90	0.8	11.83(µw)	30.63(nw)
Avg. Power	45	1	7.86(µw)	38.94(nw)
Avg. Power	45	0.5	**1.128(uw)**	**15.24(nw)**
D-Q delay	90	1	18.94(ps)	50.503(ps)
D-Q delay	90	0.8	6.76(ps)	134.5(ps)
D-Q delay	45	1	18.43(ps)	**38.94(ps)**
D-Q delay	45	0.5	**1.128(ps)**	554.4(ps)

4. RESULT AND DISCUSSION

The Table.2 and Table.4 represents simulation result of proposed circuit 1 and proposed circuit 2 respectively, where work is done on 90nm and 45nm technology. Proposed circuit 1 used 6 no. of transistor and 2 clocked transistors with dual edge triggering mode whereas in proposed circuit 2, only 1 clocked transistor are used and total 8 no. of transistors are used.

The Table.2 represents the simulation result of proposed circuit 1, at 90nm technology Supply voltage goes from 1V to 0.8V avg. Power reduced from 129.8(μw) to 11.83 (μw) and delay will change from 18.94(ps) to 6.76(ps). Similarly in 45nm technology supply voltage goes from 1V to 0.5V avg. Power reduces from 7.86(μw) to 1.128(μw) and delay will change from 18.43(ps) to 4.072(ps). Due to clock allocation, it will reduced D-Q delay, because of the use of PTL logic the switching activity will increase therefore a small amount of delay we can see.

Table.4 represents the simulation result of proposed circuit 2, at 90 nm technology voltage goes from 1V to 0.8V avg. Power reduced from 148.3(nw) to 30.63(nw) and delay will change from 44.85 (ps) to 134.5(ps). Similarly in 45nm technology supply voltage goes from 1V to 0.5V avg. power reduces from 47.45(nw) to 15.24(nw) and delay will also change. Due to dynamic signal driving strategy avg. Power consumption is very less.

In Table.5 we compare proposed circuit with different flip flop on basis of technology, supply voltage, power, delay and area.

In compare to CDMFF DDFF DSD-DETFF proposed circuit 1 improved 69.42% 67.69% 57.62% avg. power consumption respectively and proposed circuit 2 improved 99.40% 99.37% 99.17% avg. power consumption respectively.

In section of delay proposed circuit 1 and 2 improved switching activity in a very high manner so their D-Q delay is very less in compare to CDMFF DSD-DETFF DDFF.

Proposed circuit 1 uses only 6 no. of transistor which utilize area, proposed circuit 2 also utilize area it uses only 8 no. of transistor. In compare to CDMFF DSD-DETFF DDFF which uses 22,6,19 respectively, proposed circuits uses less area.

Performance analysis of area occupied of proposed circuit 1 used 98.06%, 95.28%, 97.22% less and proposed circuit 2 used 97.61%, 94.17%, 96.57% less than CDMFF DSD-DETFF and DDFF at 45nm technology.

The Table.6 shows performance of comparison result at 90nm and 45nm technology on varying voltage. In 90nm, 1V and 0.8V proposed circuit 2 consumes 99.88%, 99.74% less avg. Power consumption than proposed circuit 1 respectively. Similarly in 45nm at 1V and 0.5V proposed circuit 2 consumes 99.51%, 98.67% less avg. Power consumption than proposed circuit 1.

In section of delay proposed circuit 1 consumes less delay than proposed circuit 2. If we reduce supply voltage from 1V to 0.5V, delay of proposed circuit 2 will decrease but in same case delay will increase in proposed circuit 1. So 1V is best for circuit switching activity for proposed circuit 2 and 0.5V for proposed circuit 1.

5. CONCLUSION

In this paper we simulate D flip flop circuit with two different technique PTL and CMOS. where both circuit results are efficient. First technique enhances circuit switching activity so there D-Q delay is very low at 0.5V, 45nm technology only 1.128(ps). This scheme also utilizes area by reducing no. of transistor, only 8.3(um^2) is used. Whether cmos scheme also utilizes area only 8 transistor are used. But only drawback in PTL scheme we analyze that in there voltage level degradation is performed which we improved in CMOS scheme. Also CMOS scheme used an efficient power consumption due to DSD strategy and lesser component it consumes only 60.98(nw) average power which is growing factor for any circuit.

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