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DESIGN OF MOSFET-C BASED FLOATING INDUCTANCE USING CFOA

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Abstract

A configuration to simulate a lossy/lossless floating inductor has been presented using CMOS CFOAs, VCRs, and capacitors. This configuration is completely programmable/ tunable because of the employment of VCRs and works on 0.35μm TSMC CMOS technology. To demonstrate the workability of an inductor, two filters, 1) second-order notch filter and 2) fourth-order Butterworth low-pass filter, have been realized. All designs have been simulated on PSPICE and the results verify the ideality of the circuit.

Keywords:

Floating Inductor (F.I.), CMOS Current-Feedback Operational Amplifier (CFOA), Voltage-Controlled Resistance (VCR), Notch Filter, Butterworth low-pass Filter

1. INTRODUCTION

Nowadays, inductance simulation is a generous topic of research because of the requirement for inductor-less networks in integrated circuits as simulated inductor provides a more stable and less sensitive realization of networks, researchers are presenting inductance simulation circuits using different active building blocks (ABBs) either CM or VM, need of inductance simulation design is due to the size and bulkiness of coiled inductor which dissipates a large amount of power and energy. Active inductors are designed as grounded inductors (G.I.s) or floating inductors (F.I.s) which are either lossy or lossless, lossless G.I.s /F.I.s are pure inductors and can be used exactly like coiled inductors and lossy G.I.s /F.I. are the combination of inductor and resistor/ capacitor either in series or parallel form. Analog signal processing circuits such as filters and oscillators are designed with either G.I.s or F.I.s where these inductors can be replaced by actively simulated inductors and work more efficiently compared to coiled inductors. Therefore, simulation of inductors using RC networks with any active device has been an alternate choice for realizing inductor-based circuits in integrated circuit (IC) form.

Lossless/lossy G.I.s /F.I.s have their own benefits in different applications as in where need to replace pure grounded or floating inductors we replace it by lossless G.I.s/ F.I.s and where need to replace with the combination of inductor and series/ parallel resistor/capacitor replace it by lossy G.I.s /F.I.s. Lossless F.I. is mainly used in LC ladder filters were replacing each inductor in a conventional LC ladder filter with a circuit that simulates an inductor, makes it more stable, less sensitive to passive component tolerances, and has a larger dynamic range. A large number of inductance simulators have been presented in the literature [1]-[26] and the references are cited therein use a wide range of commercially available active building blocks such as an operational amplifier and current-feedback operational amplifier (CFOA), and commercially unavailable other active elements. A traditional operational amplifier (OA) based simulated inductors had been investigated whose description has been given from [1]-[3] [6] [7] but gain bandwidth dependency and requirement of a large number of components were the main disadvantages here. Operational Transconductance Amplifiers (OTAs) were used to simulate inductors which have been described in [5] [8]. The main advantage of this device was that its transconductance gain gm can be varied by external bias current I_{bias} which provides electronic tunability but it was thermally unstable. After that Current mode device called Current Conveyor (CC) got more popular with remarkable features like high bandwidth independent of closed-loop gain and higher slew rate. Simulated inductors and other impedance functions using second-generation current conveyor (CCII) have been cited in references [4] [11].

From the last two to three decades, current-feedback operational amplifier (CFOA) integrated circuits have mainly been used by researchers with more interest because these circuits reveal better performance, more linearity, particularly higher speed and better bandwidth. ICs of CFOAs are made up of BJT, CMOS, or BiCMOS among which CMOS ICs are more beneficial as CMOS consumes less power and allows the increasing density of transistors in the circuit, and is more stable in higher temperatures. Many simulated inductance functions have been realized using CFOAs, some of them, related to inductor simulation have been cited in the references from [9] [12] [14] [16] [18] [26]. It can be observed that CFOAs that have been used so far to simulate floating inductors were mostly greater than two in number and BJT architectured of AD844 type. Even MOS-C based inductor simulator mentioned in [13] did not use CFOA as a building block. Therefore, no such inductor simulator circuit has so far been presented which is based on MOSFETs and capacitors only. Therefore, a lossless floating inductor simulator has been presented which is a modification of R. Senani's & D. R. Bhaskar's earlier mentioned floating inductor circuit from [19] which performs just according to the previous design but with better results.

2. DESIGN OF MOSFET-C BASED FLOATING INDUCTOR

A configuration of the floating inductor has been shown in Fig.1 which consists of BJT CFOA and passive components. This circuit has been modified and the new design consists of two CMOS CFOAs instead of BJT CFOA of AD844 type. The CMOS CFOA has been taken from [16] given in Fig.1 and BJT CFOA has been replaced by this CMOS CFOA because of less area consumption, low power dissipation, and higher slew rate of CMOS CFOA over BJT CFOA. One more modification has been done which is the replacement of all passive resistors with voltage-controlled resistors (VCRs), mentioned in [27] which provide tunability to the design with the reduction in area.

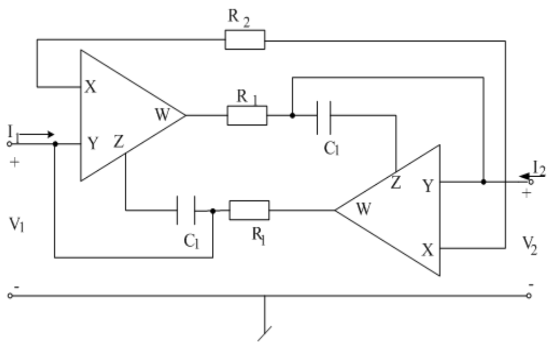


Fig.1. Floating Inductor Configuration [19]

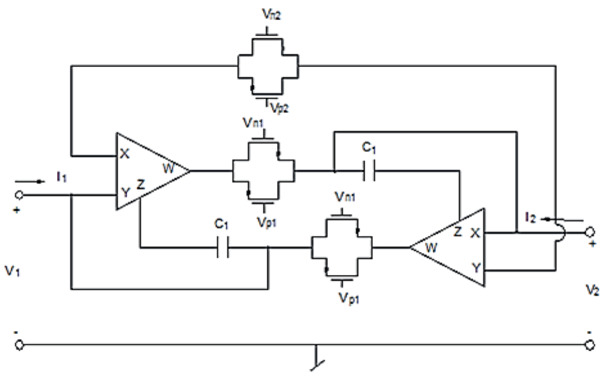


Fig.2. Resistorless Floating Inductor Configuration

The designed MOSFET-C based Floating Inductor (FI) has been shown in Fig.2 consisting of only MOS transistors and capacitors. This type of inductor is called MOSFET-C based floating inductor as it contains only MOSFETs and capacitors. This idea is also useful from IC implementation point of view as passive components are not being employed, so, it saves more area and less power dissipation because of simulated resistor usage.

2.1 IDEAL ANALYSIS OF SIMULATED INDUCTOR

Assuming CFOAs to be characterized by $i_y = 0$; $v_x = v_y$; $i_z = i_x$ and $v_w = v_z$. By analyzing the circuit given in Fig.1, we obtain Y-parameters as shown below.

$$[Y]=\left[\left(\frac{1}{R_1}-\frac{1}{R_2}\right)+\frac{1}{sC_1R_1R_2}\begin{bmatrix}1 & 1\\ -1 & 1\end{bmatrix}\right] \quad (1)$$

For $R_1<R_2$, the circuit simulates a floating parallel R-L admittance with equivalent resistance and equivalent inductance values which have been given below.

$$\frac{1}{R_{eq}}=\frac{1}{R_1}-\frac{1}{R_2};L_{eq}=C_1R_1R_2 \quad (2)$$

where,

$$R_i=\frac{(V_1-V_2)}{I}=\frac{1}{K_0\left(V_{ni}-V_{pi}-V_{tn}-V_{tp}\right)} \quad (3)$$

This is the resistance of MOSFET-based VCR [27], on observing Eq.(2), we get that equivalent inductance is dependent on two resistors R_1 and R_2. Hence by varying any one of them or both we can obtain a variable equivalent inductance value.

In order to vary the resistance of VCR, one of its two voltages V_n or V_P is varied by keeping the other voltage constant. Normally we apply a voltage of -0.9V at V_P and different-different values on V_n to make that particular resistance vary.

For R_1=R_2=R_0, the circuit simulates a lossless F.I. with an equivalent inductance value which has been taken from [19].For one matching condition, the circuit simulates a lossless floating inductor.

$$L_{eq}=C_1R_0^2 \quad (4)$$

This is the case when CFOAs have been taken as the ideal which means no input resistance of inverting terminal *X* i.e. R_X and no output impedance (parallel combination of parasitic resistance, R_P=3MΩ, and parasitic capacitance, C_P=3.5pF-4.5pF) at Z-terminal have been considered. Therefore, equivalent resistance and equivalent inductance are constant and independent of the frequency term.

2.2 NON-IDEAL ANALYSIS OF SIMULATED INDUCTOR

If we consider parasitic resistances and impedances of CFOA then Y-parameters according to [19] would be symmetrical and dependent on frequency as shown below:

$$Y'_{11}=Y'_{22}=\frac{1}{R_1}+\frac{sC_1}{\left(1+sC_1Z_p\right)}+\frac{Z_p}{\left(1+sC_1Z_p\right)\left(R_1R_2+2R_1R_X\right)} \quad (5)$$

$$Y'_{12}=Y'_{21}=-\left[\begin{array}{l}\dfrac{sC_1Z_p}{R_1\left(1+sC_1Z_p\right)}+\dfrac{sC_1Z_p}{\left(1+sC_1Z_p\right)\left(R_2+2R_X\right)}\\ +\dfrac{Z_p}{\left(1+sC_1Z_p\right)\left(R_1R_2+2R_1R_X\right)}\end{array}\right] \quad (6)$$

It may be seen that with $Z_P\rightarrow\infty$ and $R_X\rightarrow 0$, the y-parameters in Eq.(5) and Eq.(6) reduce to those in Eq.(1). From the non-ideal terms of the y-parameters of the proposed circuit, it may be easily envisioned that the high-frequency presentation would be affected because of these parasitic impedances. However, this is a common drawback exhibited by all inductance simulation circuits known so far and hence, is not a problem with our circuit only.

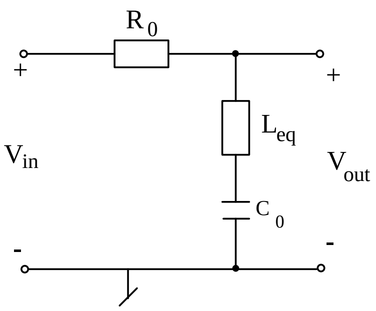
3. APPLICATIONS OF MOSFET-C BASED F.I.

Now some applications have also been presented in the support of this simulator design in order to demonstrate its workability of it in some applications.

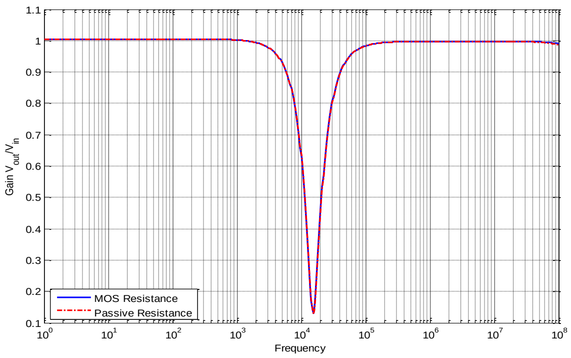
3.1 SECOND ORDER NOTCH FILTER

A second-order notch filter using RLC components has been shown in Fig.3(a) with component values taken as C_1 = 1 nF, C_0 = 0.1 nF, R_1 = R_2 = 1 kΩ, R_0 = 0.1 kΩ corresponding to the design parameters of the filter as f_0 = 15.9kHz, H_0 = 1 and bandwidth = 15.9kHz. The simulated frequency response of the notch filter using CMOS CFOAs, VCRs, and biased with ±1.25V DC power supplies is shown in Fig.3(b). Another frequency response of the same filter which uses CMOS CFOAs and passive resistance has also been shown in the same plot. We can visualize that both responses are similar to each other which means we achieve the same behavior of the circuit by replacing passive resistors with simulated MOS resistors which reduce significant area. The response is found to be in reasonably good agreement with the previous response given in [19] and thus, confirms the workability of the circuit as an FI.

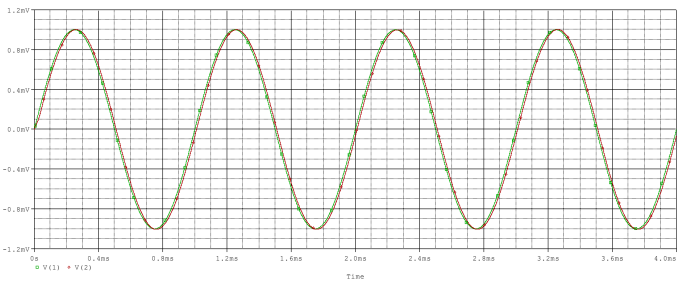
Transient behavior of the same circuit has also been simulated for the same values of components on PSPICE has been shown in Fig.3(c).



(a)



(b)



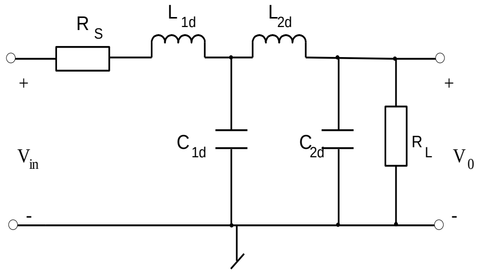
(c)

Fig.3.(a) Second Order RLC Notch Filter, (b) Frequency Response of Notch Filter, (c) Transient Response of Notch Filter

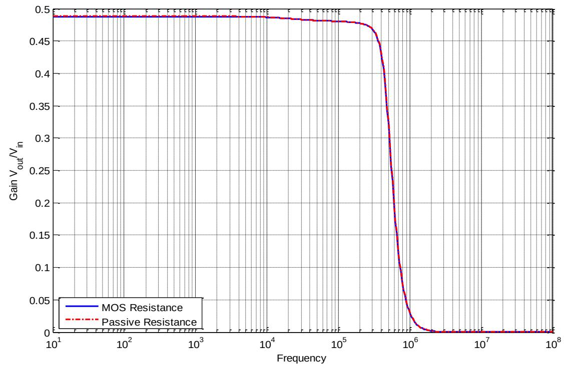
4. FOURTH ORDER BUTTERWORTH LOWPASS FILTER

The circuit configuration of fourth order LC ladder Butterworth lowpass filter has been shown in Fig.4. The filter with a cutoff frequency of 500 kHz has been designed. The component values, after appropriate frequency and impedance scaling, has been taken as $R_s = R_L = 1$ kΩ, $L_{1d} = 0.2437$ mH ($R_1 = R_2 = 1.561$ kΩ and $C_1 = C_2 = 0.1$ nF), $C_{1d} = 0.5884$ nF, $L_{2d} = 0.5884$ mH ($R_1 = R_2 = 2.425$ kΩ and $C_1 = C_2 = 0.1$ nF), $C_{2d} = 0.2437$ nF. CMOS CFOAs are biased with DC power supplies of ±1.25V. The circuit has been simulated on PSPICE for two cases and their frequency responses have been plotted. In case one, the inductor uses CMOS CFOAs with VCRs but in the second case, passive resistors have been used instead of VCRs. Both frequency responses have been compared through MATLAB and have been shown in Fig.5. We can see that both responses are the same and identical to the response given in [19].

Transient behavior of the same circuit has also been simulated on PSPICE and has been shown in Fig.6.



(a)



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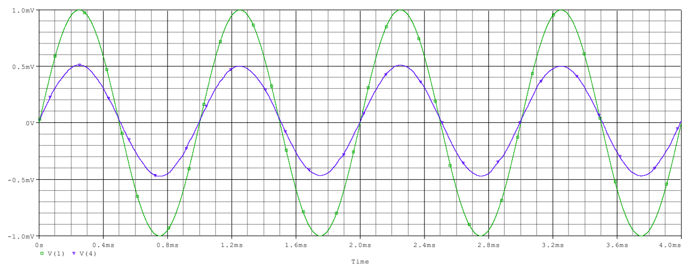

(c)

Fig.4.(a) Fourth Order Butterworth Lowpass Filter, (b) Frequency Response of Butterworth Lowpass Filter, (c) Transient Response of Butterworth Lowpass Filter

5. ADVANTAGES OF MOSFET-C BASED F.I. OVER CONVENTIONAL F.I.

The main advantage of MOSFET-C based FI includes the usage of voltage controlled resistance instead of passive resistors which results in fully integrated continuous time filters which are widely used in wireless communication as portable terminals. The CMOS architectured CFOA replaces BJT-based AD844 type CFOA. Thus fully integrated filters without any external passive resistor elements are very effective in reducing their cost, size, and power dissipation.

Table.1. Comparison of presented F.I. with earlier published F.I.

Reference Number/Published Year	Active Building Block Used	Number of Active Building Blocks Used	Number of Passive Resistors Used	Number of Passive Capacitors Used	Tunability	Type of Device
[2]/1974	O.A.	2	3	2	NO	BJT
[3]/1977	O.A.	2	9	1	NO	BJT
[4]/1979	CCII	1	2	1	NO	BJT
[5]/1983	OTA	4	-	2	No	BJT
[6]/1986	O.A.	2	4	1	NO	BJT
[7]/1989	O.A.	2	4	1	NO	BJT
[9]/1996	CFOA	1	4	2	NO	BJT
[11]/2003	CCII	6	4	1	No	BJT
[12]/2007	MCFOA (equivalently 3 CFOAs)	1	2	1	NO	CMOS
[14]/2008	MCFOA (equivalently 3 CFOAs)	2	2	1	NO	CMOS
[15]/2008	CFOA	4	4	1	NO	BJT
[16]/2009	CFOA	4	3	1	No	CMOS
[17]/2010	FDCCII	1	2	1	YES	CMOS
[18]/2011	CFOA	1	2	1	NO	BJT
[19]/2012	CFOA	2	2	1	NO	BJT
[21]/2015	CFOA	3	2	1	NO	BJT
[22]/2015	CFOA	1	2	1	NO	CMOS
[23]/2016	CFOA	3	2	1	YES	BJT
[25]/2017	CFOA	2	2	1	NO	BJT
[26]/2019	CFOA	2	2	1	NO	BJT
Presented Design	CFOA	2	0	2	Yes	CMOS

Another advantage of the designed floating inductor is its tenability which was absent in conventional FI. In this case, the equivalent inductance value can be varied as its MOSFET-based resistance is voltage controllable. One more advantage that we observed here is the difference between cut-off frequencies calculated theoretically and practically is less in the case of MOSFET-C based FI as compared to conventional FI given in [19] for the same gain value. Frequency responses of both filters have been shown in Fig.3(b) and Fig.4(b) respectively. That means this configuration shows more accuracy as compared to the conventional one.

6. CONCLUSION

A MOSFET-C based floating inductor has been presented using CMOS CFOAs, VCRs, and capacitors. This floating inductor is completely programmable or tunable because of the employment of VCRs. CMOS CFOA has improved the performance of the device with respect to area consumption, power dissipation, accuracy, and speed. The filters realized using this new proposed circuit have good linearity and less error with respect to cut-off frequency. The modified circuit has the following features:

- Only two CMOS CFOAs are used in compare to previously known BJT CFOA of AD844 type-based F.I.s of [15] [21] [23] needing three to four CFOAs.
- The elasticity of realizing either lossless or lossy F.I. from the similar circuit.
- Employment of three voltage-controlled resistances (VCRs) made of MOSFET provides electronic tunability to the design.
- Requirement of only two capacitors and no passive resistor.
- In case of lossless F.I. realization there is simple component-matching condition.

The applications of the MOSFET-C based F.I. configuration have been demonstrated through the implementation of a second-order notch filter and a fourth-order Butterworth low pass filter using PSPICE simulations using CMOS CFOA, VCRs, and capacitors.

REFERENCES

[1] D. R. Wise, "Active Simulation of Floating Lossy Inductances", *Proceedings of the IEEE*, Vol. 121, No. 2, pp. 85-87, 1974.

[2] D.S.C. Roy, "A Circuit for Floating Inductance Simulation", *Proceedings of the IEEE*, Vol. 121, No. 1, pp. 521-523, 1974.

[3] Q.L. The and T. Yanagbawa, "Some New Lossless Floating Inductance Circuits", *Proceedings of the IEEE*, Vol. 65, No. 7, pp. 1071-1072, 1977.

[4] V. Singh, "A New Active-RC Circuit Realization of Floating Inductance", *Proceedings of the IEEE*, Vol. 67, No. 12, pp. 1659-1660, 1979.

[5] R. Senani, "On the Synthesis of a Class of Immittances and Filters Using Grounded Capacitors", *Letters to the Editor*, Vol. 43, No. 1, pp. 410-415, 1983.

[6] V.D.C. Grunigen, D. Ramseier and G.S. Moschytz, "Simulation of Floating Impedances for Low-Frequency Active Filter Design", *Proceedings of the IEEE*, Vol. 74, No, 2, pp. 366-368, 1986.

[7] V. Singh, "On Floating Impedance Simulation", *IEEE Transactions on Circuits and Systems I*, Vol. 36, No. 1, pp. 161-162, 1989.

[8] I.A. Khan, T.M. Ahmed and N. Minhaj, "Novel Technique for Immitance simulation Realisation of Some All-Active Simulators", *International Journal of Electronics*, Vol. 72, pp. 431-441, 1992.

[9] A.M. Soliman, "Applications of the Current Feedback Operational Amplifier", *Analog Integrated Circuits and Signal Processing*, Vol. 11, pp. 265-302, 1996.

[10] R. Senani, "Realization of a Class of Analog Signal Processing/Signal Generation Circuits: Novel Configurations using Current Feedback Op-Amps", *Frequenz*, Vol. 52, No. 9-10, pp. 196-206, 1998.

[11] G. Ferry, N.C. Guerrini and M. Diqual, "CCII-Based Floating Inductance Simulator with Compensated Series Resistance", *Electronics Letters*, Vol. 39, No. 22, pp. 1-13, 2003.

[12] E. Yuce, "On The Implementation of the Floating Simulators Employing a Single Active Device", *International Journal on Electronics and Communications*, Vol. 61, pp. 453-458, 2007.

[13] T. Sato, S. Takagi and N. Fujii, "A Design of MOSFET-C Impedance Simulation Circuits Based on a GIC", *Proceedings of the IEEE*, Vol. 182, pp. 547-555, 2007.

[14] E. Yuce and S. Minaei, "A Modified CFOA and its Applications to Simulated Inductors, Capacitance Multipliers, and Analog Filters", *IEEE Transactions on Circuits and Systems I*, Vol. 55, No. 1, pp. 266-275, 2008.

[15] C. Psychalinos, K. Pal and S. Vlassis, "A Floating Generalized Impedance Converter with Current Feedback Operational Amplifiers", *AEU International Journal of Electronics and Communications*, Vol. 62, pp. 81-85, 2008.

[16] R. Senani, DR. Bhaskar, S.S. Gupta and V. K. Singh, "A Configuration for Realizing Linear, Voltage-Controlled Resistance, Inductance and FDNC Elements", *International Journal of Circuit Theory and Applications*, Vol. 37, No. 5, pp. 709-719, 2009.

[17] F. Kacar, "New Lossless Inductance Simulators Realization Using A Minimum Active And Passive Components", *Microelectronics Journal*, Vol. 41, pp. 109-113, 2010.

[18] F. Kacar and H. Kuntman, "CFOA-Based Lossless and Lossy Inductance Simulators", *Radio Engineering*, Vol. 20, No. 3, pp. 627-631, 2011.

[19] R. Senani and D. R. Bhaskar, "New Lossy/Loss-Less Synthetic Floating Inductance Configuration Realized with only two CFOAs", *Analog Integrated Circuits and Signal Processing*, Vol. 73, pp. 981-987, 2012.

[20] S. Minaei and E. Yuce, "A Simple CMOS-Based Inductor Simulator and Frequency Performance Improvement Techniques", *International Journal on Electronics and Communications*, Vol. 66, pp. 884-891, 2012.

[21] M.T. Abuelmaatti and S.K. Dhar, "New CFOA-Based Floating Lossless Negative Immittance Function Emulators", *Proceedings of the IEEE*, Vol. 189, No. 3, pp. 1-13, 2015.

[22] H. Alpaslan and E. Yuce, "Inverting CFOA Based Lossless and Lossy Grounded Inductor Simulators", *Circuits, Systems, and Signal Processing*, Vol. 34, No. 10, pp. 3081-3100, 2015.

[23] M.T. Abuelmaatti and S.K. Dhar, "New CFOA-Based Floating Immittance Emulators", *International Journal of Electronics*, Vol. 14, No. 2, pp. 1-14, 2016.

[24] L. Zhong, X. Lai, D. Xu, M. Short, B. Yuan and Z. Bing, "An Improved CMOS-Based Inductor Simulator with Simplified Structure for Low-Frequency Applications", *Journal of Computational Electronics*, Vol. 15, No. 3, pp. 1-14, 2016.

[25] M.T. Abuelmaatti, S.K. Dhar and Z.J. Khalifa, "New Two-CFOA-based Floating Immittance Simulators", *Analog Integrated Circuits and Signal Processing*, Vol. 91, No. 3, pp. 479-489, 2017.

[26] M.T. Abuelmaatti, Z.J. Khalifa and S.K. Dhar, "New CFOA-Based Lossless Floating Inductor and Capacitance/Resistance Multipliers for Low Frequency Applications", *Journal of Active and Passive Electronic Devices*, Vol. 14, No. 2-3, pp. 229-237, 2019.

[27] M.S. Al-Shahrani, "A Novel CMOS Wideband Auto-Tuining Phase Shifter Circuit", *Proceedings of International Conference on Electronics, IEEE, Circuits and Systems*, pp. 649-652, 2007.