ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2022.0237

A NOVEL QUASI-BALLISTIC DRAIN CURRENT MODEL VALID FOR SYMMETRIC QUADRUPLE GATE (QG) NANOSCALE MOSFET

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Abstract

Conventional bulk MOSFETs are being replaced by potentially efficient multi-gate devices in very large scale integrated technology. Multi-gate MOSFETs offer better channel control and exhibit excellent scaling ability in the nanoscale regime. A Quadruple Gate (QG) MOSFET which is a prime variant of multi-gate MOSFETs is believed to provide better electrostatic integrity compared to a Double Gate (DG) MOSFET because of the gate surrounding the channel completely. Due to the structural advantage in a QG MOSFET, scattering effects are reduced and better quasi-ballistic behaviour is observed in the nanoscale regime. This work proposes a quasi-ballistic drain current model applicable for state of art symmetric QG MOSFET structures in the nanoscale regime. The proposed model evolves from the well known Natori's ballistic theory and nanoscale carrier scattering theory. The drain bias dependency on the critical carrier scattering length is explored and applied to the proposed model successfully. The simulation results obtained demonstrate that the proposed model is physically apt, exhibits continuity in all regions of the device operation and hence can be adopted in multi-gate compact models for circuit simulation applications.

Keywords:

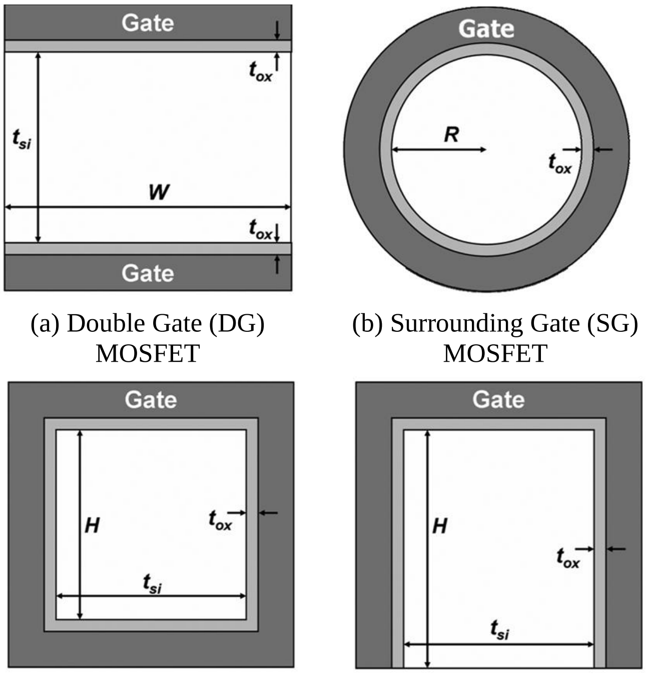
Quadruple Gate MOSFET, Quasi-Ballistic Transport, Carrier Scattering, Compact Modeling

1. INTRODUCTION

Multi-gate MOSFETs are considered as better potential candidates over conventional bulk MOSFETs due to their excellent scaling ability much beyond the bulk CMOS channel length limits [1]. The multiple gates in these device structures offer a high current driving capability [2] and better control ability over the short channel effects. Double-gate (DG), triple-gate (TG), quadruple-gate (QG) and surrounding-gate (SG) MOSFETs are some of the important variants in multi-gate MOSFETs [3] that are currently being subjected to intense research.

The Fig.1 shows different schematic variants of multi-gate MOSFETs with their cross-sections perpendicular to the channel direction. Among these structures, DG MOSFETs and TG MOSFETs are most feasible in terms of technology. However, in theory, QG MOSFETs and SG MOSFETs are believed to offer best electrostatic integrity due to their structural advantages. In both these device variants, the gate surrounds all around the basic structure that leads to robust channel control and reduction of short channel effects. Further, owing to the volume inversion effect [4] and inherent structural advantages, QG and SG MOSFETs are believed to offer lesser carrier scattering and better quasi-ballistic behaviour in the nanoscale regime.

An exhaustive review on compact modelling of multiple gate MOSFETs is given in [5]-[7]. These models are of closed form and provide analytic potential solutions to the Poisson's and the current continuity equations for DG and SG



(a) Double Gate (DG) MOSFET

(b) Surrounding Gate (SG) MOSFET

(c) Quadruple Gate (QG) MOSFET

(d) Triple Gate (TG) MOSFET

Fig.1 Schematic of various Multi-gate MOSFET cross-sections perpendicular to the channel direction [7].

MOSFETs, with accurate explicit functions. Moreover, these models exhibit excellent continuity in all regions of device operation. A unified multi-gate model is derived in [7] from the core long channel compact model and further extended to the QG and TG variants. The models presented in [5], [6] and [7] are perfectly valid in the long channel regime which are further modified to include the short channel effects [8] and quantum effects. However, these long channel models clearly over predict the drain current [9] in the short channel regime, which is visibly higher than the ideal ballistic limit proposed by Natori [10]. In the nanoscale regime, drift-diffusion transport alone is not sufficient to explain the complete device physics. Drift–diffusion transport models fail to capture the velocity overshoot, while the energy transport models [11] ignore certain details in the ballistic limit. In a long channel device, the maximum drain current is limited by pinch-off, whereas in a short channel device it is first the velocity saturation and later the source injection velocity that limits the drain current. Modern state of art nanoscale devices exhibit quasi-ballistic phenomena [12], because the maximum drain current is restricted by the rate at which carriers are injected from the source. This condition implies for the need to include both diffusive and the ballistic transports appropriately with the inclusion of scattering physics. The recent work undergone by Vyas *et.al* in [13] and [14] demonstrates carrier scattering dependency at the critical layer near the low field source region on the drain current characteristics. This dependency is derived from the scattering theory in terms of transmission and reflection coefficients. However, the quasi-ballistic models proposed in [13] and [14] are applicable to DG MOSFETs only.

A Quadruple Gate MOSFET offers better electrostatic integrity than a DG MOSFET due to its advantage of the gate surrounding all around the device structure [4]. Hence, a relevant Quadruple Gate MOSFET model valid in the nanoscale regime is highly preferred and recommended for state of art compact modeling applications. This work proposes a semi-ballistic drain current model applicable for a nanoscale QG MOSFET. The proposed model evolves from the quasi-ballistic DG model [14] which is suitably modified as per the structural refinements applicable for QG MOSFET. As the proposed QG model evolves from the nanoscale DG model [14], it inherits all the advantages of the explicit DG Taur model [15] without neglecting the essential physics. The core part of the proposed model is derived directly from the Pao-Sah integral with undoped or lightly doped silicon body without considering the charge sheet approximation. The proposed QG model includes the concepts of scattering theory pertaining to nanoscale transistors. In the subsequent sections, it is demonstrated that the proposed QG model includes all the essential physics and the results show its validity in the diffusive, quasi-ballistic and ballistic limits. Section 2 provides the mathematical background and the analytical approach of the proposed work. Section 3 discusses the results obtained for the proposed model. Conclusion is finally done in section 4.

2. MODEL DESCRIPTION

The proposed model partly evolves from the well-known Natori's ballistic model, which is further modified from fully ballistic to a quasi-ballistic model by considering the physics of scattering theory in terms of transmission and reflection co-efficients applicable to a QG MOSFET device. The device schematic in Fig.1(c) is taken as the reference structure for the proposed QG MOSFET model development. A symmetrical QG structure is chosen, because it greatly simplifies the mathematical analysis and modeling steps in the development of compact models. The silicon film is presumed to be lightly doped and fully depleted so that the discrete dopant fluctuations are avoided. The proposed schematic considers n^+ polysilicon gate all around so that lower threshold voltages are achieved. The all-around gate structure has identical work function, giving rise to a quadruple shaped inversion channel (top, bottom and two sides), that switches at a common gate potential.

The drain current for a complete ballistic bulk MOSFET (Natori's model [10]), under non-equilibrium conditions is expressed in Eq.(1) as:

$$I_{ds,bulk} = G\left[F_{1/2}(\xi) - F_{1/2}\left(\xi - \frac{V_{ds}}{v_T}\right)\right] \quad (1)$$

where $\xi = \left(\frac{E_{fs} - E'_c - E_0}{kT}\right)$ and parameter $G = \frac{8\sqrt{2m_t}qW(kT)^{3/2}}{h^2}$.

Eq.(1) is derived from the concept of flux theory. The Fermi-Dirac integral expression in the brackets for ξ is obtained from [12] and given below as:

$$\left(\frac{E_{fs} - E'_c - E_0}{kT}\right) = \ln\left[\frac{1}{2}\left\{\sqrt{\left(e^{V_{ds}/v_T} - 1\right)^2 + 4\exp(g)} - 1 - e^{\frac{V_{ds}}{v_T}}\right\}\right] \quad (2)$$

where g is another intermediate parameter expressed as:

$$g = \left(\frac{h^3\varepsilon_{ox}\left(V_{gs} - V_t\right)}{4\pi qkTt_{ox}m_t} + \frac{V_{ds}}{v_T}\right) \quad (3)$$

In the above equation, h is the Plank's constant, thermal voltage $v_T = kT/q$ and electron effective mass in the transverse direction $m_t = 0.19m_0$ where m_0 is the free electron mass. Eq.(2) and Eq.(3) conceptually relate the energy band diagram of nanoscale MOSFET illustrated in Fig.2. All the terms and notations given in Eq.(2) and Eq.(3) are similar to the ones mentioned in [13] and [14].

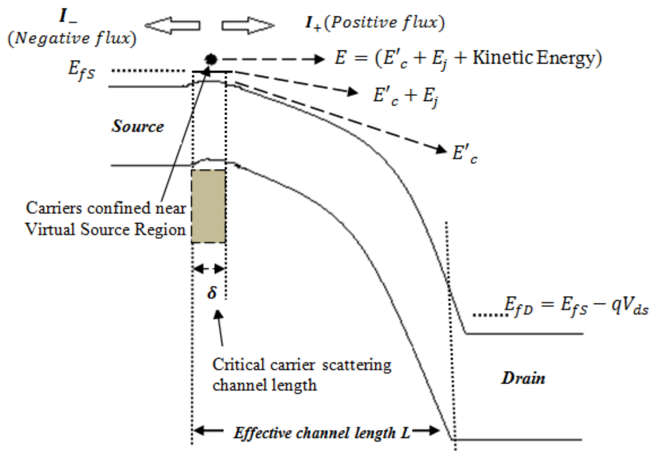


Fig.2 Schematic of a nanoscale MOSFET band diagram under high-drain bias conditions [9]. The highlighted section near the virtual source is the critical carrier scattering channel length.

In the schematic of Fig.2, E_{fS} and E_{fD} denote degenerately doped source and drain Fermi levels respectively (denoted by dotted lines), I_- and I_+ are left to right and right to left current components respectively based on the concept of flux theory. Going by the physics of ballistic transport theory [7] and referring to Fig.2 it is evident that the highest potential barrier is near the source where the carriers populate with allowed discrete sub-bands. At the top of the barrier the vertical component of the electric field is nearly zero, hence velocity saturates at that position (virtual source). Carriers that are confined in the inversion layer occupy discrete sub-bands with a minimum energy E_j above conduction band E'_c .Further, the energy level $E = (E'_c + E_j + \textit{Kinetic Energy})$.

The Eq.(1) represents the net drain to source current with one sub-band approximation, with the lowest sub-band being j=0 of un-primed valley. Using Blakemore's explicit analytical model [17], the Fermi-Dirac integral in (1) can be expressed as:

$$F_{1/2}(\xi) \approx \frac{2}{3}(\xi)^{\frac{3}{2}} \quad (4)$$

Eq.(1) also represents maximum drain current for a complete ballistic MOSFET. For a symmetric DG MOSFET (Fig.1(a)), the currents and the inversion charge capacitances are doubled when compared with a bulk MOSFET of similar channel length. In the proposed work, the reference structure is a Quadruple Gate (QG)

MOSFET (Fig.1.c), which consists of gate material surrounding all the four sides of the channel layer. So, conceptually the gate all around symmetric structure is equivalent to two symmetric DG MOSFETs with one DG positioned in horizontal way and the other DG structure placed vertically. Due to the aforementioned structural equivalence and physical intuition, the magnitude of the drain current for different multi-gate devices mentioned in Fig.1 can be related to the bulk MOSFET as:

$$I_{ds,QG} = 2I_{ds,DG} = 4I_{ds,bulk} \tag{5}$$

The above relations are valid for symmetric structures only. In asymmetric cases, the structural variations and irregularities must be considered, while accurately calculating the drain current. Considering the equivalence for structurally symmetric devices given in Eq.(5), the drain current for a fully ballistic QG MOSFET can be expressed as:

$$I_{ds,QG} = 4G\left[F_{1/2}(\xi) - F_{1/2}\left(\xi - \frac{V_{ds}}{v_T}\right)\right] \tag{6}$$

Eq.(6) represents the maximum current carrying capability of a hypothetically complete ballistic symmetric QG MOSFET. The fully ballistic QG MOSFET drain current in Eq.(6) is derived by ignoring the carrier scattering events. However, current state of art nanoscale devices exhibit quasi-ballistic nature [18] and this is due to unavoidable scattering effects. In the nanoscale regime, the carrier transport becomes quasi-ballistic (an appropriate combination of diffusion and ballistic current components), highly dependent on the drain bias. Hence, for accurately capturing the physics of quasi-ballistic transport, the proposed QG model in Eq.(6) needs modification, which is done by including the scattering effects in terms of transmission and reflection coefficients. The scattering equations in terms of transmission coefficient (T_C) and reflection coefficient (R_C) is given in Eq.(7) as:

$$T_C + R_C = 1 \tag{7}$$

where

$$T_C = \lambda/(\lambda+L) \text{ and } R_C = L/(\lambda+L) \tag{8}$$

In Eq.(8), λ denotes the mean free path of the carriers calculated similarly as in [8]. Eq.(7) and Eq.(8) present a straightforward relation between diffusive and ballistic transport. Based on the fundamental concepts of scattering physics [18-20], different carrier transports occurring in MOSFETs are listed in Table.1.

Table.1. Different carrier transport with conditions as per scattering theory [20]

Condition	Type of carrier transport
T_C=0 and $L \gg \lambda$	Drift-Diffusive with significant scattering
$0<T_C<1$ and $L \geq \lambda$ (low drain bias)	Quasi-Ballistic with uniform scattering throughout L
$0<T_C<1$ $L \approx \lambda$ and $\delta<\lambda$ (high drain bias)	Quasi-Ballistic with positional carrier scattering near virtual source
T_C=1 and $L<\lambda$	Ballistic with no scattering

In quasi-ballistic MOSFETS, the transmission co-efficient varies between 0 and 1. The QG device structure in the proposed work consists of a low field region near the source (depicted in Fig.2) that is firmly controlled by gate voltage V_{gs} and a high field region near the drain that is controlled by drain voltage V_{ds}. For low drain bias voltages, channel length L and the mean free path λ are sufficient to determine carrier transport. The grey shaded data in Table.1 suggests that for very low drain biases, the entire channel acts as critical channel length with uniform carrier scattering throughout the length L. However, for high drain voltages, the carrier scattering largely depends on the critical carrier scattering length δ that is positioned just near the virtual source (again highlighted in Fig.2). The parameter δ is a function of drain voltage V_{ds} and its functional dependency is given by a semi-empirical solution as in [14].

Based on the preceding explanation and considering the condition for the critical carrier scattering length near virtual source as $L \approx \lambda$ and $\delta<\lambda$, the transmission co-efficient and reflection co-efficient terms in Eq.(8) are re-written by replacing L by δ and further expressed in Eq.(9) as:

$$T_C = \lambda/(\lambda+\delta) \text{ and } R_C = \delta/(\lambda+\delta) \tag{9}$$

Using Eq.(5) and Eq.(9), the drain current equation in Eq.(6) is finally modified and expressed in Eq.(10) as:

$$I_{ds} = 4GT_C\left[F_{1/2}(\xi) - F_{1/2}\left(\xi - \frac{V_{ds}}{v_T}\right)\right] \tag{10}$$

The Eq.(10) denotes the drain current equation valid for the proposed symmetric quadruple gate (QG) MOSFET structure that includes quasi-ballistic transport in the presence of scattering and carrier degeneracy effects prevailing in nanoscale regime. In case of structural asymmetry the model equations change accordingly. Further, the proposed model ignores quantum effects for simplicity. Section.3 presents the simulation results obtained as per the proposed model.

3. RESULTS AND DISCUSSIONS

The results for the proposed quasi-ballistic QG MOSFET model are presented in this section. The nanoscale QG device in Fig.1(c) is considered as the reference structure. As stated in the previous section, the semi-ballistic carrier transport primarily depends on the mean free path λ and the critical carrier scattering channel length δ near the low field source region. So, δ determines the carrier scattering rate and magnitude of diffusive current. For obtaining the results, the following structural and physical device parameters are considered: channel height H = 10 nm , effective channel length (as per the scaling limit in [21]) L = 15 nm in nanoscale regime and L = 100 nm in larger channel length regime, silicon layer thickness t_{si}=10nm, oxide layer thickness t_{ox}=1nm, doping density of Si film N_a = 1x10^{12} cm^{-3}, bulk electron mobility μ=300cm^2/Vs. Effective mobility for electrons μ_{eff} is calculated as a function of surface potential ψ_s and gate voltage V_{gs} and the same is used to estimate the mean free path λ. Further, λ and the thermal injection velocity v_{therm} with which the electrons travel are computed as in [22].

The Fig.3 and Fig.4 provide the drain current results obtained using Natori's fully ballistic model [10] and a well known drift-diffusion model [7] for two different channel lengths. The drain current is correctly depicted by the drift-diffusion model [7] in Fig.3 when the channel length L = 100 nm. However, the same model [7] in Fig.4 erroneously over predicts the drain current when the channel length is rigorously scaled down to the magnitude of L= 15 nm. As per the physics of carrier transport in MOSFETs [12], the magnitude of ballistic current is always greater than the drift-diffusion current. This is essentially due to the presence of carrier scattering in drift-diffusion transport and absence of scattering in the fully ballistic case [20]. So, Fig.4 clearly suggests that in the nanoscale regime the traditional drift-diffusion models fail to explain the essential physics of nanoscale devices.

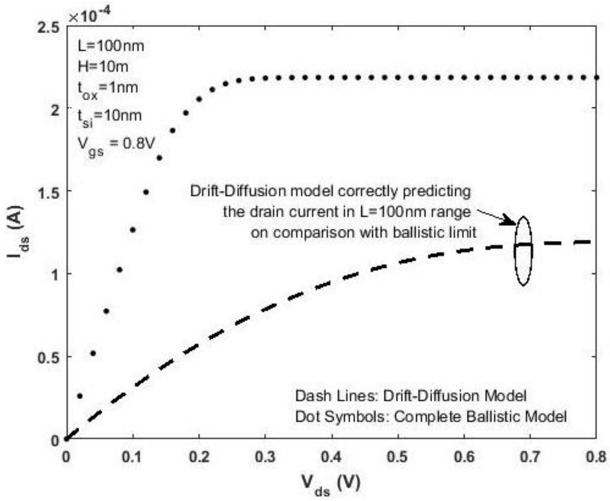


Fig.3. Drain current I_{ds} as a function of V_{ds} at V_{gs}=0.8V. It is observed that the drift-diffusion transport model [7] (Dash lines) is compared with the ballistic transport model [10] (Dot Symbols) for channel length L =100nm and the results appear to be predictive.

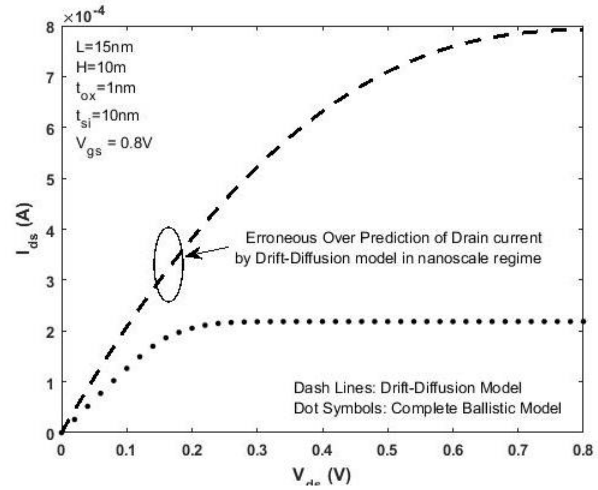


Fig.4. Drain current I_{ds} as a function of V_{ds} at V_{gs} =0.8V. Here, it is observed that the drift-diffusion transport model [7] (Dash lines) clearly over-predicts the drain current when compared with the ballistic transport model [10] (Dot Symbols) for channel length L =15nm. The erroneous current values clearly imply the failure of the model [7] in nanoscale regime.

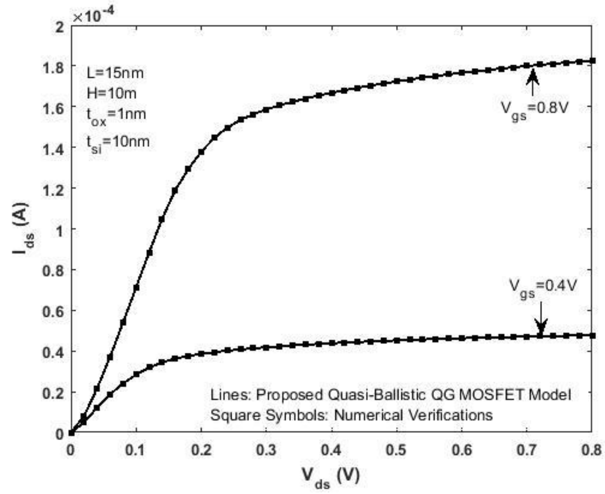


Fig.5. Drain current I_{ds} as a function of V_{ds} for the proposed quasi-ballistic QG MOSFET model. The lines represent the proposed model and the square symbols represent the numerical verifications.

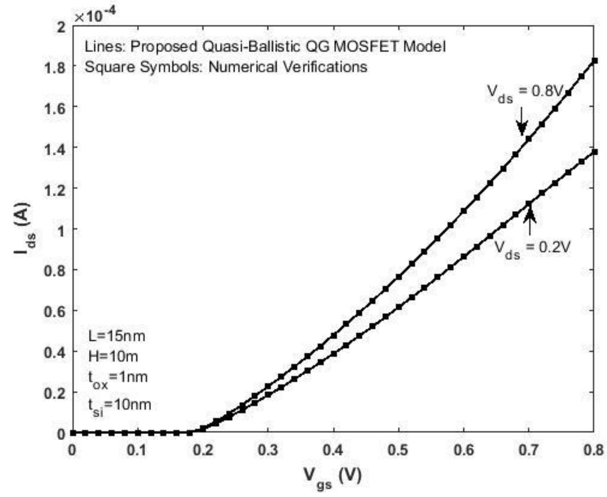


Fig.6. Drain current I_{ds} as a function of V_{gs} for the proposed quasi-ballistic QG MOSFET model. The lines represent the proposed model and the square symbols represent the numerical verifications

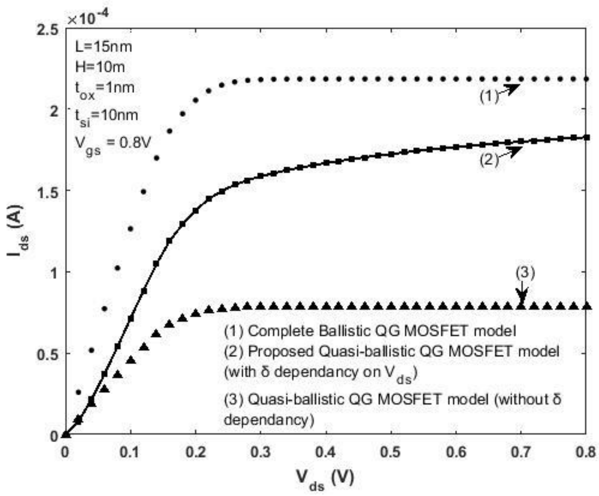


Fig.7. Comparison of the proposed quasi-ballistic QG MOSFET model with other related models for L =15nm. The proposed

drain current model effectively captures the δ dependency on the quasi-ballistic behaviour in the nanoscale channel length regime

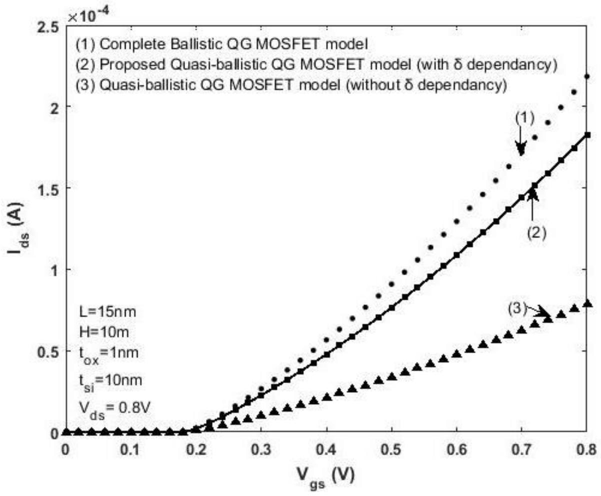


Fig.8. Drain current I_{ds} as a function of V_{gs} predicted by the proposed QG model and compared with other related models for L =15nm. The proposed drain current model clearly captures the δ dependency.

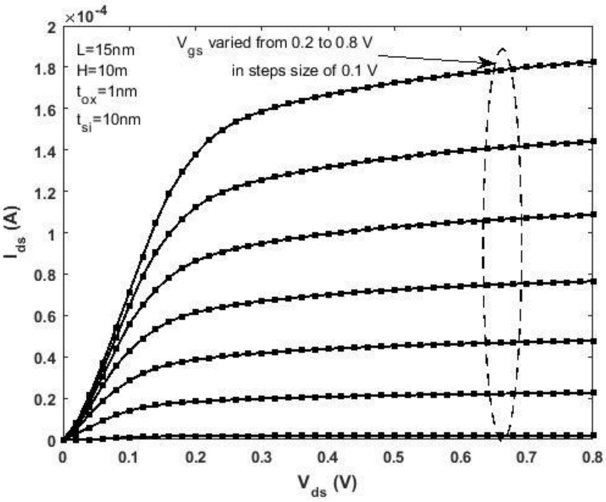


Fig.9. Drain current I_{ds} as a function of V_{ds} for different V_{gs} values. The key signature of a short channel device is effectively captured by the proposed quasi-ballistic QG model

The inaccurate results of traditional drift-diffusion models is successfully addressed and corrected in this proposed work. Fig.5 and Fig.6 present the core results of the proposed work expressed through Eq.(6)- Eq.(10). The drain currents for the proposed QG model in Fig.5 (output characteristics) and Fig.6 (transfer characteristics) effectively include the scattering physics that results in the quasi-ballistic behaviour of the device. Further, the model in Eq.(10) successfully includes the effect of drain bias dependency on the critical carrier scattering channel length δ.

The real strength of the proposed model is shown in Fig.7 and Fig.8, where it is compared with the fully ballistic model [10] and δ independent quasi-ballistic model [13]. The proposed model (Lines) results are verified with numerical simulations (square symbols). The Fig.9 demonstrates excellent continuity of the proposed model in all regions of device operation. Further, the proposed QG MOSFET model effectively captures the signature effect of nanoscale devices. On comparing the proposed QG model results with that of a DG model [14] it is clearly justified that the QG MOSFET structure provides higher current driving capability and better electrostatic integrity when compared to a DG structure. The proposed QG core model can be extended further to obtain charges and capacitances similar to [13] for model completeness.

4. CONCLUSION

The work proposes a quasi-ballistic drain current model applicable for a symmetric Quadruple Gate (QG) MOSFET in nanoscale channel length regime. The proposed model partly evolves from the well-known Natori's ballistic model, which is further modified from fully ballistic to a quasi-ballistic model by including scattering theory physics. The structural refinements valid for a QG MOSFET are also considered in the proposed model. The simulation results obtained through the proposed model demonstrate the drain current continuity in all regions of device operation. Further, the model equations and results clearly justify the advantage of a QG MOSFET over a DG device in terms of higher current driving capability and better channel electrostatic integrity. The model results are also compared with other recent transport models to highlight and present the physical accuracy and effectiveness. To summarize, the proposed quasi-ballistic QG model may serve as a potential candidate in multi-gate compact model and circuit simulation applications.

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