DOI: 10.21917/ijme.2022.0233

AN EFFICIENT NOVEL 6T SRAM CELL WITH OPTIMIZED LAYOUT AND DESIGN METRICS IN 45NM TECHNOLOGY

Rohin Gupta[1] and Sandeep Singh Gill[2]

[1]*Department of Electronics and Communication Engineering, I.K. Gujral Punjab Technical University, Kapurthala, India*

[2]*Department of Electronics and Communication Engineering, National Institute of Technical Teachers Training and Research, Chandigarh, India*

Abstract

In this paper, a novel 6T SRAM (Static Random Access Memory) cell is proposed with fast performance, high density, and low power consumption. The proposed configuration has exploited the benefits of feedback cutting transistor for the efficient and stable bit storage and transmission gate transistor for fast and power efficient structure. The proposed structure is comparatively more area efficient due to the use of more PMOS (P-Channel Metal-Oxide Semiconductor) transistors than NMOS (N-Channel Metal-Oxide Semiconductor) transistors without any performance degradation. It has been founded that the proper management of transistor blocks can play an important role in designing an efficient circuit. The presented SRAM cell consumes lesser power, is faster, and is taking relatively less read and write time as compared to standard 6T cell and previous configurations. The data bits in the cell are efficiently stored and are stable. The novel SRAM cell is 24.17% more compact than the traditional 6T SRAM structure. Simulation findings demonstrate that the suggested cell has shown significant improvement in performance characteristics such as reduction in leakage current, power consumption, and delay (range of 8.66% to 77.7%) as compared to similar latest research which includes advanced and costlier technologies like FINFETs (Fin Field-Effect Transistor). The proposed 6T structure is simulated in 45nm technology node using the cadence virtuoso tool.

Keywords:

Novel 6T Configuration, Complementary Metal-Oxide Semiconductor SRAM Cell, Low Power SRAM Cell, 45nm Technology Node, SRAM Layout

1. INTRODUCTION

In this electronic era, SRAMs are extensively used especially in battery-operated portable devices due to its inherent advantages. It consumes less area, has less leakage, and is power efficient. Static RAMs are comparatively faster than other memory storage methods as it requires less read and write time [1]. SRAMs have become a vital component in most electronic gadgets due to its storage utilization and dependency of battery life on it. The increasing size of the storage modules on components like embedded systems and microprocessors makes SRAM a critical performance issue component since its power consumption is considerable in comparison to other circuit components. Also, its extensive usage in processor-based gadgets makes it a demanding module of the processor that determines the delay of the processor. Power dissipation in VLSI chips has become an essential parameter (design metric) because of the compact integration, and extensive proliferation of portable gadgets. Increasing on-chip memory size increases the number of memory cells, which in turn increases the power absorption due to static leakage current in the idle mode of the circuit [2]. The semiconductor memory modules are designed by organizing and arranging the SRAM cells in arrays of densely packed cells for minimal leakage and power dissipation enhancing the performance by improving the peripheral circuit and optimizing the cell ratio parameters (width, length, doping profile of the transistor) [3]. For a complete circuitry, the individual circuits or modules or blocks (like SRAM cell, processor, ROM, etc.) are considered for floor planning for the efficient performance of the gadgets [4]-[6]. In a particular block, the transistors are kept in a managed way, and nowadays even in the third dimension for optimized performance [7].

Many configurations have been proposed by researchers in various articles. The most widely used conventional (or traditional) Complementary Metal-Oxide Semiconductor (CMOS) 6T SRAM circuit is quite power efficient with high resistance to voltage variation and transient noise and has less leakage than the four transistors resistive load cell structure. Hence, CMOS SRAMs are favored over resistive load cells structure for low power and high-speed applications [8]. Stable Data retention and robust performance is the key goal while designing any memory cell or circuit. Due to uniformity in the conventional 6T SRAM structure, the power consumption in writing and reading data bits '0' and 'l' remains generally the same. But with the increasing demand for portable devices, various other configurations of the SRAM cell are looked upon including the asymmetric configurations. As technology scales down, Very Large-Scale Integration (VLSI) circuits use less power supply. With the scaled technologies, these configurations are a boon to today's electronic gadgets.

The main design challenge includes the design of low power, low leakage, and high-density memory cell. Many points need to be taken care of while designing a memory cell, which includes process variation, bit cell stability (write, read and standby stability), sensing, architecture, and effective CAD techniques. Due to the enhanced use of embedded memory (in electronic gadgets) in scaled technology, the need for low power SRAM system is felt. Integrating more silicon memory on the chip is replacing traditional storage devices due to CMOS memory's low power density, layout regularity, performance, and power advantages.

There are many possibilities through which we can enhance the performance of the chip like changing of doping profile, aspect ratio, width, length, power supply, or configuration for optimal results. This paper aims at devising a new topology, which can store the bits efficiently with low leakage current and is area and power efficient. Based on the literature review, an appropriate solution methodology is utilized to achieve the objectives of the research. For better results, widths and the other parameters of the various circuit elements (in this case CMOS transistor) are analyzed through transient analysis of the circuit. After finding the most optimized solution, the results are compared with those available in the literature. The results of the proposed configuration are found to be better than the previous state-of-the-art research. The configuration is checked for

operation under a practical temperature range. In this paper, the transistor's name starting with the letter 'P' (PM0, PM1, PM2, and PM3) are PMOS transistors and the transistor name starting with the letter 'N' (NM0, NM1, NM2, and NM3) are NMOS transistors.

2. STANDARD 6T CONFIGURATION

The conventional (or traditional) 6T SRAM cell is considered to be the standard SRAM cell. Static RAM is a type of RAM that stores data without needing to be refreshed as long as the circuit is powered. As depicted in Fig.1, a traditional 6T memory cell constitutes two cross-coupled CMOS inverters linked back-to-back, along with two pass transistors linked to complementary bit lines BL and BLB. The WL (word line) is connected to the access transistor gates 'NM2 and NM3', which are used to have data transferred to or read from the memory cell through the BLB and BL (bit lines) during read and write operations. Bit lines serve as Input/ Output (I/O) buses, transporting data from the write circuitry to the SRAM module and from the memory module to the sense amplifier. The output of SRAM configuration is generally available at Bit_Line (BL) and Bit_Line_Bar (BLB) lines. A sense amplifier transforms a differential signal or signal from the mid value to either '0' or '1' (logic-level output). Amidst the idle operation, the bit lines are returned to the power supply 'V_{DD}' (positive supply rail). WL (Word Line) is linked to supply 'V_{DD}' during the write operation, and the BLs are driven to either V_{DD} or V_{SS} according to the data to be written, that is either at logic '1' or logic '0', which overpowers the memory cell data bits.

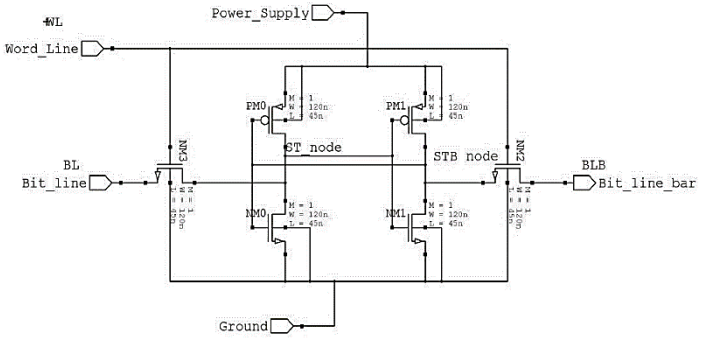


Fig.1. The standard 6T SRAM cell.

Word Line (WL) is linked to GND and the Bit Lines are left floating or linked to supply 'V_{DD}' during the hold operation. Three roots of intersection, showing bistability, are sought during read or hold. Only one root of intersection is sought during write, such that the cell will deterministically flip between the two data states determined by the BL polarity. Although two-bit lines are not required, a dual-ended SRAM cell enhances bit stability and reliable operations on it. Three different functions hold, read and write operations are executed by the SRAM circuitry [9]. The SRAM cell current and the read static noise margin (SNM) are two critical characteristics of the cell structure. The read static noise margin (SNM) of the cell indicates the cell's robustness amid the read cycle and the SRAM cell current influences the SRAM cell's time delay. Less SRAM cell current lengthens the bit-line (BL) latency, and read SNM deterioration causes data loss during read operations [10]. The current levels of Read SNM and SRAM cells are significantly reliant on the access NMOS transistors' driving capabilities. Segregation of the data output and data retention elements is used to solve the SRAM cell current and read SNM inverse correlation problem [11]. This can remove the ambiguity of cell delay and read SNM degradation problem.

3. NOVEL INNOVATIVE 6T SRAM CELL STRUCTURE

The presented novel structure of 6T SRAM circuitry is depicted in Fig.2. The structure consists of transmission gate transistor rather than access transistor, an NMOS transistor removed from the standard CMOS inverter circuit and adding feedback cutting PMOS transistor. The transmission gate transistor helped in fast performance with comparatively less leakage of current and power. The novel configuration exploits the benefits of feedback cutting transistor and transmission gate transistor. At nodes ST and STB, stored bits are obtainable. The presented configuration is a single-ended SRAM cell. The transmission gate with governing signals WLB and WL (Word lines), reads and writes data from and to BL (Bit line). The feedback cutting transistor (PM2) is ON and the transmission gate is OFF while the cell is in idle mode (no read or write operations). If data '1' is present in the memory cell structure, the transistors NM0 and PM3 are turned on, and consequently, the STB node is brought down to GND, resulting in positive feedback between the STB node and the ST node. When '0' is available in the cell structure, transistor PM1 is ON, it will force the STB node to V_{DD}. Bit '0' is maintained at the ST node by the current leakage from the ST node to the BL through the transmission gate transistor, since the BL (bit line) is linked to the ground during the idle condition. In the presented configuration, the supply voltage 'V_{DD}' is set to 1V and the ground voltage 'GND' is set to 0V during the simulation process with 45nm technology.

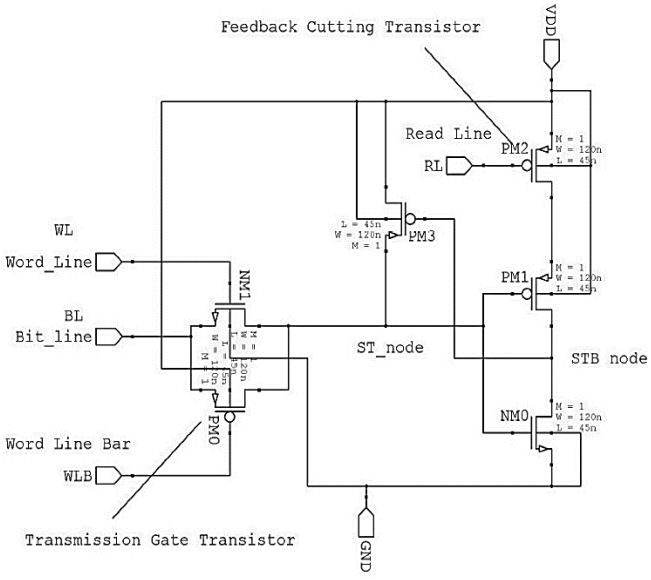


Fig.2. Proposed novel 6T SRAM cell circuit in 45 nm Technology

The comprehensive description of the presented 6T SRAM circuit when data '0' is written to the cell is depicted in Fig.3. The data bit '1' is stored by the forcing element from the power supply. Data '0' is maintained in the cell due to leakage factor

from ST node to Bit Line, since in the idle condition, BL is connected to ground or discharged to ground. In this cell feedback cutting transistor, PM2 is used to disconnect the power supply during the read operation. This process improves the SNM of the SRAM cell [3]. To maintain data '0' at the node, the leakage current from the ST node should be higher in comparison to other leakage current from other transistors to the ST node. If leakage is not from ST node to ground, data '0' cannot be retained. Therefore from Fig.3, I_1 should be greater than all other leakage currents and its direction should be from ST node to ground through the transmission gate, that is:

$$I_1 > I_2 + I_3 \quad (1)$$

Due to the low threshold voltage (V_t), the sub threshold leakage has become a dominant factor. Subthreshold current is the drain-source leakage current when the transistor is operating in the weak inversion zone [12] [13]. It can be calculated by Eq.(2):

$$I_{sub} = \frac{W}{L}.\mu.{V_{th}}^2.C_{sth}.e^{\frac{V_{gs}-V_t+\eta V_{ds}}{nV_{th}}}\left(1-e^{-\frac{V_{ds}}{V_{th}}}\right) \quad (2)$$

where,

W - Width of transistor

L - Length of the transistor

μ - Carrier mobility

V_{th} - Thermal voltage at temperature T. Also,

$$V_{th} = kT/q$$

C_{sth} - summation of depletion region capacitance per unit area (C_{dep}) and interface trap capacitance per unit area (C_{it}) at the CMOS gate.

$$C_{sth} = C_{dep} + C_{it}.$$

η - DIBL coefficient

V_{gs} - Gate source voltage

V_{ds} - Drain Source voltage

V_t is the threshold voltage and is defined as the addition of Flat Band Voltage (V_{FB}), twice bulk potential (φ_F), and the voltage across gate oxide due to depletion layer [12] [13] as expressed by Eq.(3).

$$V_t = V_{FB} + 2\varphi_F + \frac{\sqrt{2\varepsilon_q N_a\left(2\varphi_F + V_{SB}\right)}}{c_{ox}} \quad (3)$$

Where bulk potential value (φ_F) depends on the doping level of the CMOS transistor. For NMOS or p-substrate, φ_F is given by Eq.(4).

$$\varphi_F = V_t \ln(N_a/n_i) \quad (4)$$

For PMOS or n-substrate, φ_F is given by Eq.(5).

$$\varphi_F = V_t \ln(N_d/n_i) \quad (5)$$

The static power dissipation is defined as the power that is wasted when either bit '1' or bit '0' is stored in the SRAM cell [13]. The static power dissipation, P_{static} can be expressed by Eq.(6).

$$P_{static} = I_{leak} * V_{dd} \quad (6)$$

where,

I_{leak} - Leakage current during stored bits, and

V_{dd} - Supply voltage.

The dynamic power dissipation of the SRAM cell is described as the power that is dissipated during the switching of bits from '0' to '1' or '1' to '0' [13]. The dynamic power dissipation, $P_{dynamic}$ can be calculated by Eq.(7).

$$P_{dynamic} = \alpha \cdot C \cdot V_{dd} \cdot V_{swing} \cdot f \quad (7)$$

where,

α - Activity factor

C - Load capacitance

V_{dd} - Supply Voltage

V_{swing} - Voltage swing during transition of bits

f - Clock frequency

The total energy 'E' dissipated in time 't' during the process can be calculated by Eq.(8).

$$E = Power * t \quad (8)$$

where *Power* can static or dynamic.

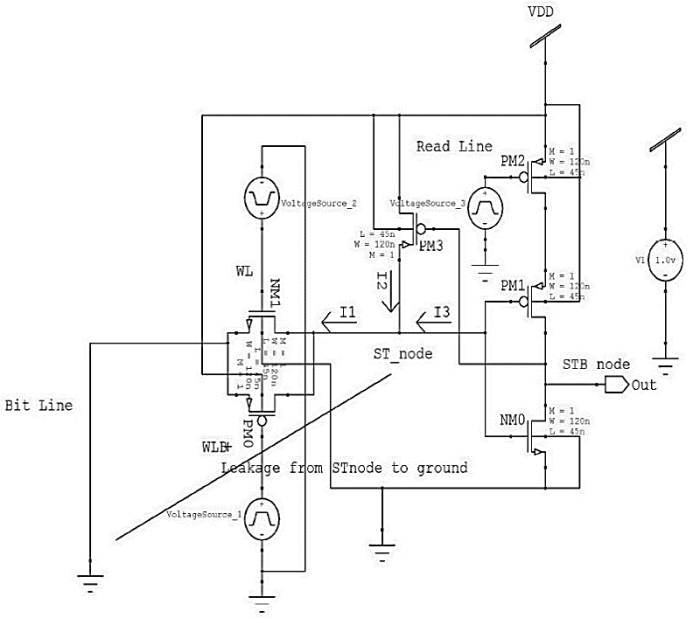


Fig.3. 6T SRAM structure in 45 nm Technology

3.1 READ AND WRITE OPERATION

When the SRAM memory cell is in the read operation, the cell has to go via many stages for reliable operation. The first step includes the bit-line discharging. In bit-line discharging, the bit line is first discharged to the ground for any unwanted effect of charge and then kept floated. During this step, Read Line is kept high (V_{DD}) means the feedback cutting transistor is kept in OFF condition. The next step is Word Line Activation in which WLB is linked to GND and WL is connected to V_{DD}. During this step, there can be two possibilities in which either bit '1' is saved in the cell (ST node is high and STB node is low) or bit '0' is stored in the cell (ST node is low and STB node is high). If bit '1' is stored, the voltage of the bit-line becomes high which is diagnosed by the sense amplifier and is read as bit '1'. If bit '0' is present in the cell the voltage of the bit-line and ST node is equalized through the transmission gate transistor that is detected by the sense amplifier and is read as bit '0'. The Fig.4 shows a probable circuit schematic of the sense amplifier in the 45nm technology node that is utilized to read data bits from the proposed novel cell [14]. The bit line

signal is amplified by the sense amplifier that is available at the bit (D0) and bitbar output (DB0). Even a tiny deviation in the input from the center value of 0.5V can be amplified by this amplifier. After the read operation is over, the cell will go to the idle mode and the bit-lines are again linked to GND.

Fig.5(a) depicts the simulation results of the read signal of the presented SRAM circuitry. ST and STB nodes hold the bits that are stored. WL and WLB signal ports are the regulating ports of the transmission gate transistor. The data from the Bit Line is transmitted to the sense amplifier. Port 'D_0' holds the signal to be read, whereas DB0 contains its inverted part. After the read operation is over, the cell goes into the idle mode in which the transmission gate transistor goes in the inactive mode (switched OFF) while the precharge circuitry in the active mode (switched ON).

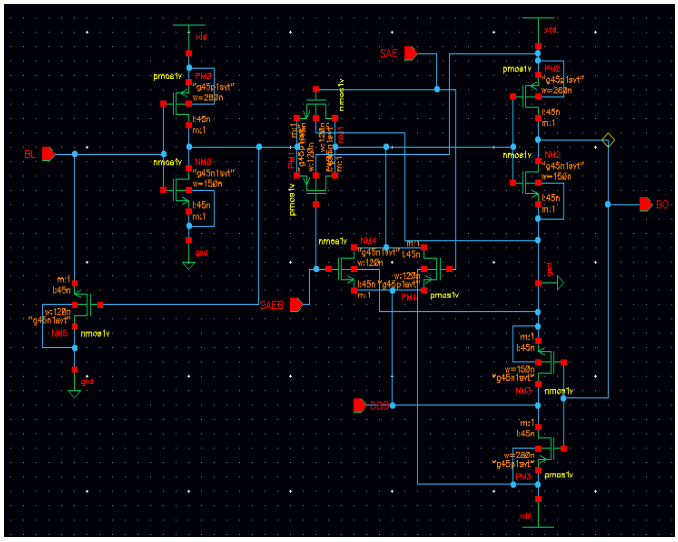
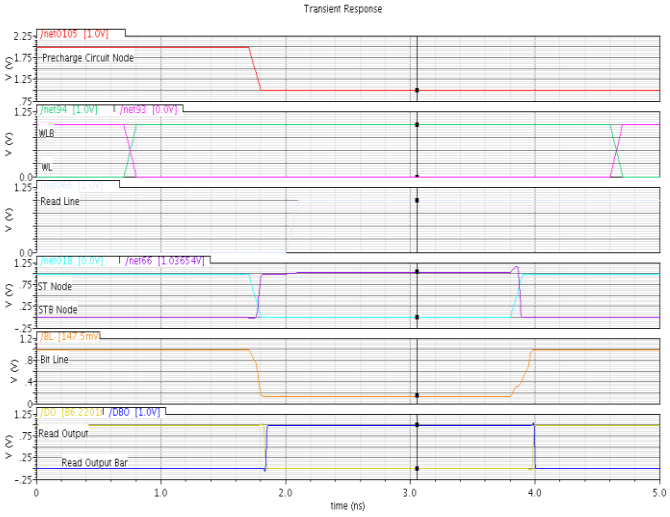
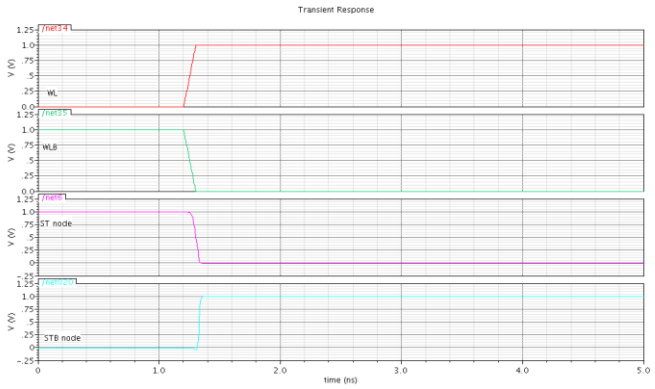


Fig.4. Sense amplifier schematic of the proposed cell

The transient response of writing bit '0' is shown in Fig.5(b). Similar to the read operation, the write operation is performed by following some steps. Amid the write operation, the transmission gate transistor is turned ON and the RL line is forced to ground. The next step involves Bit-line driving. In this step, the data to be written is linked to BL (Bit-Line). WL (Word-Line) is connected to $V_{DD,}$ and WLB (Word-Line-Bar) is connected to ground 'GND'. The next step includes the cell flipping step. In this step, there can be two conditions in which either data '0' or data '1' is to be written. In the case of data '0', the ST node is forced down to GND through the transmission gate transistor, and consequently the load transistor 'PM1' gets turned ON resulting in pulling up of the STB node to V_{DD}. Similarly, if bit '1' is to be written, the ST node is pulled up to V_{DD}-V_{tn} (V_{tn}: Threshold voltage for NMOS transistor) by the transmission transistor. As a result, the NM0 (NMOS) driving transistor gets turned ON, and the STB node is pushed down to ground 'GND' resulting in the generation of positive feedback. After the write operation is over, the cell goes to the idle mode where bit-line, WL, and WLB lines are linked to GND and V_{DD} respectively.



(a)



(b)

Fig.5. Simulated results of the (a) read and (b) write ('0') operation of the presented novel SRAM cell.

4. RESULTS AND DISCUSSION

4.1 LEAKAGE CURRENT

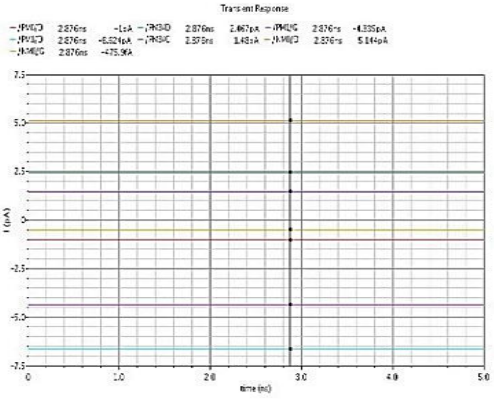
The novel 6T SRAM cell retains the data '0' utilizing the leakage current from the ST node to the bit line through the transmission gate transistor as depicted in Fig.3. The leakage is allowed through the transmission gate transistor as the bit line is connected to ground 'GND' in the idle mode. In the other state (when data '1' is stored), the 6T SRAM cell retains its data through feedback. Hence the novel innovative structure utilizes the leakage current too in stabilizing the stored bits. Simulation results show that the leakages (current) in the novel structure are significantly less than the previously published SRAM structures. The Table.1 compares the leakage current of the proposed novel 6T cell with conventional 6T and previously mentioned 5T cells. Comparison results depict that the presented circuit has shown the finest results yet for write '1' at ST node with 77.7% reduction and write '0' at STB node with 8.66% reduction in leakage current. For write '0' at ST node, it is near to best result while for write '1' at STB node has shown degraded result. The results are found to be even better when compared to costlier FinFET technology. The simulated leakage current during write operation at various nodes is shown in Fig.6. In the presented cell structure,

various leakage currents have been calculated by probing the current leakages at the nodes (ST and STB nodes).

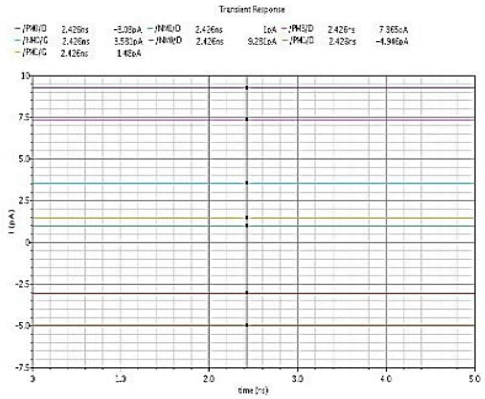
Table.1. Comparison of the leakage current at ST and STB nodes of the proposed cell with the previous results.

Parameters/ References	Write '0' at ST node	Write '1' at ST node	Write '0' at STB node	Write '1' at STB node
5T cell (2011) [3]	3.60 nA	18.9 nA	5.51 nA	-9.824 nA
Conventional 6T cell [3]	9.20 nA	-32.10 nA	94.11 nA	-0.229 nA
5T cell (2014) [14]	5.14 pA	6.61 pA	-5.415 pA	-475.88 fA
6T FinFET at 27° C [15]*	235pA			
Proposed 6T cell	-5.41 pA	1.47 pA	-4.946 pA	6.623 pA

*indicates minimum leakage in the particular configuration literature



(a)



(b)

Fig.6. Various node leakages during (a) write '0' operation and (b) write '1' operation.

4.2 DELAY

The propagation delay of the SRAM cell is defined as the time expenditure from the input port (Bit Line) to the output port (ST and STB node where ST node is preferred for delay calculation). It can also be defined as the input (BL) to output (ST node) signal delay during the low to high (τ_{PLH}) or high to low (τ_{PHL}) transition of the input and output signal. During the calculation of the delay, the signal is considered to be an optimal signal with zero fall and rise time (though in reality, zero fall and rise time is not feasible). In the proposed configuration, the ST node holds the stored data and its inverted bit is available at the sense amplifier during the read operation, hence ST node is given preference. Though table 2 mentions delay at both ST and STB nodes for the proposed configuration.

The Table.2 compares cell delay with recent state of art research results reported in different works of literature that include 5T SRAM cell (2011) [3] in 45nm, Conventional 6T SRAM cell in 45nm [3], 7T1, 7T2, 7T3 [16] in 45nm, 5T SRAM cell (2014) in 45nm [14], minimum delay in NC and PP configuration in 45nm [17]**,** minimum delay in Gated VDD in 90nm [18]**,** minimum delay in Fin Field-Effect Transistor (FinFET) 6T in 22nm[19], minimum delay in 11T SRAM configuration in 40nm technology [20], 6T FinFET in 22nm [21], 6T FinFET in 18nm [22], 7T CMOS in 28nm [23], 8T TG-DTMOS in 45nm [24], 6T SG mode in 45nm [25] and 10T FinFET in 45nm and 32nm tech [26] . For comparison, similar parameters are taken into consideration with minimum delay. The comparison is made for 45nm, 90nm, 40nm, and 22nm technology node in CMOS and FINFET technologies. The table depicts that the proposed 6T SRAM cell's delay (45nm) is the minimum of all. If compared with the previous best at the ST node [14], it shows an 11.11% reduced delay, and at the STB node 19.4% reduction in delay. The important point to be noted is that the proposed configuration is better in performance even when compared with advanced and costlier FINFET technology with a 77.4% reduction in delay. In summary, the proposed 6T cell is outperforming other configurations with significant improvement in speed or reduced delay.

Table.2. Comparison of the delay of the proposed cell with the previous cells

Parameters	Delay at ST node	Delay at STB node
5T cell (45nm) (2011)	2.453 ns	14.24 ps
Conventional 6T cell (45nm)	0.839 ns	47.72 ps
7T1 cell (45nm)	39.18ps	39.18ps
7T2 cell (45nm)	28.96ps	34.53ps
7T3 cell (45nm)	31.48ps	31.48ps
5T SRAM cell (2014) (45nm)	5.13 ps	17.66 ps
NC (45nm)*	459.6ps	
PP (45nm)*	430.3ps	
Gated VDD (90nm)*	14.35ps	
MTCMOS (90nm)*	13.5ps	
FinFET 6T (22nm)*	98ps	
11T (40 nm)*	48ps	
FinFET 6T (22nm)*	20.2ps	
6T FinFET (18nm)*	400ps	
7T CMOS (28nm)*	90ps	
8T TG-DTMOS (45nm)*	385ps	
6T SG mode (45nm)*	33.28ps	

10T FinFET (45nm)*	50ps	
10T FinFET (32nm)*	80ps	
Proposed 6T CMOS SRAM cell (45nm)	4.56 ps	14.23 ps

* indicates minimum delay in the particular configuration

4.3 POWER CONSUMPTION

The power used by the active transistor (in operation) or switched-on transistor determines the power consumption of the SRAM memory cell [13]. When stored bits are changed (or flipped), the power consumption is known as dynamic power consumption. Power consumption during stable bits (no change) is known as static power dissipation. In SRAM cell, power consumption is mainly due to the sub threshold leakage current since the technology used is the scaled one [27]. The current and voltages are calculated across the transistors that are in ON condition during the write functionality (writing data '1' or '0') and are measured to determine power usage during the process. Table 3 depicts the contrast of the recent state of art research results including 5T SRAM cell (2011) [3], conventional 6T SRAM cell [3], 7T1, 7T2, 7T3 SRAM cell [16], 5T SRAM cell (2014) [14], minimum power consumption in NC and PP (45nm) [17], minimum power consumption in FINFET 6T SRAM cell in 22nm [19], minimum power consumption in 8T SRAM cell in 65nm technology node [28], 7T FINFET SRAM cell in 18nm [29], 7T CMOS in 28nm [23], 10T FinFET in 45nm and 32nm tech [26]. In the table, the term 'nW' is Nano Watt and 'pW' is Pico Watt. The comparison has been made with the research with similar parameters or near to similar parameters. It is quite clear from the comparison that the proposed configuration is generating robust results with less power consumption even when compared with advanced and costlier FINFET technologies. The proposed configuration compared with other configurations show an 8.7% reduction in power consumption for write '0' at STB node and near to best results for write '1' at STB node and comparatively worse result for write '0' and write '1' at ST node. Results comparison with other research than [3] and [14] shows significant improvement even when compared to the latest FinFET technologies with stable bit storage.

Table.3. Power consumption comparison of the proposed cell with the previous cells

Parameters	Write '1' at ST node	Write '0' at ST node	Write '1' at STB node	Write '0' at STB node
5T cell (45nm)	9.8nW	85.01nW	67.3nW	9.8nW
6T cell (45nm)	0.011pW	0.003pW	30 pW	28 pW
7T1 cell (45nm)	59.4nW	52.5nW	56nW	58.8nW
7T2 cell (45nm)	78.5nW	81.2nW	71.2nW	74.3nW
7T3 cell (45nm)	98.9nW	93.9nW	90.4nW	95.6nW
5T cell (45nm)	6.62pW	0.465pW	5.14 pW	5.422pW
NC (45nm)*	16.3nW			
PP (45nm)*	36.83nW			
FINFET 6T (22nm)*	1.6nW			
8T SRAM cell (65nm)*	43nW			
7T SRAM cell FINFET (18nm) SVL Tech*	5.6nW			
7T CMOS (28nm)*	210pW			
10T FinFET (45nm)*	582.5pW			
10T FinFET (32nm)*	685.4pW			
Proposed 6T CMOS cell	1.47pW	5.423pW	6.624pW	4.95pW

*indicates minimum power consumption in the particular configuration

4.4 COMPLETE SRAM CIRCUITRY

The Fig.4 depicts a potential sense amplifier circuit for the proposed SRAM [3]. Even a slight signal variation from the center voltage (0.5V) can be amplified using this amplifier. The probable schematic of the sense amplifier depicted in Fig.4 when tested and simulated as transient and DC response, it has been found that the sense amplifier is switching and amplifying even a minute variation of the signal from the center value and is close to the ideal switch attributes.

The Fig.7 depicts the memory cell's circuitry, which includes the proposed innovative 6T SRAM cell, sense amplifier, and precharge circuitry. The bits are written to the cell when the transmission gate transistor is turned on, transferring the bits from the bit lines to the SRAM cell nodes. When the Sense Amplifier Enable port is enabled, the stored data bit is read from the cell. Outputs are accessible at ports D0 and DB0. The simulation results for the read function and write '0' is shown in Fig.5.

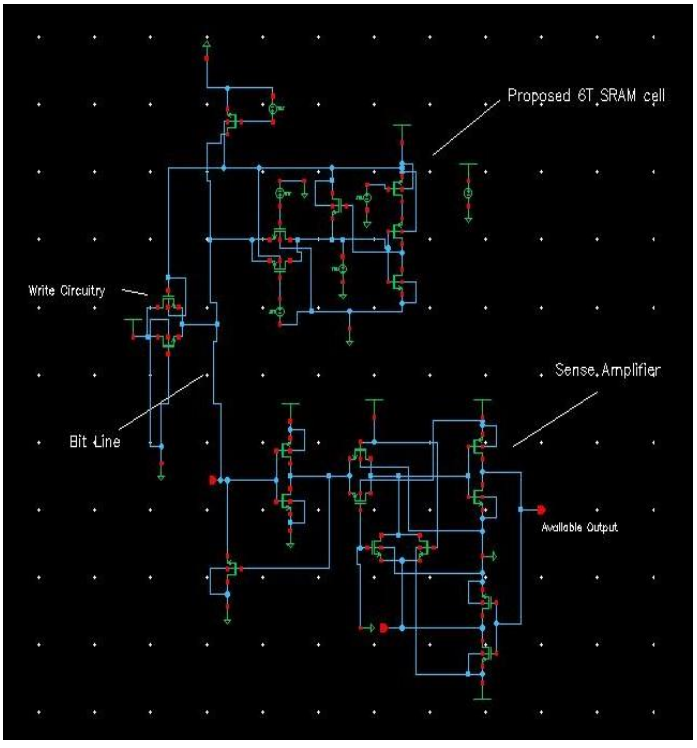


Fig.7. Complete circuitry includes the proposed 6T SRAM cell, sense amplifier, and precharge circuitry

4.5 LAYOUT

The designed layout of the proposed 6T SRAM cell in the 45nm technology node is depicted in Fig.8. The mentioned widths

in the schematic (Fig.2) have been utilized in designing the layout. Table 4 shows the contrast of the proposed configuration with different literature results all in 45nm technology which includes conventional 6T configuration [3], 5T SRAM cell (2011) [3], 7T SRAM cell [16]**,** 5T SRAM cell (2014) [14]. The comparison is made with the research in which a single cell layout is present. The conventional 6T SRAM cell is as compact as possible with an area of 3.438 μm^2 [3], whereas the proposed 6T SRAM cell demands only 2.60 μm^2 area. The calculated area excludes the area pruned by area sharing with the adjoining cells. With neighboring cells area sharing, the area can be reduced significantly. Using the same design criteria, the novel cell size is 24.17% smaller than the traditional 6T SRAM cell. This is because of the use of 4 PMOS transistors. The layout of the previous 5T cell (2014) is demanding an area of 2.60 μm^2 [14] which is similar to the proposed 6T cell. It is clear from table 4 that a reduced area can be achieved for the same or even a smaller number of transistors (5T SRAM cell (2011)) with proper placement and management of transistors on the floorplan (layout of the cell).

Table.4. Area comparison of the previous configurations with the proposed cell

Configuration	**Area occupied for a single cell in um^2**
6T Conventional	3.438
5T SRAM (2011)	2.69
7T SRAM cell	4.41
5T SRAM (2014)	2.60
Proposed 6T SRAM cell	2.60

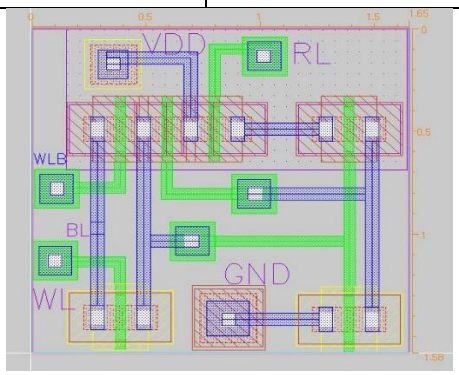


Fig.8. The layout of the proposed 6T SRAM structure in the 45nm technology node

5. CONCLUSIONS

An innovative 6T SRAM configuration is presented. It has been found that using a transmission gate rather than an access transistor increases the performance to a great extent, though an extra transistor is required. The PMOS feedback transistor helps in stable bit storage. Leakage current is calculated at the nodes where the corresponding transistors are OFF. Results have shown that the presented configuration has shown a significant reduction in leakage current and power consumption of the cell. In terms of area, the presented configuration is 24.17% smaller than the traditional 6T SRAM cell. Even when compared with lesser transistor configuration (5T SRAM configurations), the area achieved by the proposed cell is the same or less. The proposed cell is showing better results when compared with even advanced and costlier technologies like FINFETs (range of 8.66% to 77.7%). The proposed configuration uses fewer transistors (less area), is fast, has less leakage with reduced power consumption, and is also comparatively more cost-efficient than advanced technology like FinFET with stable bit storage without any performance degradation. It can be concluded from the results that the proper management and choice of transistors can lead to an efficient structure with better performance in terms of design metrics like area, current leakage, and power consumption.

The proposed configuration can be further improved by using other circuit techniques. Changes in the aspect ratio of the cell can be explored for better results. The application of the clock to the power supply and read circuit can also be explored further for reduced leakage and power consumption. The stacked transistor technique can be used for power efficient circuits. The peripheral circuitry can also be improved for better performance.

ACKNOWLEDGEMENT

The authors are thankful to Guru Nanak Dev Engineering College, Ludhiana for Cadence Virtuoso tool support. The authors would also like to extend gratitude to Dean RIC, I.K. Gujral Punjab Technical University, Kapurthala for support in the completion of this research work.

REFERENCES

[1] K. Khare, N. Khare, V. Kumar Kulhade and P. Deshpande, "VLSI Design and Analysis of Low Power 6T SRAM Cell using Cadence Tool", *Proceedings IEEE International Conference on Semiconductor Electronics*, pp. 117-121, 2008.

[2] B.C. Paul, A. Agarwal and K. Roy, "Low-Power Design Techniques for Scaled Technologies", *Integration*, Vol. 39, No. 2, pp. 64-89, 2006.

[3] S. Akashe, S. Bhushan and S. Sharma, "High Density and Low Leakage Current based 5T SRAM Cell using 45 nm Technology", *Proceedings International Conference on Nanoscience, Engineering and Technology*, pp. 346-350, 2011.

[4] P.N. Guo, C.K. Cheng and T. Yoshimura, "An O-Tree Representation of Non-Slicing Floorplan and its Applications", *Proceedings of International Conference on Design Automation*, pp. 268-273, 1999.

[5] Y.C. Chang, Y.W. Chang, G.M. Wu and S.W. Wu, "B*-Trees: A New Representation for Non-Slicing Floorplans", *Proceedings of International Conference on Design Automation*, pp. 458-463, 2000.

[6] R. Gupta and S.S. Gill, "Adaptive Memetic Algorithm on Novel CBLSP Algorithm for O-Tree Implementation", *Proceedings of International Conference on Advances in VLSI and Embedded Systems*, pp. 1-13, 2021.

[7] R.K. Nain and M. Chrzanowska Jeske, "Fast Placement-Aware 3-D Floor Planning using Vertical Constraints on Sequence Pairs", *IEEE Transactions on Very Large Scale*

Integration (VLSI) Systems, Vol. 19, No. 9, pp. 1667-1680, 2011.

[8] V.S. Babu, "*Solid State Device and Technology*", Pearson Publication, 2008.

[9] N. Rahman and B.P. Singh, "Design of Low Power SRAM Memory using 8T SRAM Cell", *International Journal on Recent Technology and Engineering*, Vol. 2, No. 1, pp. 123-127, 2013.

[10] L. Villa, M. Zhang and K. Asanovic, "Dynamic Zero Compression for Cache Energy Reduction", *Proceedings on Annual IEEE/ACM International Symposium on Microarchitecture*, pp. 214-220, 2000.

[11] L. Chang, "Stable SRAM Cell Design for the 32 nm Node and Beyond", *Proceedings of Symposium on Digest of Technical Papers on VLSI Technology*, pp. 128-129, 2005.

[12] S. Mishra, A. Dubey, S.S. Tomar and S. Akashe, "Design and Simulation of High Level Low Power 7T SRAM Cell using Various Process and Circuit Techniques", *Proceedings of IEEE International Conference on Signal Processing, Computing and Control*, pp. 1-7, 2012.

[13] N.H.E. Weste, D. Harris and A. Banerjee, "*CMOS VLSI Design*", Pearson Education, 2005.

[14] R. Gupta, S.S. Gill and N. Kaur, "A Novel Low Leakage and High Density 5T CMOS SRAM Cell in 45nm Technology", *Proceedings of International Conference on Recent Advances in Engineering and Computational Sciences*, pp. 1-6, 2014.

[15] A.A. Kumar and A. Chalil, "Performance Analysis of 6T SRAM Cell on Planar and FinFET Technology", *Proceedings of International Conference on Communication and Signal Processing*, pp. 375-379, 2019.

[16] S. Akashe, S. Rastogi and S. Sharma, "Specific Power Illustration of Proposed 7T SRAM with 6T SRAM using 45 nm Technology", *Proceedings of International Conference on Nanoscience, Engineering and Technology*, pp. 364-369, 2011.

[17] V.K. Joshi and S. Borkar, "A Comparative Study of NC and PP-SRAM Cells with 6T SRAM Cell using 45nm CMOS Technology", *Proceedings of International Conference on Advances in Electrical, Electronic and Systems Engineering*, pp. 58-62, 2016.

[18] A. Bhaskar, "Design and Analysis of Low Power SRAM Cells", *Proceedings of International Conference on Innovations in Power and Advanced Computing Technologies*, pp. 1-5, 2017.

[19] S. S. R.B. R. S., Samiksha, R. Banu and P. Shubham, "Design and Performance Analysis of 6T SRAM Cell in 22nm CMOS and FINFET Technology Nodes", *Proceedings of International Conference on Recent Advances in Electronics and Communication Technology*, pp. 38-42, 2017.

[20] J.K. Mishra, H. Srivastava, P.K. Misra and M. Goswami, "A 40nm Low Power High Stable SRAM Cell Using Separate Read Port and Sleep Transistor Methodology", *Proceedings of IEEE International Symposium on Smart Electronic Systems*, pp. 1-5, 2018.

[21] Y. Sharma, A. Singh and A. Pandey, "Comparative Design and Analysis of FinFET and CMOS SRAM Cell," in *Proceedings 2019 International Conference on Signal Processing and Communication (ICSC)*, pp. 275-278, 2019.

[22] R.R. Vallabhuni, P. Shruthi, G. Kavya and S. Siri Chandana, "6Transistor SRAM Cell Designed using 18nm FinFET Technology", *Proceedings of International Conference on Intelligent Sustainable Systems*, pp. 1584-1589, 2020.

[23] J. K. Mishra, P. Kumar Misra and M. Goswami, "A Low Power 7T SRAM cell using Supply Feedback Technique at 28nm CMOS Technology", *Proceedings of International Conference on Signal Processing and Integrated Networks*, pp. 597-602, 2020.

[24] A. Chunn, A. Agrawal and A. Naugarhiya, "An 8T TG-DTMOS Based Subthreshold SRAM Cell with Improved Write Ability and Access Times", *Proceedings of International Symposium on VLSI Design and Test*, pp. 1-6, 2020.

[25] G. Ravikishore. and N.M. Nandhitha, "6T-SRAM Design to Optimize Delay using Finfet Technology", *Proceedings International Conference on Intelligent Communication Technologies and Virtual Mobile Networks*, pp. 540-544, 2021.

[26] D. Sharma and S. Birla, "Design and Analysis of 10T SRAM Cell with Stability Characterizations", *Proceedings of International Conference on Advances in Electrical, Computing, Communication and Sustainable Technologies*, pp. 1-5, 2021.

[27] J.T. Kao and A.P. Chandrakasan, "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits", *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 7, pp. 1009-1018, 2000.

[28] B.N.K. Reddy, K. Sarangam, T. Veeraiah and R. Cheruku, "SRAM Cell with Better Read and Write Stability with Minimum Area", *Proceedings IEEE Region 10 Conference*, pp. 2164-2167, 2019.

[29] T.S. Kumar, S.L. Tripathi and S.K. Sinha, "Comparative Analysis of Leakage Power in 18nm 7T and 8T SRAM cell Implemented with SVL Technique", *Proceedings of International Conference on Intelligent Engineering and Management*, pp. 121-124, 2020.