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DESIGN OF NOISE TOLERANCE 9T SRAM CELL

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Abstract

This paper describes the well-thought-out design of a 9T Static Random Access Memory single Bit cell with enhanced performance. Monte-Carlo simulations are utilized for this proposed 9T SRAM circuit, and the outcomes are verified by comparing with various like Conv6T, Conv7T and Conv8T SRAM cells in the 22-nm PTM with variable supply voltage. The proposed 9T SRAM shows 1.02/1.265/ 0.259 × lesser read delay and 1.028/1.032/0.857 × write delay as compared to Conv6T/Conv7T/ Conv8T respectively. Our proposed 9T SRAM showing 2.06/12.5 × less leakage power dissipation as compared to Conv6T/ Conv8T respectively.

Keywords:

Read Access Time, Write Access Time, Read SNM, Read Power, Write Power, Hold Power

1. INTRODUCTION

In today rapidly evolving technology, the design of micron circuits is primarily reliant on power, and the process of designing relatively low power circuits has become a costly endeavor. Furthermore, in the design of circuits in sub 180nm technology, leakage power must be considered, resulting in the design of system on chips with significantly improved performance. As a result, our primary goal is to create an SRAM cell with a high noise margin and a low power consumption. And, in the memory design, SRAM is the key component. SRAM can be implemented using 6,7, or 8 transistors depending on the requirements. In this study, we develop an SRAM with 9 transistors, one of which is a transmission gate.

Historically, static ram (SRAM) has dominated the total power of microprocessors. As a result, lowering the voltage supply (VDD) for static ram is one of the most requested strategies for reducing power consumption and prolonging battery life. This has also been highlighted that creating a high-density Static RAM with a low Power supply is extremely difficult for a variety of reasons. The 6T SRAM cell consists of two CMOS inverters with cross coupled to each other, that is the input of one inverter is connected to output of other inverter and two extra transistors are used between world-line and bit-line as shown in the Fig.1. As shown in Fig.1 the conventional 6T SRAM has on WWL line connecting the two transistors at their gate terminal and BL and BLB to the drain terminal of two separate transistors, and two cross coupled inverters with one terminal to VDD (Power supply) and other terminal to ground. This circuit is on when WWL (Write Word Line) is kept to logic one and off when WWL kept to logic zero. Here MP1, MP2, MN1 and MN2 work as cross coupled and MN3 and MN4 are connected to WWL [1]-[5].

The conventional way of designing 6T SRAM has many design techniques, out of the some may have better results compared to other techniques. Some use power gating techniques some use decoupled circuits and some use other based on their intensions. But all the techniques in 6T SRAM use 6 transistors in their design. The design is same but the techniques are different.

In designing of 6T S-RAM cell there are some limitations regarding read and write static noise margin (SNM). To overcome this a new 7T S-RAM cell is proposed by adding a new transistor to the existing 6 transistors.

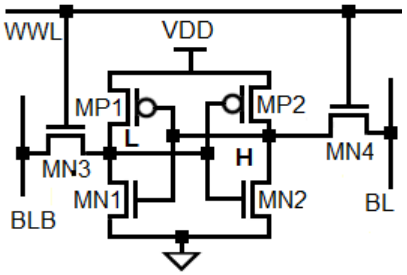

Fig.1. Conv 6T Static-RAM Single Bit-Cell.

The traditional 7T Static RAM design depicted in Fig.2 is a single bit Static RAM with a (Read Bit-line) RBL, a (Write Bit-line) WBL, a (Write Word line) WWL, as well as a read word line (RWL). In this scenario, transistor MP3 acts as supply feedback in order to bring down the pull up path while the writing operation is taking place [2].

In Conv7T SRAM Bit Cell, MP4 act like access MOS transistor because PMOS have a high level of susceptibility to fundamental error. Moreover, PMOS transistor showing less effect on noise during read and write operation. It likewise incorporates a read access transistor (MN4), where it fills in as common for the whole row. The excess MOS transistor are utilized to make-up the 6T SRAM single Bit-Cell [3]-[7]. This compensates for the substantial decrease in Read-Static-Noise-Margin (RSNM) caused by voltage division among access MOSFET and Pull-Down Network.

In spite of the way that maximal stability is accomplished when the read activity is occurring, the read current way is isolated from the storage node. However, adding more MOS transistors affects the volume of the SRAM and takes up a significant percentage of the memory. To counter these design constraints, a more effective S-RAM including one extra transistor, referred as 8T S-RAM cell is proposed. In comparison to the conventional 6T SRAM method, the conventional 8T SRAM shown in Fig.3 is designed with two transmission gates, implying the use of two NMOS access pass gate transistors [4] [9].

For a read operation, BL and BLB are Pre charging, then, making WLB line low and WL high and finishing the read activity in the SRAM cell. When both BL line and BLB line have been pre-charged, one of the bit-lines (BL or BLB) releases and others remains recharge based on data stored at node-L and node-H. This is how the read operation takes place.

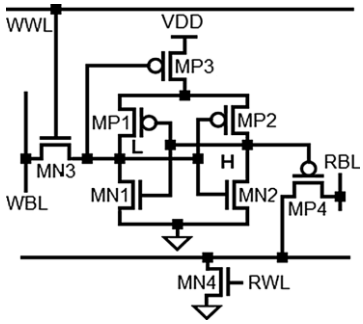

Fig.2. Conv 7T Static-RAM Single Bit- Cell.

When logic one is stored in H transistor MN1, then BLB begins discharging through MN3 once it becomes ON. BL remains at the initial pre charged state while MP3 and MN1 are read (WL-high, WLB-low). When the difference between BL and BLB reaches 50 mV, a sense amplifier connected to BL and BLB detects the difference and decodes the stored value in the storage nodes L and H. As a result of Transmission Gate use of.

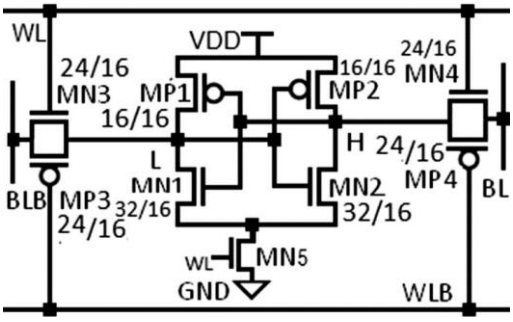

Fig.3. Conv 8T S-RAM Single Bit-Cell.

2. PROPOSED DESIGN AND SIZING

This study provides a proposed S-RAM circuit with 9 transistors Bit cell and 64×32 bits size of memory. The suggested circuit architectural architecture comprises of normal 7 transistors, with a transmission gate employed in place of the 9th transistor. The read delay is reduced when a transmission gate is used instead of a conventional transistor [5], [11]. The right-side portion of the circuitry is read decoupled in a quiet way that it is only accessed during the read operation.

During the reading process, only the right-side part of the circuit is activated, whereas the entire circuitry is activated during the writing activity. The S-RAM cell reads and writes data to memory based on the supply voltage delivered to the circuit V_{DD}. Assume logic one is stored, and to access it, a read action is executed, and to alter logic one to zero, a write operation is performed.

In the following paper, we will go over the proposed circuit and its functionality in further depth. This section includes a brief explanation of the suggested design, as well as simulated results and correlations observed. Finally, the paper is summarized.

The Fig.4 shows the proposed 9T Static RAM Bit-Cell. Bit-Line (BL) and Bit-line bar (BLB) connected write operation and Read Bit line (RBL) for read operation. Also included are a Write-Word-Line (WWL) and a Read Word-Line (RWL) (RWL). The MN5 and MN6 are Read Access Transistors where as MN4 and TG for write access. Leftover MOS transistors will act as a storage purpose like 6T Static RAM Bit cell.

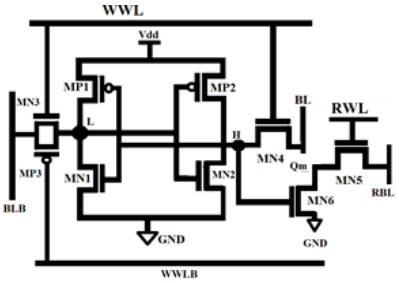

Fig.4. Proposed Read-Decoupled 9T Static RAM Single Bit-Cell

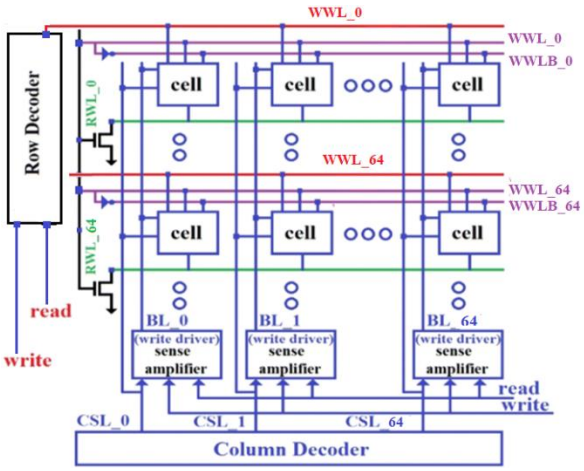

Fig.5. Architecture of proposed 9T Static RAM.

Since the technology node is 22nm so the channel lengths of all transistors are 22 nm, and the widths MOSFETs are picked as displayed underneath:

MP1 and MP2 have widths of 22 nm, 44 nm for MN1 and MN2, and 33 nm for MN3 and MN4. The MP3 transistors has 33nm and MN5, MN6 has 33nm and 44nm individually. The Fig.5 portrays the structural plan of the proposed Static RAM.

3. SIMULATION RESULTS

3.1 SIMULATION SETUP

All simulations are run on a 22-nm PTM with a variable inventory voltage to accomplish fluctuated results. As per ITRS 2011, a 10% variety in V_{DD} is projected in continuously scaled innovation hubs [2]. Thus, the plan measurements have been approximated for a stockpile voltage scope of 0.68 V to 0.40 V in 0.04V advances.

3.2 READ DELAY TIME ANALYSIS

MN5 and MN6 transistors are used in the read process. The transmission gate is connected to node '*L*.' Bit Line must be pre-charged and Read-Word-Line must be high for the read operation to be accomplished. The ON or OFF state of the MN6 is determined by the value of storage node '*L*' [6]. Assume that when node L is set to logical one, the MN5, MN6 are activated, and the Read-Bit-Line begins to discharge; the time necessary to discharge by 50mv is known as the read delay time. If the node

L=0, MN6 will remain in the OFF state and no Read-Bit-Line will be discharged.

Table.1. Read access time (T_{ReaD})

V_{DD} (V)	Conv-6T(ns)	Conv-7T(ns)	Conv-8T(ns)	Prop9T (ns)
0.68	0.404	0.492	0.121	0.392
0.64	0.466	0.539	0.132	0.460
0.60	0.542	0.607	0.146	0.543
0.56	0.622	0.690	0.162	0.622
0.52	0.704	0.810	0.182	0.702
0.48	0.799	0.970	0.207	0.811
0.44	0.934	1.230	0.240	0.952
0.40	1.200	1.880	0.288	1.220

The Table.1 shows a descriptive analysis of read access time to validate the performance of our proposed One-Sided 9T SRAM single Bit Cell. The Fig.6 depicts the results graphically to present a clear comparison. At high supply voltages, our proposed Read decoupled 9T SRAM bit cell demonstrates its fastness by exhibiting shorter read delay time (TRD).

As the comparative results take the reference circuits from differential circuits that are derived by some of the base papers that are taken as reference to proceed the work of the proposed circuit and the comparative results are taken for the circuits that are incorporated from the base paper that are chosen for literature survey.

3.3 WRITE DELAY TIME ANALYSIS

In the proposed circuit the right side of the circuit that is read de-coupled part is not included for write operation. Only the basic 6T transistor setup is accessed for writing. The transmission gate incorporated in circuit is only used to decrease read time and it is kept idle for write operation [7]. In this proposed SRAM Cell Bit-Line is used for reading as well as writing.

Bit-Line is assigned to logical one in order to perform a write operation. When the access transistor MN4 switches on, the node-H begins raising its value and the node-*L* begins discharging its value, a write operation occurs. The time taken to write a logical one (‘1’) that increases its value by 90% of supply VDD is termed to be write access time.

Bit-Line is assigned logical zero in order to write a ‘0’ operation. Where the access transistor MN4 switches on, node-H begins to decrease its value and node-*L* begins to increase its value. As a result, the write delay time to write ‘0’ is termed as the time it takes the ‘*H*’ node to reduce its value by 90% of the supply voltage.

Table.2. Write-access-Time (T_{WRITE})

V_{DD} (V)	Conv 6T (ns)	Conv 7T (ns)	Conv 8T (ns)	Prop9T (ns)
0.68	0.751	0.754	0.826	0.730
0.64	0.782	0.807	0.916	0.757
0.60	0.823	0.873	0.997	0.778
0.56	0.877	0.966	1.420	0.821
0.52	0.953	1.100	2.230	0.888
0.48	1.040	1.330	3.060	0.959
0.44	1.180	1.790	3.860	1.030
0.40	1.480	2.790	4.680	1.770

3.4 STATIC NOISE MARGIN ANALYSIS

The greatest noise that a circuit might endure during a read operation or write activity is indicated as the static noise margin. The margin while write operation is known as Write Static Noise Margin (WSNM), and the noise margin during read operation is known as Read Static Noise Margin (RSNM) [10]-[15].

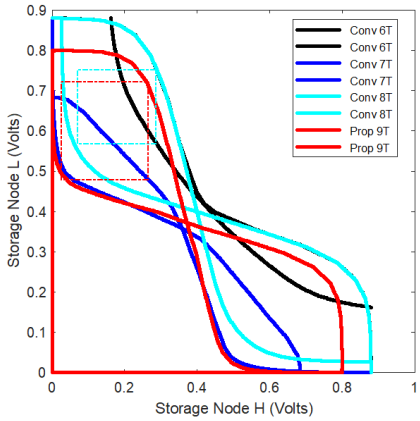

Fig.8. Read Static Noise margin vs Supply voltage

Read static noise margin determines how much maximum noise voltage (disturbance) that can tolerates the flipping of the present status of the stored data during a reading operation. RSNM can measured by butterfly curve. The largest side length of lob in Butter fly curve is the read static noise margin [16].

3.5 READ WRITE POWER DISSIPATION

The power expected to perform reading or writing activity is called read and write power of that circuit. The power while read activity is called read power and the power while write activity is write power [17]-[21]. The comparative results of proposed with conventional for read and write are shown in figures below.

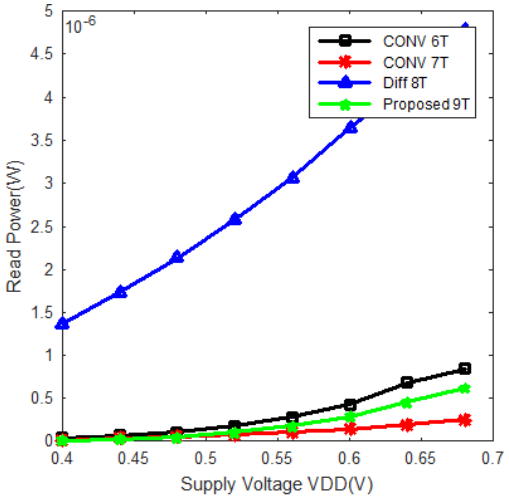

Fig.9. Supply voltage vs. write power

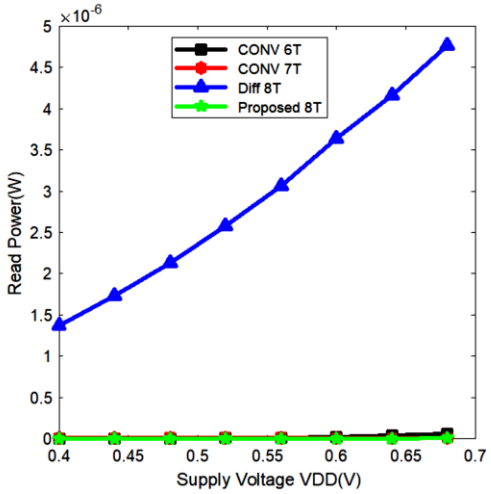

Fig.10. Supply voltage vs. read power

3.6 HOLD POWER

The power dissipation during hold or ideal mode the SRAM bit cell is termed as leakage or Hold power. That means when read and write operation is not happening and that time whatever power dissipated is called hold power. Power utilization while circuit not under use it relying upon the parts utilized in the circuit. In the proposed model we utilized transmission gate to diminish hold power [21]-[23]. While read activity the write part of circuit is off to consume less power as well as the other way around. The analysis results of hold power are shown below.

Table.3. Hold-Power (P_{hold})

V_{DD} (V)	Conv 6T (W)	Conv 7T (W)	Conv 8T (W)	Prop 9T (W)
0.68	4.4e-09	3.83e-10	1.8e-08	1.7e-09
0.64	2.9e-09	2.87e-10	1.4e-08	1.2e-09
0.60	1.9e-09	2.18e-10	1.1e-08	88.e-09
0.56	1.3e-09	1.65e-10	7.9e-09	6.3e-10
0.52	8.5e-10	1.24e-10	5.9e-09	4.4e-10
0.48	6.89e-10	9.23e-11	4.4e-09	3.1e-10
0.44	5.27e-10	9.64e-11	3.2e-09	2.1e-10
0.40	3.89e-10	8.72e-11	2.3e-09	1.4e-10

4. CONCLUSION

This paper presents Novel 9T SRAM Bit cell in 22 nm technology node for noise tolerance and low power application. Most of the design parameters of Static RAM Bit cell are examined. The proposed design provides less read/write delay, lower hold power, upgraded RSNM are accounted, to help the designers in choosing the best cells relying upon explicit necessities.

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