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DESIGN OF TWO STAGE CMOS OPERATIONAL AMPLIFIER IN 180NM TECHNOLOGY WITH LOW POWER, HIGH GAIN AND HIGH SWING

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Abstract

For certain applications, high bandwidth operational amplifiers are required. This necessitates research into the area of op-amp bandwidth expansion without influencing any other parameters significantly. This study presents a CMOS two-stage 0perational amplifier, that operates at 1.8 V power supply in 180 nm technology and has a bias current dependent input terminal. The supply voltage has been reduced to lower the system's overall power usage. Our primary goal is to reduce power loss, higher gain, and higher difference between maximum voltage and minimum voltage at output port. There is a trade-off between rate, power, and benefit at high supply voltages. The rate, power, and benefit of any circuit determine its performance. This op-amp has low standby power expenditure, with high driving capability, and runs at low voltage, consequential a low-power circuit. The op-amp has a gain of 70.37 decibel, a bandwidth of 53.01 MHz, and a phase margin of 27.83 degree. The operational amplifier power consumption and CMRR are also determined as 523µW and 73.33 decibel, respectively.

Keywords:

Low Power, Phase Margin, CMOS, Op-Amp

1. INTRODUCTION

An operational amplifier have main three terminals packaged as a components where two input one is inverting terminal and other is known as non-inverting terminal and single ended output. Op-amps are an essential component of numerous analog and combined sign structures. Op-amps with very much exclusive degrees of difficulty are used to comprehend functions ranging from direct current bias generation to filtering or high-rate amplification circuits. In this section ideal **0**p-amp and its fundamental characteristics, shape and its advantage bandwidth multiplication value, CMMR means common mode rejection ratio, power deliver rejection ratio and many others characteristics of operational-amp are mentioned. Op-amp is two stage differential amplifier first stage is known as a higher gain stage and second stage known as a higher swing stage with dual input terminals and single output terminal, endless gain, limitless enter resistance in order that there is no loading impact can arise in design of CMOS op-amp and zero output resistance of two stage differential operational amplifier.

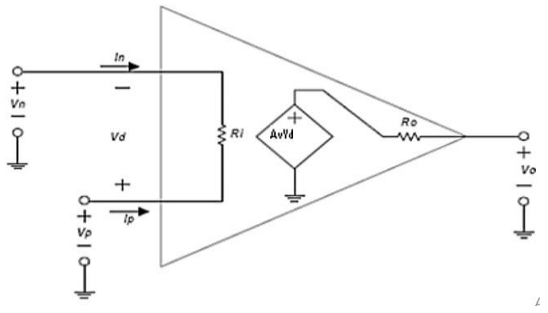

Fig.1. Symbol of Equivalent Circuit an Op-amp with R_{in} and R_0

Figure1 shows that Thevenin amplifier model of regular op-amp notation with R_{in} and R_o. This regular op-amp amplifies the voltage difference of two input terminals of op-amp, which is given that $V_D = Vp - Vn$, at the input port and set an output voltage, Vo at the output port of operational amplifier that is referenced to ground. The regular Thevenin amplifier model was derived to simplify complex calculations of circuits and this model is very frequently used by researcher and engineers in initial categorize mathematical approximation calculations. The regular Thevenin model of op-amp makes three simple assumptions:

- Gain $A_v = \infty$
- Input Resistance $R_i = \infty$
- Output Resistance $R_0 = 0$

After Applying above simple assumptions gain A_v, input resistance Ri, and output resistance R_0, in Fig.1 given above, results in the ideal op-amp model shown in Fig.2 where $R_i = \infty$, $R_0 = 0$.

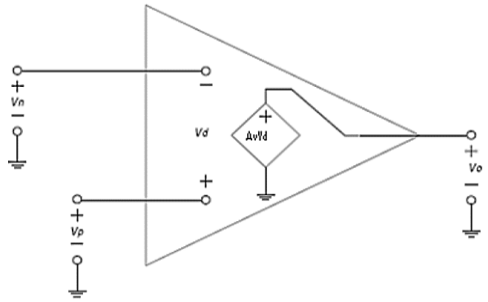

Fig.2. Ideal Op-amp with $R_i = \infty$ and $R_0 = 0$ Model

In this article now find out some other parameters using the ideal representation of op-amp.

$$I_N = I_P \text{ and } I_P = 0 \ (I_P = I_N = 0)$$

Due to input resistance $Ri = \infty$ we assume $I_N = I_P$ and $I_{P=}$ zero ($I_P = I_N = 0$). Due to this no loading effect at the input ends of op-amp.

$$V_0 = A_v \times V_D$$

Due to output resistance $R_0 = 0$ therefore no loading effect at the output end of op-amp: $V_D = 0$. At linear operation of the op-amp and differential voltage= 0, Then V_0 output voltage must be a predetermined voltage: $V_0 = V_D \times Av$. On the solving of given equation $V_D = V_0/Av$. Since Av = ∞, $V_D = V_0 / (A_v = \infty) = 0$.

When Common mode gain = 0. The perfect voltage source driving the output terminal relies just upon the difference voltage across its input terminals. It dismisses any voltage which is common to both voltage V_N and V_P.

- Bw of ideal model of op-amp = ∞
- Slew Rate (SR) of ideal model of op-amp = ∞

2. METHODOLOGY

We can characterize as a "excessive-advantage differential amplifying device". By excessive imply a value this is fine for the use, generally within the range of hundred and one to a hundred and five. While this two-stage op-amps are typically hired to execute response system. Open loop gain of the given system is preferred in step with the accuracy required of the closed loop system of the circuit.

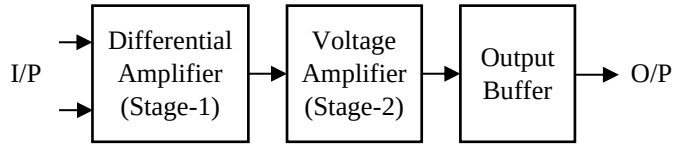

Fig.3. Block Diagram of Two-Stage Op-amp with O/P Buffer

A conventional op-amp structural design is made of three stages as proven in Fig.3, despite the fact that it is known as a "two-level" operational amplifier, ignoring the buffer degree (0.33 level). The first stage is differential input stage generally includes a higher-benefit differential amplifier. This first stage of three stage differential amplifier has pole with the maximum value of the device. The second stage which is voltage amplifier stage of above Fig.3 meets all specification of amplifier with moderate advantage. The last stage of above block diagram as a team spirit advantage CS amplifier which is known as source follower with a high frequency as well as insignificant pole value [7]. With the dual stage op-amp construction is a primary amplifier topology of Complementary Metal Oxide Semiconductor (CMOS) with excessive advantage. A regular CMOS differential amplifier degree is proven in Fig.4. Differential amplifiers are often desired because their differentials enter to one ended output communication and higher benefit. The input active component in Fig.4 given below is P type-channel metal oxide semiconductor field effect transistor with three terminals component which also known as PMOS. PMOS are used in a designing of two stage op-amp because of its progressed slew charge and decreased $1/f$ times noise [7]. Input of P-channel MOS devices also offer reduced strength supply rejection due to the modern-day mirror low sensitivity to exchange in electricity deliver voltage respectively.

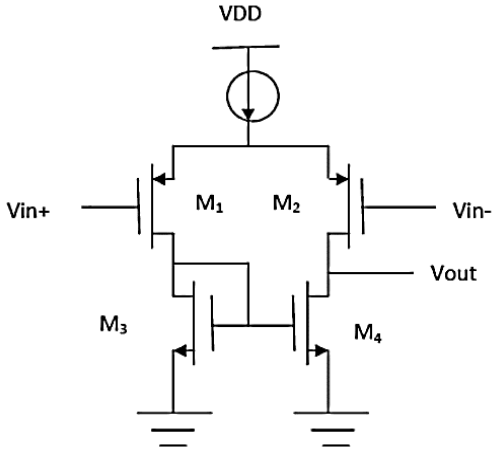

Fig.4. Differential I/P Stage Circuit with PMOS and NMOS

Calculations of gain A_1 and bandwidth Bw_1. For the differential input stage of CMOS circuit design, where $(r_{ds2}||r_{ds4})$ is the output resistance and $Cout$ output capacitance of first stage CMOS differential amplifier.

$$A_1 = g_{m1}(r_{ds2}||r_{ds4})$$

$$Bw_1 = (C_{out}(r_{ds2}||r_{ds4}))^{-1}$$

Realization of cascade design can enhance the reasonable benefit of op-amp at this level to a unwarranted value. The degree's principal pole has a C_{out} which is output capacitance at output terminal, inclusive of specifically, the drain-to-bulk capacitance of transistor M_2 and transistor M_4. While regularly negligible, some other transistor M_1 and transistor M_3 are connected then more number pole and zero are generated [8]. The dual stage realization of a not unusual supply amplifier proven shown in Fig.5. Similar to the primary degree, additional cascade component can enhance gain of this level of circuit. In this current level higher profits are regularly appropriate at the output. When the usage of miller repayment technology, despite the fact that better profits lead to decrease bandwidth and vice-versa due to unity gain bandwidth product.

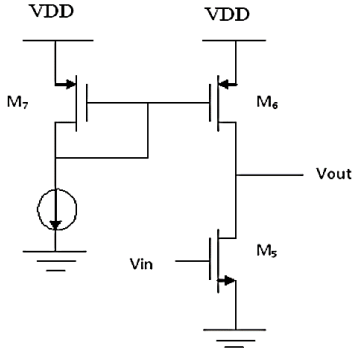

Fig.5. Common Source Amplifier Stage

Before really starting with the circuit designing section, let us examine a few significant terms for execution of an Op-amp. Slew rate,

$$S.R = I_5/C_c \quad (1)$$

where, I_5 is a tail current and C_c compensation capacitor.

$$\text{First-stage gain, } A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \quad (2)$$

$$\text{Second-stage gain, } A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6 + \lambda_7)} \quad (3)$$

$$\text{Gain bandwidth, } GB = (g_{m1})/C_c \quad (4)$$

$$\text{Output pole, } p_2 = -(g_{m1})/C_L \quad (5)$$

$$\text{RHP zero, } z_1 = (g_{m6})/C_c \quad (6)$$

$$\text{Positive CMR, } V_{in}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} + V_{T3(\max.)} + V_{T1(\min.)} \quad (7)$$

$$\text{Negative CMR, } V_{in}(\min) = V_{SS} - \sqrt{\frac{I_5}{\beta_1}} + V_{T1(max.)} + V_{DS5(sat.)} \quad (8)$$

$$\text{Saturation voltage, } V_{DS(sat.)} = \sqrt{\frac{2I_{DS}}{\beta}} \quad (9)$$

All given above relationships it is assumed that the each and every transistor which is use for designing of the circuit shown in Fig.6 given below are in saturation mode due to transistor in saturation mode transconductance g_m is high and this g_m help to increasing the overall Gain of the two stage CMOS differential amplifier so that

$$gm_1 = gm_2 = gm_{\mathrm{I}} \text{ (First stage)}$$
$$gm_6 = gm_{\mathrm{II}} \text{ (Second stage)} \quad (10)$$

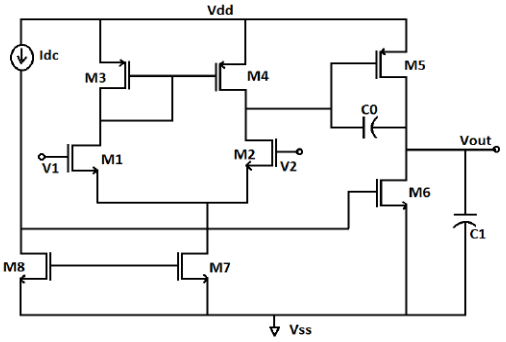

Fig.6. Circuit Diagram of Two Stage Op-amp using Eight Transistor

Following main steps are follow to designing of two stage CMOS differential amplifier [8]. The design procedure steps given below.

First of all, selecting a specific topology so that the size of circuit become minimizes and overall performance of the circuit become increase. After first step find out the direct current (DC) currents flow in a circuit. After second step calculating the aspect ratio $S=W/L$ of each and every transistor of the circuit, at the last step of design procedure of the circuit designing finalize the value of passive component like that resister and capacitors value connected in the CMOS circuit diagram in Fig.6.

In the designing steps of the circuit, we assume DC gain denoted by (A_v), Unity-gain bandwidth denoted by (GB), Input common-mode range [V_{in}(min.) and V_{in}(max.)], Load capacitance denoted by (C_L), Slew rate denoted by (S_R), Time taken by output to respond to a step change in input of the circuit known as a Settling Time it is denoted by (T_s), Output voltage swing [V_{out}(max.) and V_{out}(min.)] and Power dissipation denoted by (P_{diss}).

- The nominal device length that will keep the channel length modulation (λ) is constant and it give very good matching for current mirrors (M_3 and M_4) and (M_5 and M_8) has been chosen.
- Minimum value of compensation capacitor C_c considers for better phase margin (PM) which we want for fulfill our preferred goal, that is for a 60^o PM. We have utilized the additional relationship given below. Let us consider that pole greater than or equal to 10GB and compensation capacitor is greater than load capacitor ($C_c > 0.22\ C_L$) which is come from frequency response of the CMOS circuit.
- Calculate min. value of drain current (I_5) of NMOS transistor with the help of SR and C_c.

$$I_5 = SR \times C_C,$$

($i_c = c \times dv/dt$ where dv/dt is slew Rate)

If slew rate not given than choose I_5 based on settling Time T_s requirement.

$$I_5 = \frac{10\left(V_{DD} + |V_{SS}|\right)}{2T_s}$$

- Design transistor M_3 with the help of max. Input voltage measurement of the circuit design. S_3 is aspect ratio of transistor M_3 which= w_3 by l_3, w_3 and l_3 is channel width and length of the transistor M_3 respectively.

$$S_3 = \frac{2I_3}{K_3^1 V_{DD} - V_{in(\max)} - \left[V_{T_3(\max)} + V_{T_1(\min)}\right]^2} > 1$$

Here $s_3 = s_4$ as M_3 and M_4 from current mirror circuit.

- Due to C_{gs3} gate to source capacitor of transistor M_3 and C_{gs4} gate to source capacitor of transistor M_4, pole and zero will not be dominant by assuming pole P_3 (pole of transistor M_3) to be greater than 10 times of GB.

$$P_3 = g_{m3}/2C_{gs3} > 10 \text{ GB},$$

where

$$Cgs = 2/3 \cdot (w \times l)_3 \cdot C_{ox}$$
$$g_{m3} = 2I_3/[\mu_p C_{ox}(w/l)_3(V_{gs3}-V_{th3}]$$

- Design and Propose transistor M_1 and M_2 in terms of width and length relationship to get preferred objective of $G \times B$. S_1 is aspect ratio of transistor $M_1 = (w/l)_1$, w_1 and l_1 is channel width and length of the transistor M_1 respectively

$$g_{m1} = G \times B \times C_c$$
$$S_1 = \frac{(g_{m1})^2}{K_2^1 I_5}$$

where $S_1=(w/l)_1$; $I_1=I_5/2$

- Design and Propose transistor M_5 in terms of width and length relationship from the min. input terminal voltage. First of all, we have found out drain to source voltage of transistor M_5 $V_{DS5(sat)}$ and then we have calculated aspect ratio S_5. S_5 is ratio of channel width and length of transistor M_5. S_8 is ratio of channel width and length of transistor M_8.

$$V_{Ds5(sat)} = V_{in(\min)} - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{0.2} - V_{TI(\max)} \geq 100mV$$

$$S_5 = \frac{2I_5}{K_5^1\left[V_{DD(sat)}\right]}$$

Here $S_5 = S_8$ as M_5 and M_8 from current mirror circuit.

- Design and propose transistor M_6 in terms of width and length relationship and drain current I_6 of transistor M_6 by letting the second pole (p_2) is directly equal to 11/5 times of $G \times B$.

$$gm_6 = 2.2 \times gm_2 \times (C_L/C_C)$$

where gm_6 greater than or equal to 10 times of gm_1.

Let $V_{SG4} = V_{SG6}$, which gives $(w_6/l_6) = (w_4/l_4)(gm_6/gm_4)$. With the help of transconductance of transistor M_6 is gm_6 and aspect ratio of transistor M_6 is S_6 allows us to find out transistor M_6 drain current I_6 as

$$I_6 = \frac{g^2 m_6}{2K_6^1 S_6}$$

- Drain current I_6 of transistor M_6 we can find out by solving for aspect ratio of transistor M_6.

$$s_6 = (w/l)_6 = \frac{g^2 m_6}{2K_6^1 C_{DS6(sat)}},$$

- Design and propose transistor M_7 to get the preferred current ratios of drain current I_5 of transistor M_5 and drain current I_6 of transistor M_6 as a result aspect ratio of transistor M_7 is

$$S_7 = (I_5/I_6)S_6$$

where $s_6 = (w/l)_6$ and $s_7 = (w/l)_7$

- In this step verify gain value and power dissipation value according to terms and condition of the circuit.
- At the end step of our designing procedure simulating the circuit we have seen and validate that all the specifications are met.

3. PROPOSED TWO STAGE CMOS OPERATIONAL AMPLIFIER

In this proposed CMOS amplifier circuit 1.8 volts power supply is given. The bias CMOS circuit produced different bias voltage which is required by op-amp circuit. CMOS op-amp has been designed and simulated According to proposed compensation procedure with standard of 0.18 µm CMOS technology. The power consumption is 523µw. The Fig.8 shows that the op-amp model design using three numbers of PMOS (p-channel MOS) transistor and five numbers of NMOS (n-channel MOS) transistor. The Table.1 shows which is given below the specification of dual stage op-amp design model.

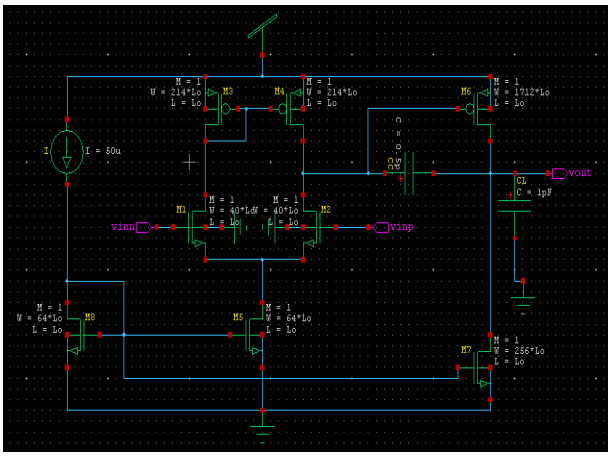

Fig.8. Schematic Model Op-amp with NMOS I/P Pair

Table 1: Characteristics of Two Stage Amplifier model

Characteristics Name	[1]	Proposed
Supply Voltage	2.5Volt	1.8Volt
Bias Current	60µAmp	50µAmp
C_C	3pF	0.5pF
C_L	10pF	1pF

4. SIMULATION RESULT

This special design of CMOS op-amp model has given result after simulation like that gain= 70.23 decibel and a 73.33 decibel common mode rejection ratio. The slew rate is 46.97 volts per microsecond. The phase margin (PM) is 27.83 degrees and the unity gain bandwidth is 53.01 MHz, making the design relatively stable as shown in Fig.10 graphical representation of frequency response of op-amp.

4.1 AC RESPONSE

In Fig.9 as shown below, there is a simple process of measuring the AC performance is offered by two input and single ended output model.

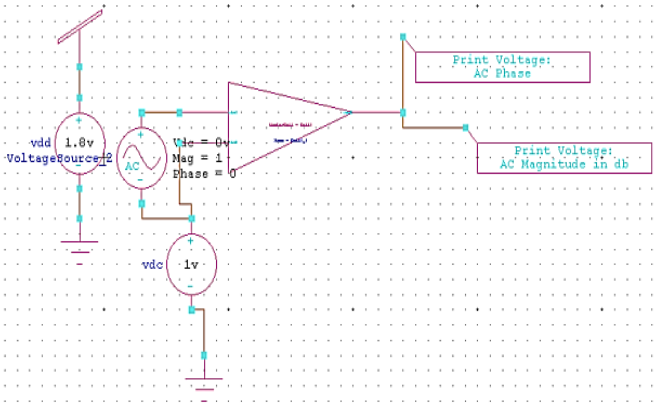

Fig.9. Simulating Model of Open Loop Frequency Response of an Op-amp

In this circuit design, the given amplifier is open loop, and the AC small signal is given at the input end. In Fig.10, a visual representation is a graph of the frequency response known as bode plot and second visual representation a graph which is expressing shifting of phase known as phase plot.

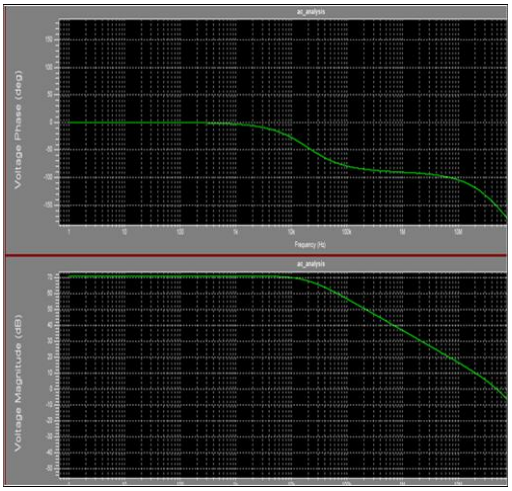

Fig.10. Frequency Response of Op-amp

A transient simulation of the amplifier having sinusoidal AC signal fed at input terminal with 1.8 volts direct current bias (DC bias).

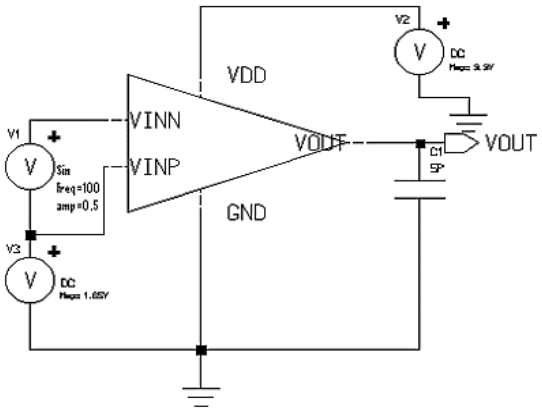

Fig.11. Transient Response Model with Sinusoidal Input

4.2 SLEW RATE

As given representation in Fig.12, a power supply V_{dd} is apply and a large step signal is fed to the input terminal of circuit given below with unity feedback arrangement. Mostly electronics devices rate of output voltage ten volt in 1ms. The Slew rate of amplifier is measured as 46.97v/µs. For the falling edge and rising edge of the visual representation as shown in Fig.13.

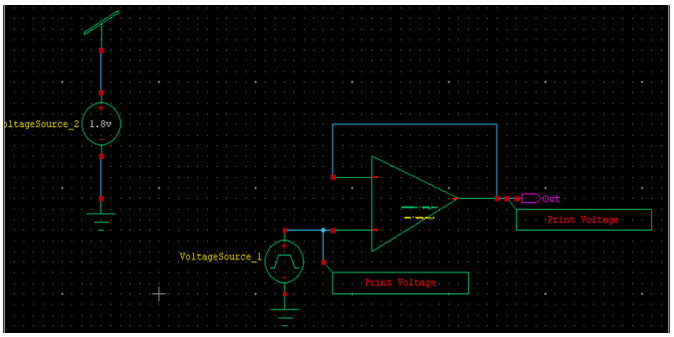

Fig.12. Schematic for Simulation and Measurement of the Slew Rate

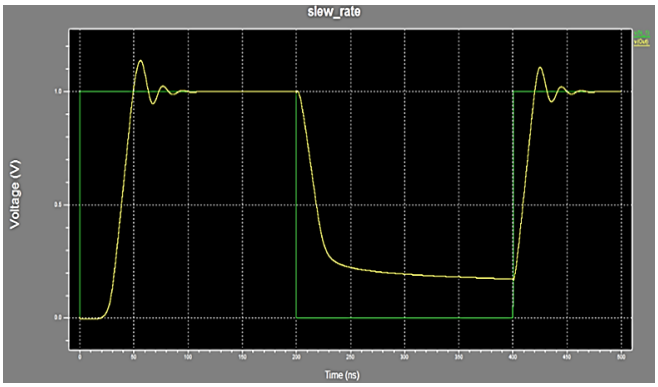

Fig.13. Slew Rate Enhancement Representation Between Voltage Vs Time

Table.2. Simulation Results of Op-Amp

Parameter	[1]	0.6Volt	1.8Volt
Power	107.88nW	523uW	583uW
G.BW	27.54kHz	47.58MHz	**53.01MHz**
Gain	60.86db	**70.37db**	70.23dB
Slew Rate (SR)	27.71mV/us	46.97V/us	**46.97V/us**
Phase Margin (PM)	63.5°	**27.83°**	25.67°
CMRR		72.86dB	**73.33dB**

The Table.2 shows that the values of op-amp characteristics such as Power, G.BW, Gain, SR, Phase Margin, and CMRR are approximately match with our desired target specifications.

5. CONCLUSION

A two-stage high gain low power operational amplifier has been designed in this study. The compensating capacitor "$C_{C,}$ plays a significant role in the design of the operational amplifier in terms of power consumption, noise characteristics and also with help of $C_{C,}$ we can control tail current as well as responsible for slew rate. The current buffer strategy has been employed since the power consumption reduces as the compensating capacitor value increases, making it less sensitive to process fluctuations. Tanner EDA (SPICE Platform) was used to design and simulate the operational amplifier in 0.18µW CMOS manufacturing technology and with 1.8Volt power supply. The operational amplifier has a 70.37dB dc gain, a 53.01MHz unity gain bandwidth, and a 27.83° phase margin. The operational amplifier power consumption and CMRR are also determined to be 523µW and 73.33 dB respectively.

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