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THE ENHANCEMENTS IN STORAGE CAPACITY AND LONG-TERM DATA RETENTION OF MULTIDIMENSIONAL FLASH MEMORY IN MODERN MICROCIRCUIT APPLICATIONS

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Abstract

Generally, flash memory is a type of permanent memory for computers in which the contents can be reprocessed or erased electronically. Compared to programmable read-only memory that can erase electricity, operations on it can be performed on modules located in different locations. Flash memory is much less expensive than EEPROM, which is why it has become a dominant technology. Especially, in situations, this stable and long-term data retention is required. Its use is allowed in various cases like digital audio players, photo and video cameras, mobile phones and smartphones, and specialized Android applications on the memory card. Additionally, it is also used on USB flash drives, traditionally used to store and transfer information between computers. The proposed model provides enhancements to the storage capacity of various flash memory modules. In a saturation point, the proposed model achieved 93.03% of NOR Memory management, 89.31% of NAND Memory management, 94.25% of Ferroelectric RAM Memory management, and 94.53% of Magnetic RAM Memory management, 96.05% of Ovonic Unified Memory management and 96.16% of Salcogenide RAM Memory management.

Keywords:

Flash Memory, Permanent Memory, Read-Only Memory, EEPROM, Data Retention, USB Flash Drives

1. INTRODUCTION

Flash memory is a type of device that can store information on its board for a long time without using much power [1]. In addition, one can observe higher speeds of data access and better resistance to operating shock compared to hard drives. With these characteristics, it has become very popular for devices powered by batteries and accumulators [2]. Another undeniable advantage is that if the flash memory is compressed on a solid card, it is almost impossible to destroy it by any standard physical means, so it can withstand boiling water and high pressure [3]. The way to access data in flash memory is very different from that used for normal displays [4]. Low-level access is done by the driver. Conventional RAM immediately responds to calls to read and write information, results in such operations, and takes time to think about the design of the flash memory [5]. At this time, flash memory is widespread, built on single-transistor components with a floating gate. This allows a higher storage density than DRAM, which requires a pair of transistors and a capacitor element [6]. At the moment, the market is filled with various technologies to develop the basic components for this type of media developed by leading manufacturers [7]. They vary by the number of layers, the methods of recording and deleting information, and the structure of the structure, commonly referred to by name [8].

At present, there are two most common types of microcircuits: NOR and NAND. In both, the storage transistors are connected to bit lines in parallel and series, respectively [9]. In the first category, cell sizes are much larger and have the potential for quick random access, which allows programs to run directly from memory [10]-[11]. The second is characterized by small cell sizes and fast serial access, which is very convenient when you need to create module type devices where large information is stored [12]. The most portable devices use solid-state drive (NOR) memory type. However, devices with a USB interface are becoming more popular now. They use NAND memory. Gradually, this changes first [13]-[14]. The first models of mass-produced flash drives did not please users with high speeds [15]. However, now the speed of writing and reading information is at a level where you can watch a full-length movie or run the operating system on a computer [16]. Many manufacturers have already proven that machines can be replaced by hard drive flash memory [17]. But this technology has a very significant drawback, which is a barrier to replacing existing magnetic disks with this medium. Due to the nature of the flash memory device, it allows to erase and write information for a certain number of cycles, which is accessible even to small and compact devices, not to mention how often it is done on computers [18]. If you use this type of media on your computer as a solid-state drive, a complicated situation will arise very quickly [19].

Such a drive is built on the property of field-effect transistors that hold it in a floating gate, and the absence or presence of a transistor is considered a logic unit or zero in binary data [20]. The recording and erasure of NAND memory are done by tunnel electrons using the Fowler-Nordheim method with the participation of the conductor. It is not required; it allows you to create cells of minimal size [21]. But it is this process that leads to the cells because the current pushes the electrons into the gate, violating the dielectric barrier [22]. However, the guaranteed shelf life of such memory is ten years. The wear and tear of the microcircuit are not due to the reading of the information but to the processes involved in erasing and writing it, because the reading does not need to change the structure of the cells, but only transfers electricity [23].

Naturally, memory manufacturers are actively working to extend the service life of these types of solid-state drives: they try to ensure the consistency of the write / erase processes throughout the sequence cells so that some do not wear out more than others. For uniform load distribution, software paths are mainly used [24]. For example, wear equalization technology is used to eliminate this phenomenon. In this case, often the modified data is moved to the address space of the flash memory and, therefore, the registration is carried out at different physical addresses. Each controller is fitted with its balancing mechanism, so it is very difficult to compare the performance of different models because the implementation details are not published. As the size of flash drives increases every year, it is necessary to use more and more

efficient algorithms to ensure the stability of the devices. One of the best ways to combat this phenomenon is to reserve a certain amount of memory, which ensures load consistency and error correction with special logical deflection mechanisms for changing the physical volumes that arise during intense work with the flash drive.

2. LITERATURE REVIEW

To prevent information loss, irregular cells are blocked or replaced with backups. Such a planned distribution of volumes makes it possible to ensure uniformity of loads, increasing the number of cycles by 3-5 times, however, this is not enough [4]. Other similar types of drives are characterized by the inclusion of a table with a file system in their service area. This prevents failures in reading the information on a logical level, for example, in the event of a faulty shutdown or sudden interruption in power supply [5]. And when using removable devices, the system does not provide cache, and then often overwriting the file allocation table and table of contents can have a very devastating effect. Even special programs for memory cards cannot help in this situation [7]. For example, with one call, one user overwrites a thousand files. Also, the study used the modules where they are located to record. But with each update of any file, the service areas were overwritten, i.e. the allocation tables went through this process a thousand times. For this reason, first, the blocks occupied by this particular data will fail. Wear-balance technology works with such modules, but its performance is very limited. It does not matter what type of computer you are using; it will fail exactly when the flash drive is provided by the creator [9].

It is noteworthy that as the capacity of the microcircuits of such devices increases, the number of total letter cycles decreases as the cells get smaller, so less and less voltage is required to dissolve the oxide walls. It isolates the floating gate. With the increase in the efficiency of the devices used, the problem of their reliability began to get worse and worse, and the class of memory cards now depends on many factors [12]. The reliability of such a solution is determined by its technical features and current market conditions. Due to fierce competition, manufacturers are forced to reduce production costs. Including simplification of design, use of components from the cheaper package, weakening control over production and other ways [13]. For example, the Samsung memory card costs more than its lesser-known counterparts, but its reliability raises far fewer questions. But even here it is difficult to talk about the complete absence of problems, and it is difficult to expect even more from the devices of completely unknown manufacturers [14]. Despite the obvious advantages, the characteristic of an SD memory card has several disadvantages, which prevent it from further expanding its scope. That is why the search for alternatives in this area continues. Of course, first, they try to upgrade the existing flash memory, which does not lead to any fundamental changes in the existing production process [15]. So, one thing should not be doubted: the companies involved in the production of these types of drives will continue to advance the traditional technology and try to use their full potential before switching to another type [16]. For example, the Sony memory card is currently available in a wide range of capacities, so it is assumed that it will continue to be actively sold. Today, however, on the brink of industrial operation, there is a full range of alternative data storage technologies, some of which can be implemented immediately at the beginning of a favourable market environment [17].

3. PROPOSED MODEL

It has been proposed to increase the capacity of unstable memory. It is generally accepted that the mechanism of operation of existing technologies involves rewriting the data in the reading process with all modifications of the basic components, which leads to a certain control over the speed capability of the devices. FRAM is memory characterized by simplicity, high reliability and speed of operation. A proposed model drive has three main components shown in Fig.1:

- **Memory Connector**: A well-known connector for the interface between the flash drive and the computer system, the personal computer system, and the multimedia centre. Or even a car radio;
- **Memory Controller** is the most important circuit element. Connects device memory with a USB connector and controls data transfer in both directions;
- **Memory Chip** is the most expensive and important part of a USB flash drive. The amount of information stored on the card determines the speed at which data can be read/written.

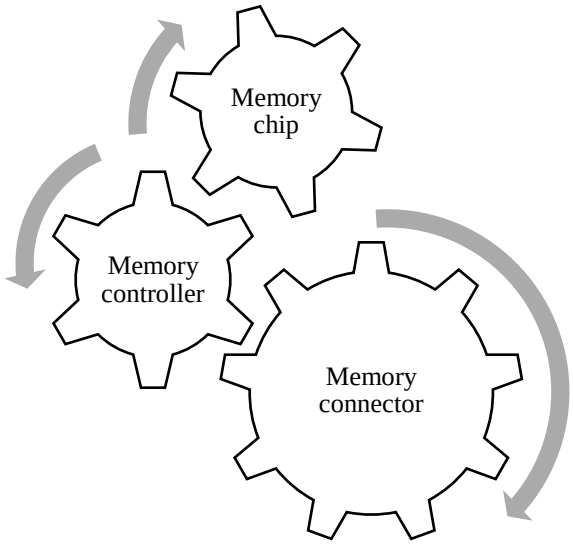

Fig.1. Proposed model memory construction

These properties are now common to DRAM - the existing unstable random-access memory. But here the possibility of long-term data storage will also be added, which can be classified, among the advantages of such technology is the ability to isolate resistance to various types of penetrating radiation, which may be required in the specialized devices used. To work in these conditions of increased radiation or space exploration. Another type of memory that is considered highly promising today is MRAM. It is characterized by high-speed indicators and energy independence. In this case, a thin magnetic film is placed on the silicon substrate. MRAM is static memory. It does not need to be rewritten from time to time and the information is not lost when the power is turned off. In theory, such a solution has a higher

storage density and maximum reliability and increased efficiency. The indicator of the maximum number of rewrite cycles is high here, for which a computer is used, in which case the flash drive lags by several orders. Key components of a proposed model are shown in Fig.2:

- Memory connection,
- Memory Controller
- PCB board
- NAND memory module
- Crystal Oscillator
- LED indicator
- Protection switch

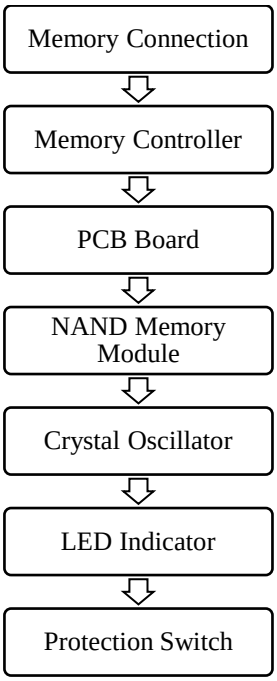

Fig.2. Components of the proposed module

A data storage unit is a floating gate transistor that holds electrons (charges), which is a data storage unit in flash memory. The main types of NAND and NOR flash memory are based on transistors. The principle of operation is based on the conversion and recording of the electric charge in the isolated area (pocket) of a semiconductor structure. The types of memory in the proposed model are shown in Fig.3

- **Multi-Level Cell Memory**: high-capacity cells and cheaper but longer access times and fewer write / erase cycles
- **Single-Level Cell Memory**: Cells with short access time and maximum write / erase cycles
- **Compact Flash** is the oldest standard for memory types. It has high reliability, large volume and high data transfer rate. Due to its large size, it is used in professional video and photographic equipment.
- **Multimedia Card** is a small size, highly compatible with various devices and has a memory controller. The SD card (Secure Digital Card) is the result of the development of the MMC standard. The card has encryption protection against unauthorized copying, increased protection of information from accidental deletion or deletion, and a mechanical write protection switch.

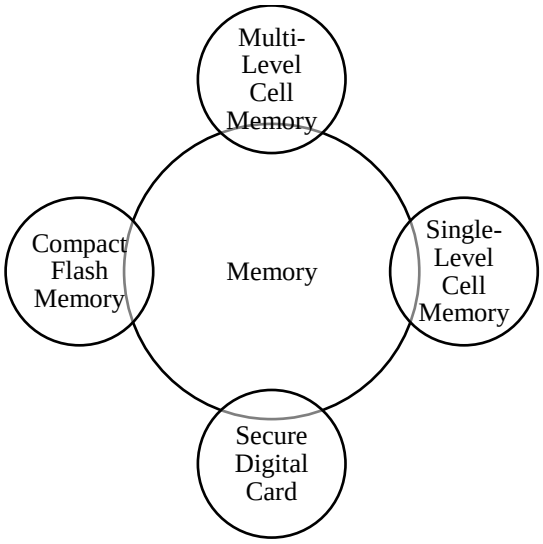

Fig.3. Types of proposed memory structure

In short, we place the same floating gate surrounded by a thin layer of conductor, between the control gate and the channel through which the current flows from the source to the drain. As a result, when current flows through such a modified field-effect transistor, some high-energy electrons pass through the conductor into the tunnel and end up in the floating gate. When the electrons were tunnelling and wandering into this gate, it became clear that they had lost their energy and could not return to practice. Again we have a two-dimensional array that needs to be filled in with 0 and 1. Since it takes a long time to accumulate charge in the floating gate, a different solution is used in the case of RAM. The memory cell consists of a capacitor and a conventional field-effect transistor. In this case, the capacitor, on the one hand, has a primitive physical device, but, on the other hand, it is trivially implemented in the hardware.

4. RESULTS AND DISCUSSION

The proposed storage capacity and long-term data retention (SCLDR) model was compared with the existing persistent virtual memory (PVM) for efficient capacity, Application-Aware Autonomous SCM Capacity Adjustment (3ASCA), Efficient Array File System (EAFS) and Dynamic Adjustment of Storage Class Memory (DASCM)

4.1 NOR MEMORY MANAGEMENT

The transistor has two gates: control and floating. The latter is completely isolated and can hold electrons for up to 10 years. The cell has a drain and a source.

Table.1. Comparison of NOR Memory management

Inputs	PVM	3ASCA	EAFS	DASCM	SCLDR
200	77.43	69.87	56.11	87.53	96.70
400	75.94	67.90	53.69	85.33	94.71
600	75.14	66.77	53.28	84.53	93.51

800	72.81	65.56	51.68	83.86	93.03
1000	71.80	65.19	49.36	82.43	91.60
1200	71.16	63.66	48.11	81.34	90.44
1400	70.50	63.16	45.38	80.86	89.67

During programming with voltage, an electric field is generated at the control gate and a tunnelling effect occurs. Some electrons pass through the insulator layer and attack the floating gate. The performance of the NOR Memory management was shown in Table.1.

The floating gate charge changes the width of the drain-source channel and its conductivity, which is used to read. The proposed model programming and reading cells are very different in power consumption: Flash memory devices use more current when writing, and while reading, power consumption is lower. To destroy the information, a high negative voltage is applied at the control gate and the electrons (tunnel) from the floating gate to the source. In the NOR configuration, each transistor must be connected to an individual contact, which increases the circuit size. This problem is solved using the NAND framework.

4.2 NAND MEMORY MANAGEMENT

The NAND-type is based on the NAND element. The principle of operation is the same, which differs from the NOR type only in cells and their interactions. As a result, it is not necessary to connect individual cells to each cell, so the size and cost of the NAND chip will be significantly lower. Writing and deleting are fast. The performance of the NAND Memory management was shown in Table.2.

Table.2. Comparison of NAND Memory management

Inputs	PVM	3ASCA	EAFS	DASCM	SCLDR
200	68.80	66.23	48.71	80.10	91.44
400	68.47	64.73	48.12	78.23	90.40
600	67.13	63.62	47.14	77.40	90.27
800	65.99	63.24	45.93	76.49	89.31
1000	64.94	62.23	44.79	75.57	89.74
1200	64.01	61.16	43.93	74.32	88.88
1400	62.99	60.21	42.93	73.24	88.44

However, this proposed configuration does not allow spontaneous cell access. NAND and NOR architectures are now parallel and do not compete with each other because they are used in different areas of data storage.

4.3 FERROELECTRIC RAM MANAGEMENT

The information storage algorithm is realized here by applying the ferroelectric effect. It assumes that the material is capable of maintaining polarity in the absence of an external electric field.

Table.3. Comparison of Ferroelectric RAM Memory management

Inputs	PVM	3ASCA	EAFS	DASCM	SCLDR
200	76.56	74.65	57.81	84.12	92.12
400	76.89	76.15	58.40	85.99	93.16
600	78.23	77.26	59.38	86.82	93.29
800	79.37	77.64	60.59	87.73	94.25
1000	80.42	78.65	61.73	88.65	93.82
1200	81.35	79.72	62.59	89.90	94.11
1400	82.37	80.67	63.59	90.98	94.98

Each FRAM memory cell is formed by placing a very thin film of ferroelectric material in the form of crystals between a pair of flat metal electrodes forming a capacitor. The performance of the NOR Memory management was shown in Table.3.

In this case, the proposed model data is stored within the crystal system. It also prevents the effect of charge leakage, which can lead to data loss. The data in the FRAM is retained even if the supply voltage is disconnected.

4.4 MAGNETIC RAM MANAGEMENT

At the moment, most experts agree that this type of memory can be called next-generation technology because the existing prototype shows much faster performance. Another advantage of this solution is the low cost of chips. Flash memory is made using a special CMOS process. Furthermore, MRAM microcircuits can be manufactured according to a standard technical process. The performance of the NOR Memory management was shown in Table.4.

Table.4. Comparison of Magnetic RAM Memory management

Inputs	PVM	3ASCA	EAFS	DASCM	SCLDR
200	67.93	71.01	50.41	76.69	90.86
400	69.42	72.98	52.83	78.89	92.85
600	70.22	74.11	53.24	79.69	94.05
800	72.55	75.32	54.84	80.36	94.53
1000	73.56	75.69	57.16	81.79	95.96
1200	74.20	77.22	58.41	82.88	97.12
1400	74.86	77.72	61.14	83.36	97.89

Also, materials may be materials used in conventional magnetic media. It is much cheaper to produce large volumes of such microcircuits than anything else. An important characteristic of the proposed model is its ability to run instantly. This is especially valuable for mobile devices. In fact, in this case, the value of a cell is determined by a magnetic field, not by electricity like conventional flash memory.

4.5 OVONIC UNIFIED MEMORY MANAGEMENT

Another type of memory that many companies are actively working on is solid-state storage based on amorphous semiconductors. It is based on phase conversion technology, which is similar to the principle of recording on regular disks.

Table.5. Comparison of Ovonic Unified Memory management

Inputs	PVM	3ASCA	EAFS	DASCM	SCLDR
200	77.82	66.91	50.25	75.68	92.86
400	79.45	68.65	51.83	77.10	94.15
600	79.93	70.99	54.03	78.36	95.16

800	81.22	71.80	55.66	80.35	96.05
1000	83.33	74.09	56.80	82.82	96.42
1200	84.82	76.02	59.00	84.26	98.06
1400	86.63	77.75	60.15	85.98	98.43

Here the state of an object in the electric field changes from crystalline to amorphous. And this change continues even in the absence of tension. The performance of the NOR Memory management was shown in Table.5.

The proposed model takes care of these devices and differs from traditional optical discs in that the heat is caused by the action of electricity, not a laser. In this case, the reading is carried out due to the reflectance difference of the object in different states, which is sensed by the sensor of the drive.

4.6 SALCOGENIDE RAM MANAGEMENT

This technology is based on phase transformations, in one stage the material used in the carrier acts as a non-conducting amorphous material; in the second it acts as a crystalline conductor. The performance of the NOR Memory management was shown in Table.6.

Table.6. Comparison of Salcogenide RAM Memory management

Inputs	PVM	3ASCA	EAFS	DASCM	SCLDR
200	76.23	72.98	49.00	76.32	91.69
400	77.90	74.11	51.93	77.58	94.16
600	79.85	74.46	53.47	79.47	94.96
800	81.84	76.41	55.50	80.67	96.16
1000	84.42	77.18	56.40	72.23	96.80
1200	86.41	77.56	58.37	83.98	98.06
1400	88.43	78.69	59.84	84.91	99.06

The transfer of a storage cell from one state to another is carried out using electric fields and heating. Such chips are characterized by resistance to ionizing radiation. At a saturation point, the proposed model achieved 93.03% of NOR Memory management, 89.31% of NAND Memory management, 94.25% of Ferroelectric RAM Memory management, and 94.53% of Magnetic RAM Memory management, 96.05% of Ovonic Unified Memory management and 96.16% of Salcogenide RAM Memory management.

5. CONCLUSION

At this time there are many options for storing information, some of which require static electricity (RAM), some are always sewn into the control microcircuits of the surrounding technology (ROM), and some combine the properties of those and others. The latter, in particular, include Flash. It sounds like unstable memory, but the rules of physics are hard to get rid of, and you still have to rewrite information on flash drives from time to time. The proposed SCLDR model was compared with the existing models. The only thing that can unite all these types of memories is more or less the same operating principle. Some have two-dimensional or three-dimensional matrices, which are filled in approximately the same way with 0 and 1, from which we can read these values or change them, viz. All of these are direct analogues of its predecessors - memory in ferrite rings.

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