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EFFECT OF ADDER CIRCUITS OVER MULTIPLIER DESIGN BASED ON VEDIC MATHEMATICS

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Abstract

Multiplication is critical for computers linked to cryptography or the ALU function. It consumes more chip area and time than the other ALU functions. The speed of the processor, coprocessor, or embedded system may depend on the multipliers' speed. Nowadays, designing a small, high-performance multiplier is a critical challenge in computer architecture, cryptographic hardware design, and embedded system design. One of the better solutions is developing a digital multiplier design based on Vedic mathematical formula. The performance of the Digital Vedic Multiplier (DVM) is entirely dependent on the adder network. DVM is evaluated here using KS Adder and CLA Adder. There are several publications on this topic, but the primary shortcoming is that they focus exclusively on the DVM without addressing the influence of the adder circuit. This work aims to investigate the impact of the adder circuit on the space-speed trade-off inherent in the design of the DVM.

Keywords:

Vedic Mathematics, Digital Vedic Multiplier, Adder, Urdhv Triyagyabhyam, Speed

1. INTRODUCTION

Arithmetic operations are essential for the architecture of digital processors and application-specific systems. Multipliers are essential components of a wide range of high-efficiency systems, including FIR, microcontrollers, microprocessors, embedded processor digital signal processors (DSP), and other types of computer circuits. Because the multiplier is typically the slowest subsystem of any processing system, the efficiency of a system is typically determined by the output of the multiplier, which is typically the slowest subsystem. Furthermore, it is typically the most expensive option when it comes to consuming space because of this, increasing the speed and area of the multiplier might be a substantial design issue. On the other hand, area and speed are generally conflicting constraints, with the result that speed increases occur mostly in greater areas [1]-[5], [10]-[15].

Conventional multiplication is based on three basic calculations

- Generation of the partial product (PPG)
- Reduction of Partial Product (PPR)
- Carry propagates addition (CPA)

All three steps required high logic hardware. To enhance the multiplier's performance, rearrangement of the adder is one of the old methods [16]. Vedic mathematics is ravelled by Shankaracharya Ji Barti Kirshna Teerathji Maharaj (1884- 1960) from Sthaptya-Veda, Up-Veda of Atharv Veda, Shankaracharya Ji gave 16 sutras and 16 Sub sutras (Formula and subformula).

The formula suggested in Vedic mathematics is also suitable for the design figure of the digital multiplier. Multiplier based on Vedic mathematics yields higher speed than other multipliers [6]. In previous work, most researchers pay attention to speed parameters; for example, in [25]-[30], they design High-Speed ALU but silent over space requirements. So, this may lead to a choice dilemma for future researchers who have to develop a high-speed circuit with limited resources. This paper tries to find a tread-off between space and speed.

2. URDHV-TRIYAGYABHAYM: THE VEDIC SUTRA, VERTICAL AND CROSS

In this sutra, partial products are generated vertically and cross manner [15]. The main advantage of this formula is that it will produce all the partial products in parallel and then sum up them. For example, we considered 12×13 (decimal multiplication of 12 and 13). This sutra includes the following steps

- Multiply 2 and 3 (2×3) = 6 (vertical multiplication) (in this case, there is single-digit number 6, we can write it as 06 here 0 will be treated as carry for step 3; this step gives list significant digit of result 6 in this case.
- Multiply 1 and 1 (1×1) = 1 (vertical multiplication) (If this step answers more digits, then the least significant of this result will be added to the outcome of step 3 as a most significant bit, and if this sum yields any carry, then this carry will be added to the remaining digit of this step, i.e., step 2; this will give us most significant digits of multiplication.
- Multiply 1 and 3 (1×3) and multiply 1 and 2 (1×2) add them with carry from step 1 and list significant bit of step 3 if any (cross multiplication); 1×3+1×2+0=5; this step gives us the middle term of the result.
- Now answer is 06+20+30+100=156 [1].

Let's assume an example 12×13:

- 1×1 = 1 (100th position) (vertical multiplication) yield 100
- 2×1 = 2 (10th Position) (cross multiplication) yield 20
- 3×1 = 3 (10th Position) (cross multiplication) yield 30
- 2×3 = 6 (unit position) (vertical multiplication) yield 06

Let's assume another example 99×99:

- 9×9=81 (vertical multiplication of most significant digit; yield 8100 (81*100))
- 9×9=81(cross multiplication yield 81*10=810; 10th position)
- 9×9=81(cross multiplication yield 81*10=810; 10th position)
- 9×9=81 (vertical multiplication of least significant digit; yield 81)

So, result is (8100+810) + (810+81) = 9801.

3. THE MULTIPLIER (DIGITAL VEDIC MULTIPLIER (DVM))

The DVM can be implemented by two sutras, namely Urdhv-Triyagbham Sutra and Nikhila Sutra [21]-[23]. The DVM can be implemented by a 2×2-bit multiplier, as shown in Fig.1 [9]. This design may also be utilized as a fundamental building element for implementing 4×4, 8×8, 16×16, and other multipliers [17].

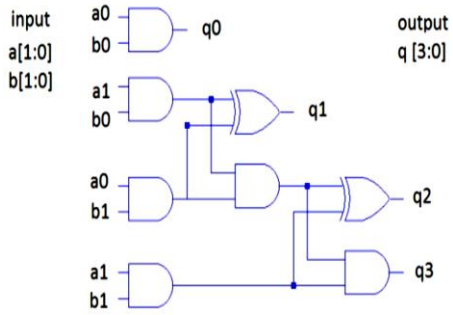

Fig.1. Implementation of 2×2 bit Digital Vedic Multiplier

Many designs are available to implement the above sutra into a high-speed digital multiplier [18] [19]. The Fig.2 shows that this design requires four multipliers, two adders, and one-half adder network [7]. The Fig.2 is the design implementation of a 4-bit digital multiplier that needs a 2-bit multiplier [20].

When we increase the number of bits, the design in Fig.2 will lead to more delay due to the half adder network. However, this design shows a better result than the booth algorithm reported in [7].

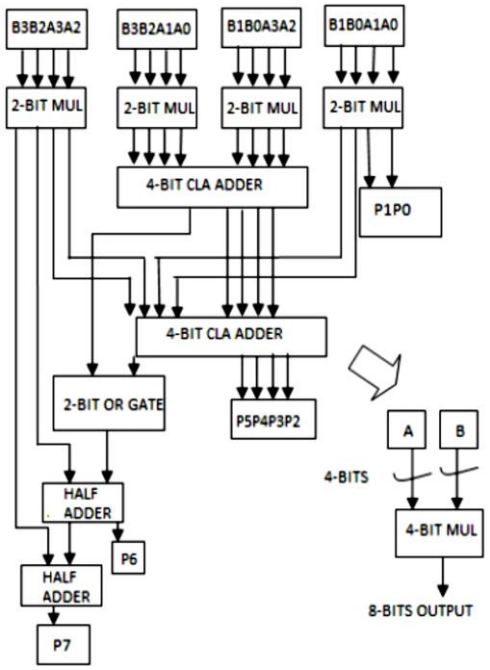

Fig.2. Implementation of 4×4-bit Digital Vedic Multiplier

Another design of (Fig.3) 16-bit multiplier as described in [8] requires 4, 8bit multiplier and 1, 16-bit CS Adder and 2, 17-bit Adders for implementing multiplier of 16 bit.

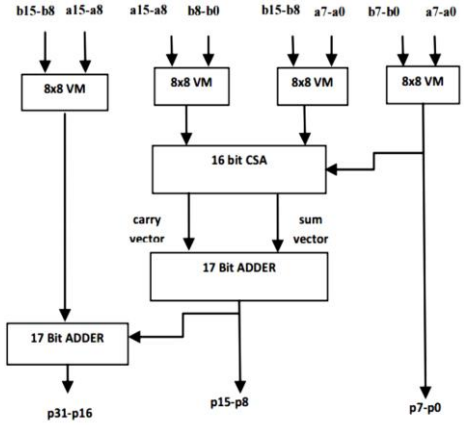

Fig.3. Implementation of 16x16 bit Digital Vedic Multiplier

In Fig.4, the 16×16 DVM is rendered with 4, 8×8 blocks. Here are the bit (n=16) multiplicands, which result in a 32-bit size. For both inputs, a and b, the input is divided into smaller segments of 0.5n size. i.e. 8. The lower part (8bits) of q_0 are passed directly to the result, while the upper bits are applied to the addition tree [6].

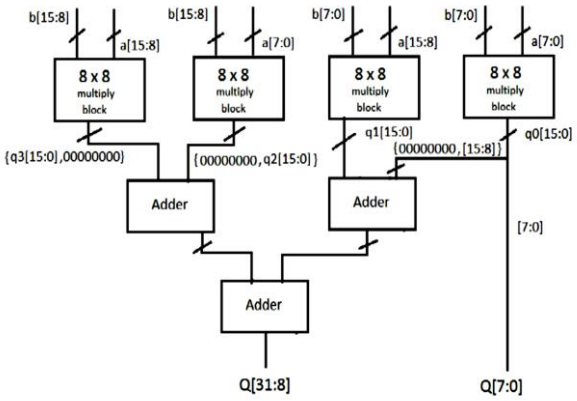

Fig.4. Implementation of 16×16 bit Digital Vedic Multiplier

The whole process can be summarized for N bit multiplier as follows:

Let's assume A and B are two n bit numbers divided into higher and lower order, i.e. A_h, A_l, B_h and B_l. Then the partial product can be generated in the following manner $A_h\ A_l \times B_h\ B_l$.

- Partial product 1 $A_h \times B_h$ (Vertical Product)
- Partial Product 2 $A_l \times B_l$ (Vertical Product)
- Partial Product 3 $A_h \times B_l$ (Cross Product)
- Partial Product 4 $A_l \times B_h$ (Cross Product)

To generate partial products 1, 2, 3, and 4, we need four multipliers of 0.5n bits. After generating all partial products, we must add the entire partial product to our final result. In addition, three adders will be required.

3.1 KEY PLAYER FOR SPEED AND AREA (ADDERS)

From the above design, it is clear that the adder plays a crucial role in the speed and performance of the digital Vedic multiplier. If we modify the configuration of the adder, then we can find the trade-off between the area and speed of the digital multiplier [11].

In [12], they used KS Adder to speed up the performance of DVM at the cost of the area. This paper examines speed and area trade-offs for KS adder and CLA adder. The K-S adder and CLA adder design are discussed in [11].

4. RESULTS AND DISCUSSION

This paper implements *KS* Adder and CLA Adder for addition blocks. The output of 8-bit KSA is shown in Fig.5

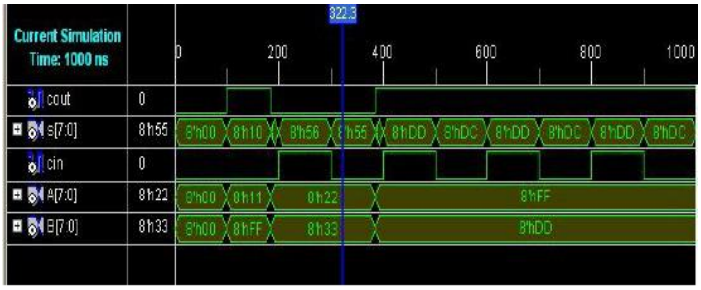

Fig.5. Output of 8-bit KSA

And the output of 8-bit CLA adder is shown in Fig.6, and the output of DVM 4 bit is shown in Fig.7

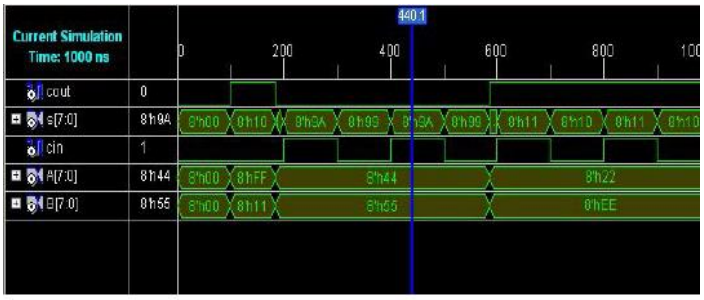

Fig.6. Output of 8-bit CLA Adder

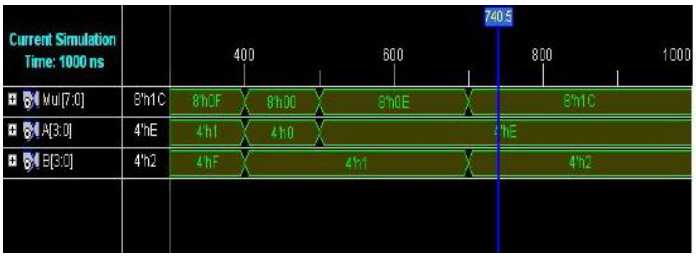

Fig.7. Output of 4-bit Digital Vedic Multiplier

Table.1. Result Reported in [11]

Parameter	CLA DVM	KSA DVM
Area	89 Slices	105 Slices
Delay	29.891 ns	31.788

Table.2. Result of [24]

Parameter	4-bit RCA Adder	4-bit KS Adder
Area	23 Slices	19 Slices
Delay	12.421 ns	11.737

Table.3. Result Of Adders

Parameter	8-bit CLA Adder	8-bit KS Adder
Area	9 Slices	16 Slices
Delay	15.235 ns	14.005

Table.4. Comparison of DVM based on CLA Adder and KS Adder

Parameter	8-bit DVM (CLA)	8-bit DVM (KS Adder)	8 Array Multiplier
Area	95 Slices	108 Slices	71
Delay	25.269 ns	24.489	25.527

From Table. 1 to Table.4, it is clear that CLA implementation of DVM consumes less hardware, 95 slices, as compared to 108 slices of KSA. However, KSA implementation gives better speed, it is tested for the 8-bit multiplier, and if we increase the number of the bit, then hardware requirement will also increase. This work helps the designer to choose a better option for their implementation.

5. CONCLUSION

In this paper, Digital Vedic Multiplier is designed and implemented in VHDL and compiled by the Xilinx synthesis tool (XST) [14]. The Table.1 shows the result of [11], Table.2 shows the analysis of adders and Table.3 shows the design implemented in this paper. The results clearly shows that we can optimize DVM for speed or area. This work can be extended with other available adders to find a better trade-off between area and time.

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