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ASSESSMENT OF POWER QUALITY DISTURBANCES USING STATIONARY WAVELET PACKET TRANSFORM BASED DIGITAL HARDWARE

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Abstract

The stationary wavelet packet transform (SWPT) based digital design is presented in this paper for the real-time tracking of power quality disturbances in the electrical power distribution system. In the SWPT technique, wavelet decomposition tree has been built with the MAC-based architecture of the low-pass filter and high-pass filter. Here, signal decomposition has been performed by the low-pass filter and high-pass filter, then filter coefficients undergo an upsampling process which produces fundamental and odd harmonic components at the output. In this way, the SWPT technique extracts various frequency components from distorted power supply waveform with respect to time and the perfect location of power quality disturbances. The proposed technique hardware implementation has been completed on the Xilinx Artix-7 FPGA AC701 board by utilizing XSG/Vivado design suite 2018.3. Then digital hardware performance has been validated through experimental test signals, which is a combination of voltage dips, voltage swells, and momentary interruptions. The obtained results prove that the SWPT-based digital design is robust and accurate for real-time tracking of power quality disturbances (PQD).

Keywords:

Stationary Wavelet Packet Transform (SWPT), Power Quality Disturbance (PQD), Field-Programming Gate Array (FPGA), Xilinx System Generator (XSG)

1. INTRODUCTION

Renewable energy sources significantly contribute to electricity generation from the past decades to fulfill the energy demand other than conventional energy sources. Consequently, high-power semiconductor devices and power electronic converter are widely used to ensure the power grid secure and reliable working. The insertion of these nonlinear loads in the power grid causes harmonic current and voltage unbalance, i.e., voltage sags, voltage swells, momentary interruption, temporary transients, which would change the attributes of the power supply waveform at the distribution system [1]. As a result, harmonic current causes overheating of equipment, signal interference, circuit breaker failure, and voltage disturbances causes damage to the protection circuits and control equipment, crosstalk, light flicker, and degrades the performance of the three-phase motor. Therefore, it is essential to recognize and diagnose these issues exactly with location to efficient control and moderate the power quality parameter.

Fast Fourier Transform (FFT) is the most traditional technique to analyze signals prescribed by the IEC and IEEE standards [2]. FFT algorithm is simple and computationally efficient but provides erroneous results in the state of nonstationary signals; thereby, it is suitable for only stationary signals. FFT algorithm is limited by the picket fence effect, spectral leakage, and fixed-time frequency resolution. In the literature survey, Discrete Wavelet Transform (DWT) [3], Discrete Wavelet Packet Transform (DWPT) [4]-[6], Hilbert–Huang transform (HHT) [7],[8], Kalman filter (KF) [9] and Artificial Neural Network (ANN) [10]-[13], all of the above stated methods show a measurable reduction in the problems associated with FFT also each and every method has its pros and cons according to its usage in various applications. The HHT technique is suitable for analyzing nonstationary and non-linear signals in which the decomposition process is performed with an adaptive basis function. Here, the output efficiency is based on the correct spline fitting that is a complex part of HHT and requires more tools to interpret the output data. Kalman Filter-based technique is a good choice for continuous assessment of power supply waveform to minimize power quality disturbances in the electrical distribution system. The accuracy of the KF is based upon earlier information of the system along with perfect filter modeling. Furthermore, it suffers from filter dropping off issues in the event of sudden amplitude variation of the signal [14].

The ANN-based technique is becoming more famous among the research community since it can perform parallel processing of signal utilizing neurons. The efficiency of the neural network depends on the learning by the training data set, so it is difficult to cover all possible real situations in the training data set. The time-frequency domain analysis of signal is possible with Wavelet Transform (WT), which is implemented utilizing filter banks [6], [15]-[21]. The width of window function involved in WT is adjusted in such a way so that it provides a larger resolution in frequency or time for the correspondingly low or high-frequency component, which makes this method more beneficial over other techniques as suggested in the literature for tracking of PQD.

The advanced form of Discrete Wavelet Transform (DWT) is the Discrete Wavelet Packet Transform (DWPT), and both of these multiresolution techniques are efficient in detecting the PQD. The best part of the DWPT technique is providing uniform frequency bandwidth of the distorted signal; however, filter down-sampling performed at every decomposition level reduces the wavelet coefficients. On the other hand, DWPT is a time-varying transform and computations involved in DWPT, making it costly. The polyphase architecture is used to minimize the calculations involved in the DWPT method for harmonic estimation in [16]. The undecimated wavelet packet transform-based approach is suggested in [19] for harmonic analysis shows excellent results.

This paper presents the hardware implementation of the Stationary Wavelet Packet Transform (SWPT) technique for the real-time tracking of the PQD. In the SWPT method, during decomposition of distorted power supply waveform, filter upsampling is involved so that it provides uniform frequency bandwidth at the output by replication of fundamental and each harmonic component; in this way it overcomes the problem of DWPT. The SWPT technique follows the time-invariant property, which makes this method most suitable for analyzing the voltage dips, voltage swells, and momentary interruption [21]. The synthesis of the proposed digital design has been done via Xilinx system generator (XSG)/Simulink domain, then implemented on Xilinx Artix-7 field-programming gate array (FPGA) AC701 board. In real-time tracking of power quality disturbance, different experimental test signals validate the proposed digital design efficiency on the FPGA platform via the hardware co-simulation process.

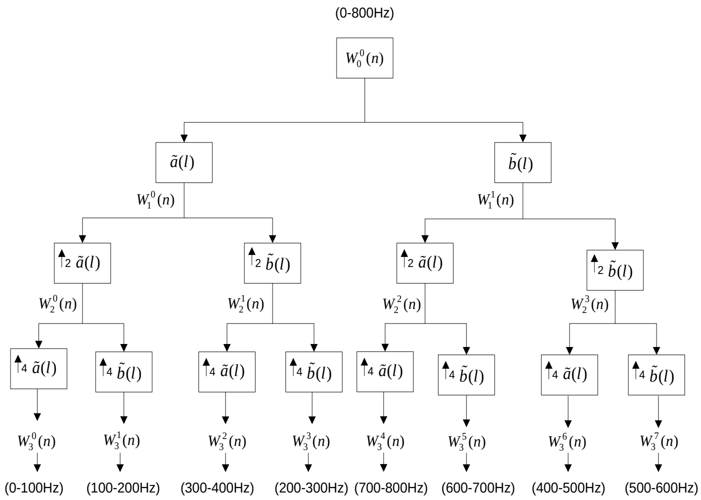

Fig.1. Stationary Wavelet Packet Transform decomposition tree

The paper remaining part is put in the following order; section 2 presents the mathematical foundation and implementation methodology of the SWPT technique. Section 3 presents the hardware design of the proposed architecture on the FPGA platform. In section 4, the proposed digital hardware performance has been investigated through experimental test signals. At last, the conclusion is presented in section 5.

2. STATIONARY WAVELET PACKET TRANSFORM (SWPT) TECHNIQUE

In the SWPT method, the distorted power supply waveform acts as input for a three-level SWPT decomposition tree at level zero. Then, signal decomposition is performed with the low pass filter and high pass filter that produces the approximation coefficients and detail coefficients, respectively. The next level involves upsampling of filter coefficients along with successive decomposition on both approximation and detail coefficients. This process is performed again up to the last decomposition level; thus, the distorted signal is decomposed into eight equal frequency bands and provides precise replication of fundamental and higher-order harmonic components at the output. The SWPT method is very much similar to the DWPT method; however, DWPT involves downsampling by two, which reduces half of the filter coefficients at every decomposition level.

As suggested in the literature, Daubechies wavelets are the most suitable mother wavelet for the analysis of power quality disturbances, which are dB10 with 20 coefficients [22], dB20 with 40 coefficients [23], dB43 with 86 coefficients [24], and also, Vaidya Nathan wavelet with 24 coefficients [25]. The wavelet filter implemented using a larger number of filter coefficients minimizes the spectral leakage problem, and it gives an accurate measurement of PQD [26]. However, it needed more hardware resources for FPGA implementation of the proposed technique with increased computations that provide slower response time. Hence, dB20 with 40 coefficients and dB30 with 60 coefficients are the optimal solution for the accurate identification of PQD with minimum resource utilization. Consequently, SWPT wavelet filters have been implemented via FIR filters utilizing dB30 with 60 coefficients. The wavelet filter coefficients of SWPT are rescaled to keep retain the energy by the Eq.(1) and Eq.(2).

$$\tilde{a}(l) = a(l)\big/\sqrt{2} \tag{1}$$

$$\tilde{b}(l) = b(l)\big/\sqrt{2} \tag{2}$$

Additionally, these filters should fulfill the criterion as stated in Eq.(3).

$$\sum_{l=0}^{L-1}\tilde{\alpha}^2(l) = 0.5\sum_{l=0}^{L-1}\tilde{\alpha}(l)\tilde{\alpha}(l+2n) = \sum_{l=-\infty}^{\infty}\tilde{\alpha}(l)\tilde{\alpha}(l+2n) = 0 \tag{3}$$

where, $\tilde{\alpha}(l) :\Leftrightarrow \tilde{a}(l)\,\text{or}\,\tilde{b}(l)$

The SWPT wavelet filters are satisfying the quadrature mirror filter (QMF) criterion given by Eq.(4) and Eq.(5).

$$\tilde{b}(l) = (-1)^l\,\tilde{a}(L-l-1) \tag{4}$$

or

$$\tilde{a}(l) = (-1)^{l+1}\tilde{b}(L-l-1) \tag{5}$$

The filter upsampling involved in SWPT reconstructs the wavelet filter at any decomposition level. Hence, Eq.(6) and Eq.(7) describe the modification of filter coefficient at the j^{th} decomposition level by inserting 2^{j-1} zeros between each pair of coefficients of $\tilde{a}_j(l)$ and $\tilde{b}_j(l)$.

$$\tilde{a}_j(l) = \begin{bmatrix} \tilde{a}(0), \underbrace{0,...,0}_{2^{(j-1)}-1}, \tilde{a}(1), \underbrace{0,...,0}_{2^{(j-1)}-1}, \\ \tilde{a}(2),........., \tilde{a}(L-1), \underbrace{0,...,0}_{2^{(j-1)}-1} \end{bmatrix} \tag{6}$$

$$\tilde{b}_j(l) = \begin{bmatrix} \tilde{b}(0), \underbrace{0,...,0}_{2^{(j-1)}-1}, \tilde{b}(1), \underbrace{0,...,0}_{2^{(j-1)}-1}, \\ \tilde{b}(2),........., \tilde{b}(L-1), \underbrace{0,...,0}_{2^{(j-1)}-1} \end{bmatrix} \tag{7}$$

The SWPT decomposition tree is presented in Fig.1, and the coefficients at the 2ith node, nth sample, and jth decomposition level are calculated by Eq.(8) and Eq.(9).

$$W_j^{2i}(n) = \sum_{l=0}^{L-1}\tilde{a}_j(l)W_{j-1}^{i}(n-l) \tag{8}$$

$$W_j^{2i+1}(n) = \sum_{l=0}^{L-1}\tilde{b}_j(l)W_{j-1}^{i}(n-l) \tag{9}$$

3. HARDWARE DESIGN OF SWPT TECHNIQUE ON FPGA

It is important to detect and diagnose the power quality disturbances in real-time hence, FPGA is most suitable for executing the proposed SWPT technique on the hardware platform [27] [28]. Therefore, the proposed method is implemented on Xilinx Artix-7 FPGA AC701 board is connected through the JTAG interface to a laptop (inclusive of MATLAB/Simulink, Xilinx System Generator). In Fig.2, the digital design of the SWPT technique is presented, which is implemented with the Xilinx block set available on XSG. The hardware co-simulation procedure involves converting Simulink data types (integer, double, single, and fixed) and system generator data types (fixed-point or floating-point). Consequently, the "Gateway In" block (act as a virtual analog-to-digital converter) and "Gateway Out" (act as a virtual digital-to-analog converter) is used. The wavelet coefficients have been quantized using 2 complements with the fixed-point format of signed 18-bit carrying 12 fractional bits, and the calculation of these wavelet coefficients is performed in module-1. Here, "db30" with 60 coefficients are utilized as the mother wavelet for the proposed technique. The filter architecture based on the direct or transpose form presented in [16] needs a large number of embedded multipliers.

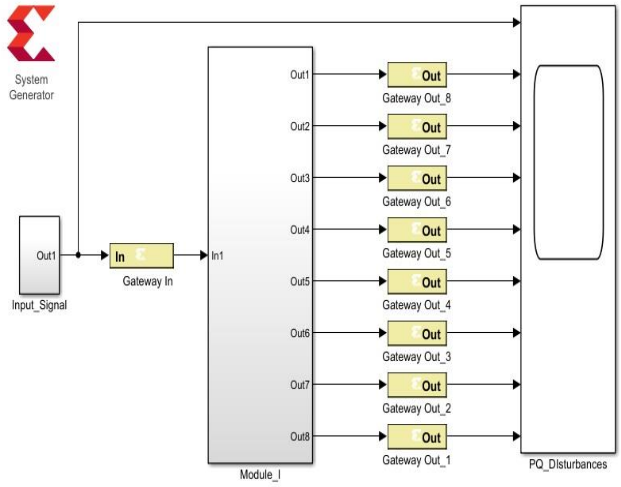

Fig.2. Digital design of the proposed SWPT based method

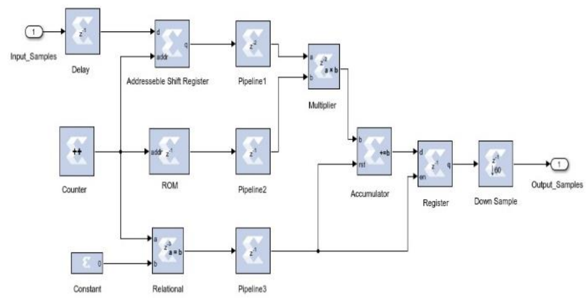

Fig.3. Digital design of MAC based FIR filter on XSG

Hence, the MAC-based FIR filter has been used to implement the low pass filter and high pass filter, which uses only one embedded multiplier to perform multiplications associated with that filter. The MAC-based FIR filter digital design is shown in Fig.3. Here, a single port ROM stores the filter coefficients in 18-bit fixed-point format with 12 fractional bits. The MAC-based architecture is slightly slower than the direct or transpose form but converges to the desired timing requirement as needed for real-time detection of PQD by the proposed technique. To efficiently use resources available on the FPGA board, the choice of suitable quantization and overflow is essential, and every functional block work upon pipelining method to enhance their performance. The proposed architecture works with a clock frequency of 50 MHz on the Xilinx Artix-7 FPGA AC701 board to converge the timing and resource utilization characteristics.

4. PERFORMANCE EVALUATION

This section illustrates the performance evaluation of the SWPT based digital design implemented on the Xilinx Artix-7 FPGA AC701 board for real-time tracking of various power quality disturbances. Here, the experimental setup comprises both software and hardware platform, which worked together using the hardware co-simulation process. Hence, the experimental test signal (which has a double-precision floating-point format having 1.6kHz sampling frequency) is generated on the MATLAB-Simulink software installed on a computing engine (1.99-GHz Intel Core i7 processor, with 8-GB random access memory) and interconnected with Xilinx Artix-7 FPGA AC701 board through JTAG interface. In real-time, signal quantization is performed through the "Gateway In" block in 18-bit fixed-point format with 12 fractional bits at the input section; then, it feeds to the implemented algorithm developed on the Xilinx Artix-7 FPGA AC701 board.

4.1 TEST 1: POWER QUALITY DISTURBANCES TRACKING BY SWPT BASED DIGITAL DESIGN

This section validates the proposed digital hardware efficiency to track the various power quality disturbances in the real-time scenario. Therefore, the experimental test signal consists of voltage swells from 0.20s to 0.25s, voltage dips from 0.40s to 0.45s and momentary interruptions from 0.60s to 0.65s duration along with fundamental, 3^{rd}, 5^{th} and 11^{th} harmonic components generated for one second duration on the MATLAB/Simulink platform. The mathematical form of experimental test signal is given by Eq.(10). The obtained results have been reported in Fig.4, which shows the performance of the proposed SWPT based digital design. It is seen from Fig.4 that the FPGA-based digital architecture has successfully extracted the odd harmonics with fundamental component and provides the precise location of voltage dips, voltage swells, and momentary interruptions, respectively. However, real-time tracking of PQD shows minor latency, which is different for fundamental and odd harmonics. The input signal is routed through various arrangements of low pass filters and high pass filters in the SWPT decomposition tree; thus, filter response is different for various frequency components.

$$v(t)=\begin{bmatrix} u(t)+0.5\{u(t-0.20)-u(t-0.25)\} \\ -0.5\{u(t-0.40)-u(t-0.45)\} \\ -\{u(t-0.60)-u(t-0.65)\} \end{bmatrix} \times \begin{bmatrix} 10\sin(\omega t)+5\sin(3\omega t) \\ +3\sin(5\omega t)+2\sin(11\omega t) \end{bmatrix} \tag{10}$$

Hence, group delay for specific filter $h(n)$ is defined by the mathematical Eq.(11) and Eq.(12).

$$\tau_H(\omega)=-\frac{d\phi(\omega)}{d\omega} \tag{11}$$

$$H(\omega) = |H(\omega)|e^{j\phi(\omega)} \qquad (12)$$

where, $\phi(\omega)$ is a phase of the wavelet filter.

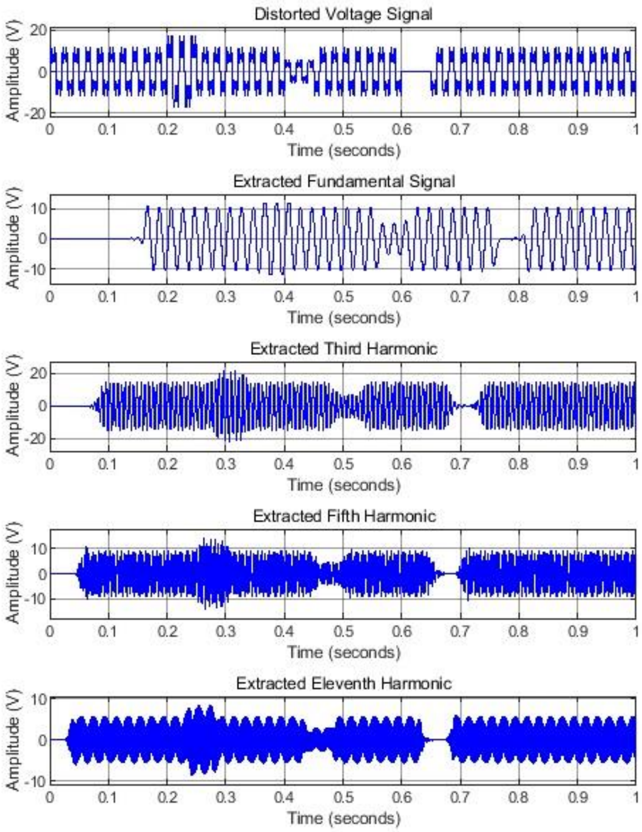

Fig.4. Tracking of PQD by SWPT technique on FPGA platform

Here, Table.1 shows the time taken by various frequency components for PQD tracking in real-time by the digital hardware implemented on the Xilinx Artix-7 FPGA AC-701 board at 50 MHz operating frequency. Also, Table.2 reports the resource utilized by the proposed digital design and the maximum operating frequency of the digital hardware on the FPGA. It is noticed from Table.2 that MAC-based digital hardware needed very low resources on the FPGA board. Consequently, ASIC of the proposed SWPT based digital design can be built at a very low cost.

Table.1. Time taken by the SWPT based digital hardware for tracking of power quality disturbances

Harmonics order	**Clock cycle required in tracking various frequency components**	**Time taken by proposed design on FPGA (ms)**
1^{st}	46,290	0.09258
3^{rd}	37,120	0.07424
5^{th}	28,100	0.0562
7^{th}	41,520	0.08305
11^{th}	25,780	0.05156
13^{th}	31,670	0.06334

Table.2. Resource utilized by the SWPT based digital hardware on FPGA board

Resource Category	**Number of resources used in proposed digital design**	**Available resources on FPGA board**
FFs	5,591(2.09%)	2,67,600
LUT	2,751(2.06%)	1,33,800
BRAM	14 (3.84%)	365
DSP slices	28 (3.78%)	740
Maximum Operating Frequency		100 MHz

4.2 TEST 2: TRACKING OF POWER QUALITY DISTURBANCES IN THE PRESENCE OF NOISE BY THE DIGITAL HARDWARE

Under this test case, the robustness of the proposed digital hardware has been verified against noise. Therefore, the experimental test signal contains voltage swell, voltage sag, momentary interruption, and additive white Gaussian noise (AWGN) with a signal-to-noise ratio (SNR) of 60dB. The obtained results have been reported in Fig.5. It is seen that the location of PQD has been efficiently detected by the proposed digital design despite the presence of noise. Thus, the proposed method has proved its capability in the occurrence of noise.

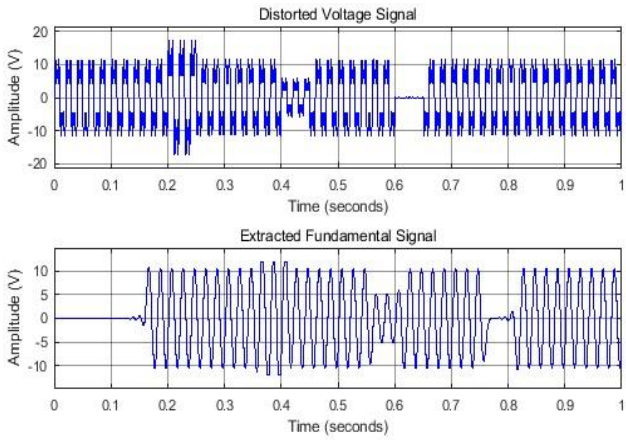

Fig.5. Tracking of power quality disturbances on FPGA platform

5. CONCLUSION

This paper presents the efficient implementation of SWPT-based methodology on hardware platform to track power quality disturbances. The proposed digital design hardware implementation has been completed on the Xilinx Artix-7 FPGA AC-701 board utilizing XSG/Vivado design suite 2018.3. The performance of the proposed digital design has been evaluated through experimental test signals generated on the MATLAB/Simulink platform. By the obtained results it is concluded that the SWPT based digital hardware is efficient in tracking of voltage dips, voltage swells, momentary interruption with their precise location. Also, the proposed hardware is capable to extract the fundamental and odd harmonics from the distorted voltage signal. The proposed digital hardware converges to timing requirements and adequately utilizes the resources available on the FPGA board. Hence, SWPT based digital design is applicable for real-time monitoring of PQD in the electrical power distribution system.

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