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# LITERATURE SURVEY ON AREA OPTIMIZATION OF CMOS FULL ADDER DESIGN

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***Abstract***

***In this paper, a novel architecture for a dynamic logic-based full adder is introduced and analyzed. In full adder architecture, the XOR and XNOR gates are commonly employed as basic logic units. In the report, improved XOR and XNOR logic gate topologies are employed to produce a full adder circuit. The envisioned XOR/XNOR gate architecture has a full logic cycle. The suggested adder design is modelled using a traditional 180 nm CMOS technique. The simulated outcomes using the SPICE simulation tool demonstrated that the proposed network has significant advantages in energy loss and efficiency while compared to previously published designs.***

***Keywords:***

***MOS Current-Mode Logic (MCML), Ternary Full-Adder (TFA), Low Power, Gate-Diffusion-Input (GDI), Ripple Carry Adder (RCA)***

## 1. INTRODUCTION

In VLSI systems, which include microprocessors, digital signal processing (DSP), image processing, and video processing, arithmetic operations are frequently used. A binary adder or Full Adder circuit is the basic structure that can be used to design arithmetic operations; As a result, the building block for Binary inclusion is a 1-bit Full Adder cell, which is the most basic and generally used arithmetic operation in digital signal processor (DSP), microprocessors, and application-specific control systems.

As a result, the effectiveness of this fundamental unit immediately increases the entire design efficiency. As a result, enhancing this capability is critical for the device's actual quality. The quantity of transistors in Full Adder architecture is a significant aspect since transistors counts have a significant impact on design complexity.

For such type of sub-micron CMOS technology topology selection, area, speed, and power dissipation is a very important aspect of low power and high-speed implementation. These barriers can be resolved by using Gate Diffusion Input (GDI) methodology. Thus, helping to boost the combinational logic circuits performance with respect to low-power and reducing static power dissipation Gate Diffusion Input (GDI) is a layout process is an effective tactic By Using GDI technique most of the logic functions can be performed with minimum transistor ranks.

GDI technique is best suited for configuration of high-speed, reduced power sophisticated circuit design with a smaller number of discrete components number especially in comparison to CMOS as well as TG technique.

## 2. LITERATURE SURVEY

Somashekhar et al. [1] described three transistors are used in the XOR gate, and two 3T XOR and one 2T multiplexer are used in the CMOS complete adder. The suggested complete adder uses a total of eight transistors to produce a power consumption of 4.604 μW and a total area of 144 $\mu m^2$. The 1-trit Ternary-Full-Adder (TFA) was proposed by Aloke et al. [2] as a component in the construction of wave-pipelined ternary-digital systems. In this paper, K-map has been implemented with regards to "SUM," the suggested Ternary-Full-Adder's circuit. The complete TFA has been designed and optimized in Tanner EDA V.16 Enhancement-type standard process which is based on the BSIM4 model on TSMC 65nm CMOS technology at 27°C temperature and 1.0Volt is applied voltage line. The values of 0 Volt, 0.5Volt, and 1.0Volt are used to represent the ternary values "00", "01", and "02". Sharmila Devi and Bhanumathi [3] described how to create a typical MCML full adder using a unidirectional line of logic gates to 6 incoming signals for executing reversibility gates. The Tanner EDA software was used to design and simulate this arrangement. After analyzing the simulation data, the suggested result is 24, which have 60%, 66.66%, and 63.63% lessen than with the TSG oriented Full Adder, Fermi gate oriented Full Adder, and Feynman gate oriented Full Adder, systematically.

Manan et al. [4] described how to construct a mathematical representation of estimating the Power Delay Product for a Full Adder. Power Delay Product was estimated with a minimal RMSE of 3.63 percent using the developed mathematical model, In addition, how the mathematical model would be utilized to characterize the Power Delay Product of the Full Adder architecture was demonstrated, Furthermore, the mathematical representation enables us to assess optimal Full Adder design for distinct functioning situations, as well as the transistor sizes (to achieve the minimal Power Delay Product) for each operational surroundings. Akhter et al. [5] explained a low-power CMOS dynamic logic-based 1-bit full adder implemented. SPICE simulation was done by using the 180 nm CMOS operation technology. The simulation outputs proved that now the adder specified is more efficient than the techniques used in previous reference paper concepts of delay and Power Delay Product. In this paper designed full adder offers an improvement of 46% in Power Delay Product compared to the previous reference paper.

Harsh et al. [6] designed a GDI-focused full adder and investigated utilizing 0.25μm advanced technologies and Tanner EDA tool used for analysis. Even as developing configuration of the circuit, the parasitic effects are considered and delay, power, and EDP. Efficiency is measured by proposed design modeling. When it tried to compare to static CMOS technology, the GDI software operates quicker, has a 19% lower latency, takes up less space, and uses 94% less power. D-Flip flops use more electricity than T-Flip flops, according to Parveen and Tamil Selvi [7]. This report explains that T-Flip-flop of full adder employing multiphase Adiabatic Static Clocked Logic (2PASCL) requires less maintenance than Positive Feedback adiabatic logic (PFAL), but also that simulation research reveals that T-Flip-flop

employing 2 Phase Adiabatic Static Clocked Logic (2PASCL) requires very little power than T-Flip-flop incorporating Positive Feedback adiabatic logic (PFAL).

Hasan et al. [8] used GDI, TG, and C-CMOS circuitry to create a hybrid Full adder cell design. While implementing 65 nm architecture and a 1.2 V reference voltage having a 1 GHz frequency, Full Adder constructed indicated 70.29 ps and 4.48 W median consumption delays. The Power Delay Factor obtained was 314.9 aJ. The initial architecture, as well as operating individuals, has been enlarged up to 32 bits in this study. The architecture of Full Adder reported in this research is particularly allowable for large adder architecture is highly developed VLSI technologies, that according to simulation outcomes.

Murugan and Baulkani [9] created an adiabatic logic-based full adder (ALFA) employing adiabatic logic after determining that adiabatic logic-based full adders (ALFA) had the least source of energy consumption owing to evaporative cooling. While trying to compare with CMOS full adder, 16T PTL to TG full adder, 16T PTL to TG full adder, and 14T pass-transistor logic (PTL) with transmission gate (TG) full adder, the suggested ALFA cell in this paper reduce energy consumed by 89.37 percent, 90.93 percent, and 98.49 percent, significantly. Thus, it occupies 54.84% less space than with a 28T CMOS-based FA device.

As per Ali et al. [10] an MRL-based crossbar configuration is utilized for frame resistive crossbar array's volume fraction and flexibility aspect's structure combining, and it is incorporated on the top layer of CMOS. It is proven that 44.79% space is reduced after this methodology, and the Energy Delay measure was utilized for comparing.

Malti and Singh [11] introduced a 10T GDI fully adder and a 28T CMOS logic some of which were examined in terms of energy, lag, and size utilizing FinFETs 18nm architecture. After modeling, it was established that the 10T GDI adder outperforms the 28T CMOS logic in terms of lag, energy, and density of Area (due to a smaller number of a transistor). As a consequence, we can see that when we develop conventional circuits including FinFETs, the efficiency is excellent.

Inamul and Chaudhury [12] compared the performance of a traditional 1bit FA versus a hybrid 1bit FA. CMOS full adder and complementary pass logic (CPL) for traditional full adders, and CMOS logic and transmission gate (TG) logic for hybrid full adders. Results were noted for characteristics such as power pace, lag, and space in this article.

Riaz et al. [13] suggested that the Dadda Algorithm is introduced in this publication. The primary component for optimizing the Full adder is this algorithm. This approach results in a complete adder with minimal power dissipation and short propagation latency. The frequency of the multiplier utilized in the study is 3.83 GHz, and the operational capability is 184.3 Watts at 1 Volt applied voltage. In this work, a 4×4 multiplier is constructed utilizing a hybrid full adder and the Dadda algorithm to boost efficiency.

Kathirvelu and Xie [14] described the different types of full adder's performance like power, PDP, delay transistor counts are examined and it is observed that the proposed architecture in this paper will require less power consumption, less transistor area and propagation delay i.e., proposed FA is 68% better performance than Hybrid Pass Logic with Static CMOS full adder. Proposed adder design by using 8-bit array multiplier and compared its performance with CMOS conventional architecture.

Lei et al. [15] designed two full adders based on quantum dots, which is performing better than other designs with few cells, small areas, and a cheaper price. The proposed two full adders have many of the same qualities, but only the cell values are used differently. After Simulation, results proved that as per circuit size changes, described architecture is reliable and flexible because the I/O cells are not shared by other cells.

## 3. EXISTING SYSTEM

Numerous full adder cells are built with many logics and technology in the digital realm. Few of them are suitable for low-power applications, while others are suitable for high-speed applications. Some of them meet the minimum area requirements, but all cells must meet the minimum area requirement. Configuration does have its specific benefits and drawbacks. Depending on the application's needs, such full adders are being used. The Fig.2 illustrates a traditional CMOS Full Adder cell block diagram. Reversible Logic-based Full Adder cell block diagram is presented in Fig.3, Static Energy Recovery FA cell (SERF) block schematic is described in Fig.4, Gate Diffusion Input FA cellblock schematic is described in Fig.5, and other full adder cells have previously been developed. Because most digital computational circuits require FA, overall power consumption may be controlled by using a high-speed, low-power adder cell. As a result, the performance of a digital circuit is determined by the full adder cells employed in the architecture. In the full adder that can be seen in Fig.1, here are three primary inputs: A, B, and Carry in (Cin), as well as two outputs: Sum and Carry out (Cout).

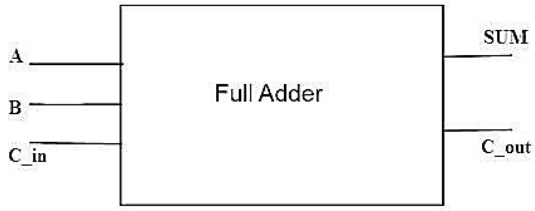


Fig.1. Basic building block of 1-bit full Adder cell

First and foremost, we will do a research study examination of the existing designs in this paper

### 3.1 CONVENTIONAL CMOS FULL ADDER

The Fig.2 depicts a 1-bit traditional CMOS complete adder cell. The design of a 1-bit CMOS FA cell necessitates the use of 28 transistors. Different reasoning styles may be examined from a variety of angles. The traditional CMOS full adder consumes a lot of power. Because of the large number of transistors employed and the longer propagation delay caused by the usage of five transistors in the input channel of circuits, the forward-path is crucial. The CMOS design approach is not appropriate for sophisticated gates that demand a lot of space and huge Fan-ins. As a result, while creating a logic function for a complete adder, a static logic style in CMOS technology must be carefully chosen.

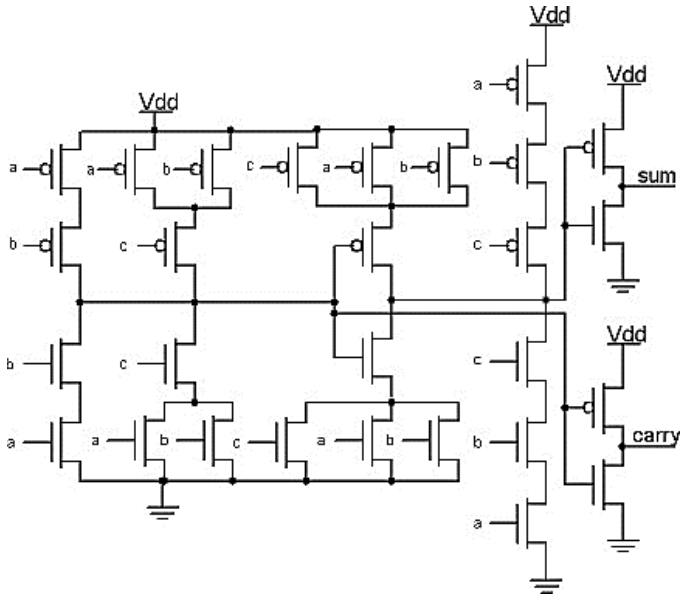


Fig.2. Conventional CMOS full adder cell

## 3.2 REVERSIBLE LOGIC BASED FULL ADDER

Basic Gates like OR, AND, XNOR, NOR, NAND are generally had various I/O pins so during information exchange operation, heat dissipated by every pin in traditional logic Circuits, hence this type of circuits not suitable for repeated operations, for saving minimum heat dissipation issue reversible logic-based circuits are used. For designing reversible Logic-based full adder normally reversible logic circuits like PERES, FEYNMAN, TSG, FREDKIN, and TOFFOLI ETC are used. In reversible logic circuit designing one to one mapping create between I/O. While some Output pins of these circuits are not required in operation so that is stored in the next stage, and those type of garbage output are stored in the quantum circuit by using Constant Inputs value 0's or 1's. Feynman gate based full adder is represented in the Fig.3.

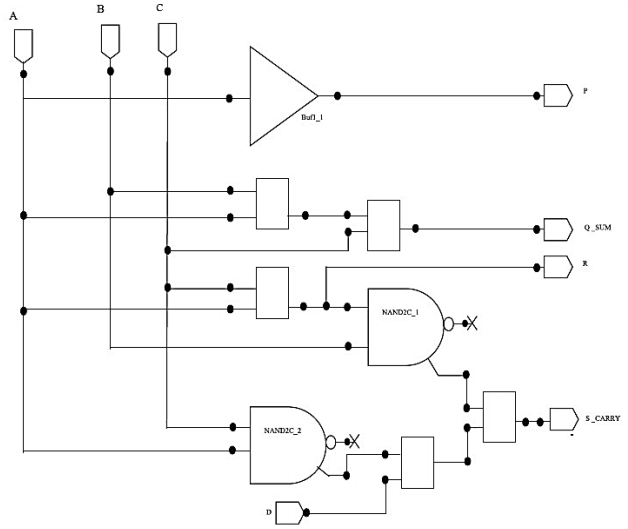


Fig.3. Schematic diagram for Feynman gate based full adder

## 3.3 STATIC ENERGY RECOVERY FULL ADDER

The design of SERF, or Static Energy Recovery FA, necessitates the use of ten transistors (10-T). A Full Adder can be used with either an X-OR or an X-NOR gate. Fig.4 displays an SER-FA implementation using X-OR gates. It employs two pipelined XOR gates to generate output (sum). SERF circuits of this type. The output signals (Sum and Cout) will not deliver a complete swing of voltages due to a threshold loss problem. The primary disadvantages of SERF include output logic swing, power dissipation, and latency, whereas the largest advantages of SERF are the small number of transistors required for chip design. The schematic diagram of SERF full adder is presented in the Fig.4.

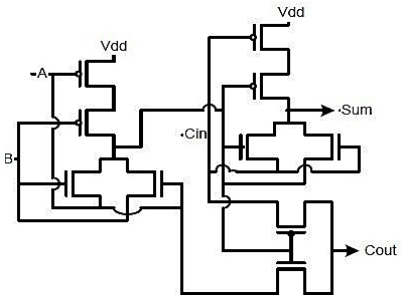


Fig.4. Schematic diagram SERF full adder

## 3.4 GATE DIFFUSION INPUT FULL ADDER

Nowadays GDI technique is more useful because this technique has many advantages along with this; there are a few drawbacks that can be rectified. In A GDI cell, there will be 3 inputs. One input G (which is the gate input for PMOS and NMOS) the main advantage of the GDI technique is that which has a large number of digital mathematical operations can be performed using this technique. Swing degradation is the main drawback of the GDI technique. For designing a full adder mainly XOR gate using GDI technique. The design of GDI full adder is shown in Fig.5.

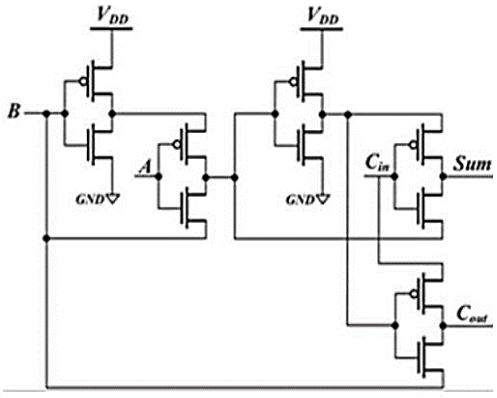


Fig.5. Schematic diagram GDI full adder

## 4. PROPOSED WORK

This survey investigation shows that how GDI technology may be used to improve the space of a CMOS full adder architecture. The comparative analysis part of the research displays the first most relevant outcomes. The area and power

efficiency of the CMOS full adder circuit is the key difficulty, according to the survey article. In the future, GDI-based full adder architecture is offered for enhanced area optimization and power consumption, which can overcome all of these concerns in digital circuits. In the future, our aim is to optimize the architectural area of CMOS full adder architectures as below presented in Fig.6 and in Fig.7 represents GDI Full Adder (8T).

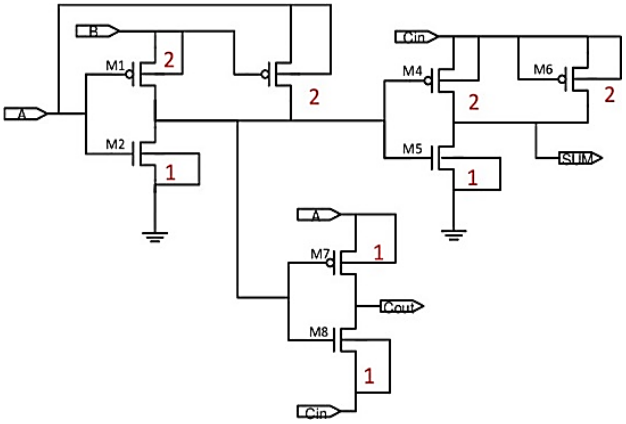


Fig.6. Architecture of Full Adder

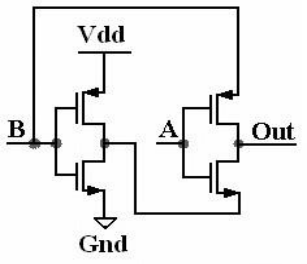


Fig.7. GDI Full Adder (8T)

## 5. CONCLUSION AND FUTURE SCOPE

According to the survey paper, the main challenges are the size and power efficiency of CMOS full adder circuits. For improved space optimization and power consumption, a GDI-based complete adder design will be introduced in the future, which will address all these issues in digital circuits and optimization of the architectural area of CMOS full adder designs. This survey investigates how GDI technology might help a CMOS full adder design to save space.

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