ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2021.0208

TRAP CHARGES INDUCED IMMUNITY IN DUAL METAL GATE (DMG) JUNCTIONLESS ACCUMULATION MODE (JAM) NANOWIRE FET (NWFET)

Deepak Kumar and Shamsher Singh
Department of Electronics and Communication Engineering, Maharshi Dayanand University, India

Abstract

In this brief, we have done a comparative study of Single Metal Gate Junctionless Accumulation Mode Nanowire FET (SMG-JAM-NWFET) and Dual Metal Gate Junctionless Accumulation Mode Nanowire FET (DMG-JAM-NWFET) for their immunity against the trap induced charges. It is so found that the DMG-JAM-NWFET poses much higher immunity against the trap charges as compared to the conventional SMG-JAM-NWFET in terms of much lower change in the potential, current, transconductance and output conductance. Aberration in other parameters like drain characteristics, Subthreshold Slope, capacitances and cut-off frequency has also been studied deeply. It is so found that the DMG-JAM-NWFET poses much higher immunity against the trap charges as compared to the conventional SMG-JAM-NWFET in terms of much lower change in the aforesaid parameters. It is so because of the impact ionization effect, the resistance to trap charges in DMG-JAM-NWFET is much higher than SMG-JAM-NWFET.

Keywords:

Immunity, Trap Charges, Junctionless Accumulation Mode, Drain Current, Transconductance Nanowire FET

1. INTRODUCTION

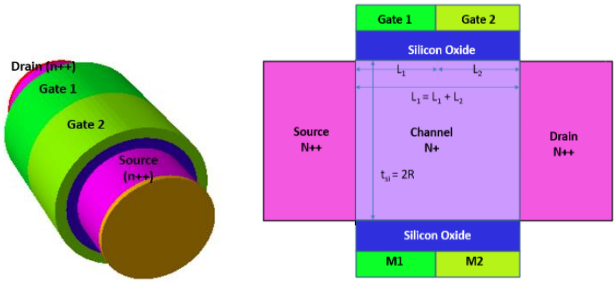
Increasing demand for compact new technologies drags the scaling of the device to new levels. The scaling of a MOS transistor is disturbed by tumbling device dimensions. In every technology generation, the dimensions of a MOS transistor is compact by 0.7 factor. Scaling results in reducing the dimensions of a conventional MOSFET, thus increasing the chip device density and functional capacity. Smaller MOSFETs are crammed into a lesser chip area, thus upsurging the chip device density and available capacity. But along with these advantages, the scaling in MOSFET creates critical performance warning factors like short channel effects (SCEs), fabrication difficulty, maintained switching speed and, considerable parasitic source/drain resistance [1],[2]. A new cohort of MOSFETs named multigate transistors has arisen. These structures are getting general because of their scaling competence, supervisory power over the channel region, and depleting the channel completely. Cylindrical Gate MOSFET is measured as utmost vital entrants for succeeding generation MOS devices among these multigate transistors as it abolishes the corner effects. The cylindrical design of MOSFET is used broadly due to its ultimate short-channel effect immunity, overturn floating body outcome, progressive carrier transport, supreme gate governance, and admirable CMOS compatibility [3]-[6] An inherent anomaly associated with CSG- MOSFET is conglomeration of highly tipped source- drain which can be easily nullified with Junctionless Field Effect Transistor (JLFET) [6].

JLFET poses a constant doping across source- channel drain ruling out the issue of rapid source- drain junction development. JFET also suffers from Carrier-Mobility-Degradation (CMD), smaller I_{ds} along with smaller g_m [7]. Junctionless Accumulation Mode (JAM) FET [8-9] is being researched to mitigate the shortcomings of JFET, which is done by keeping channel concentration of is subordinated with respect to source/drain (n+-n-n+). JAMFET poses improved performances than JFET.

The manuscript is summarized as: section 2 describes the device structure of DMG-JAM-NWFET. Section 3 gives out the results and their discussion on the efficacy of DMG-JAM-NWFET, for its immunity against the trap induced charges Finally, conclusion is compiled in section 4.

2. DEVICE-STRUCTURE

The 3-D structure of DMG-JAM-NWFET is pictured in Fig.1(a), and the 2-D design structure is in Fig.1(b). The design contains two gates; the Control gate – Gate1 and the Auxiliary gate-Gate2. The source and drain are very heavily doped (N++) with N type doping of $10^{19}/cm^{-3}$ and the channel is heavily doped (N+) with N-type doping of $10^{19}/cm^{-3}$. The various structural parameters of the projected devices are illustrated in Table.1. Silvaco device-simulator named ATLAS 3-D [15] arrayed to comprehend the device simulations. The Newton method and Gummel method are concurrently used for numerical calculations. The models used in simulation with their explanation are tabulated in Table.2.



(a) (b)

Fig.1. (a) Schematic view of 3D DMG-JAM-NWFET and (b) Schematic view of 2D DMG-JAM-NWFET

Table.1. Structural Parameters

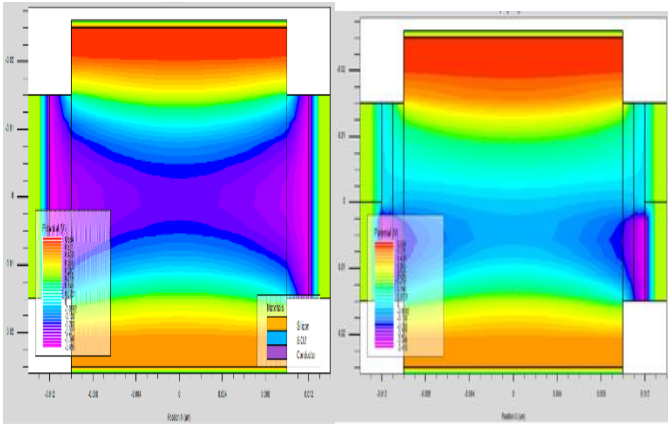
Device Parameters	Symbol	SMG-JAM-NWFET	DMG-JAM-NWFET	
Channel Length	L_{ch}	30 nm	30 nm	
Thickness of channel	t_{si}	20 nm	20 nm	
Outer/Inner depth of Gate oxide	t_{ox}	2nm	2nm	
Source/Drain Length	$L_{S/D}$	15nm	15nm	
Channel doping	N_A	10^{15} cm^{-3}	10^{15} cm^{-3}	
Gate Work function (eV)	Φ_m	5.2	Φ_{m1}	Φ_{m2}
			5.13	4.91

Table.2. Various Simulation Models

Physical model	description
Carrier to carrier scattering model (CCSMOB)	CCSMOB deployed for elevated concentrations of carrier and assist temperature upshot on mobility.
Schottky Read Hall (SRH)	SRH model deployed to cartel minority recombination possessions.
Boltzmann	The Boltzmann transport model is deployed for energy balance and works well for channel lengths greater than 40nm.
Concentration dependent model (CONMOB)	CONMOB model deployed to define numerous regions on a semiconductor.
Lombardi model (CVT)	CVT model deployed for non-planner device construction.

3. RESULT ANALYSIS

The contour plot of potential for V_{gs} = 0.5 V and V_{ds} = 0.5V with no-trap (q_f=0) charges with (a) SMG-JAM-NWFET (b) DMG-JAM-NWFET is shown in Fig.2. The Fig.2 depicts that in DMG-JAM-NWFET shows higher potential over SMG-JAM-NWFET. This elevation in the carrier concentration creates a further elevation in the mobility owing to an aberration of Fermi level toward the bandgap due to the higher work function towards the drain end in DMG-JAM-NWFET.

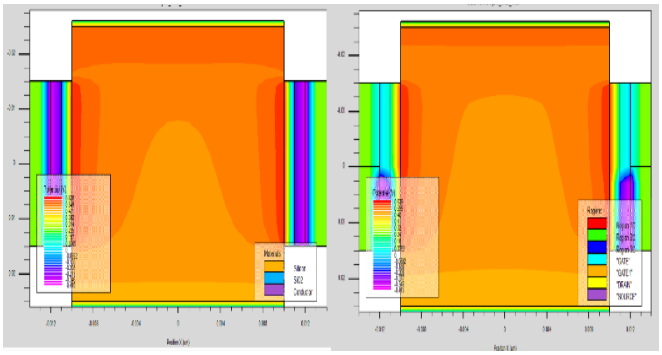


(a) SMG-JAM-NWFET (b) DMG-JAM-NWFET

Fig.2 Contour Plot of Potential for V_{gs} = 0.5V and V_{ds} = 0.5V with no trap charges

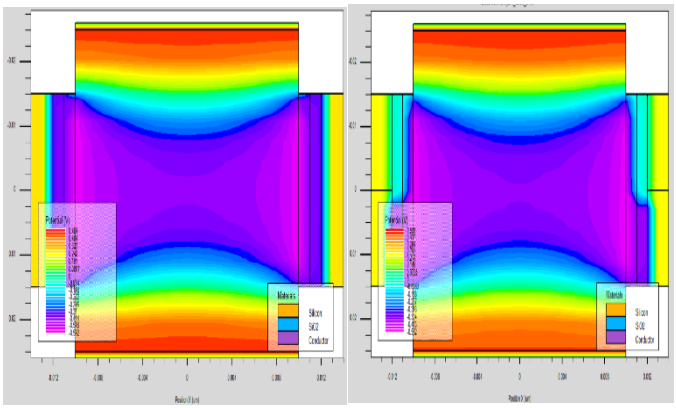
The contour plot of potential for V_{gs} = 0.5V and V_{ds} = 0.5V with positive trap charges (q_f = +1E^{12}) with (a) SMG-JAM-NWFET (b) DMG-JAM-NWFET is shown in Fig.3. It can be clearly seen from Fig.2 that in DMG-JAM-NWFET shows higher potential over SMG-JAM-NWFET. This elevation in the carrier concentration creates a further elevation in the mobility owing to an aberration of Fermi level toward the bandgap due to the higher work function towards the drain end in DMG-JAM-NWFET.

The contour plot of potential for V_{gs} = 0.5V and V_{ds} = 0.5V with negative trap charges (q_f = -1E^{12}) with (a) SMG-JAM-NWFET (b) DMG-JAM-NWFET is shown in Fig.4. It can be clearly seen from Fig.2 that in DMG-JAM-NWFET shows higher potential over SMG-JAM-NWFET. This elevation in the carrier concentration creates a further elevation in the mobility owing to an aberration of Fermi level toward the bandgap due to the higher work function towards the drain end in DMG-JAM-NWFET.



(a) SMG-JAM-NWFET (b) DMG-JAM-NWFET

Fig.3. Contour Plot of Potential for V_{gs} = 0.5 V and V_{ds} = 0.5V with Positive trap charges



(a) SMG-JAM-NWFET (b) DMG-JAM-NWFET

Fig.4 Contour Plot of Potential for V_{gs} = 0.5V and V_{ds} = 0.5V with q_f = -1E^{12}

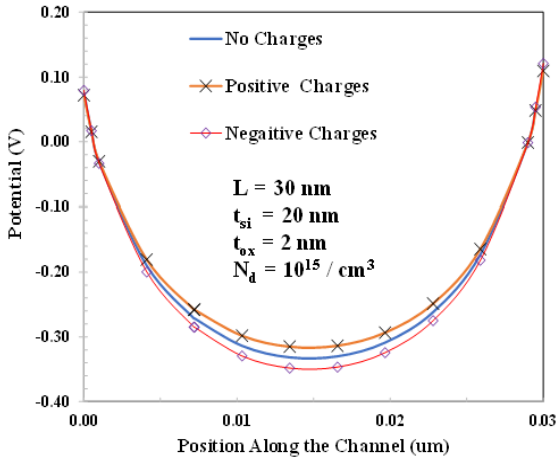


Fig.5(a). Trap Charges Impact on potential of SMG-JAM-NWFET

The Fig.5(a) and Fig.5(b) defines potential with position along the channel intended for Fig.5(a) SMG-JAM-NWFET and Fig.5(b) DMG-JAM-NWFET. As discussed in Fig.1, the impact

ionization is reduced in the DMG-JAM-NWFET over SMG-JAM-NWFET. This reduction in impact ionization (due to dual metal gate ($\Phi_{m1}>\Phi_{m2}$) in SMG-JAM-NWFET) further manifests a minimal change in potential on application of trap charges in DMG-JAM-NWFET over SMG-JAM-NWFET and henceforth posing immunity against the trap charges.

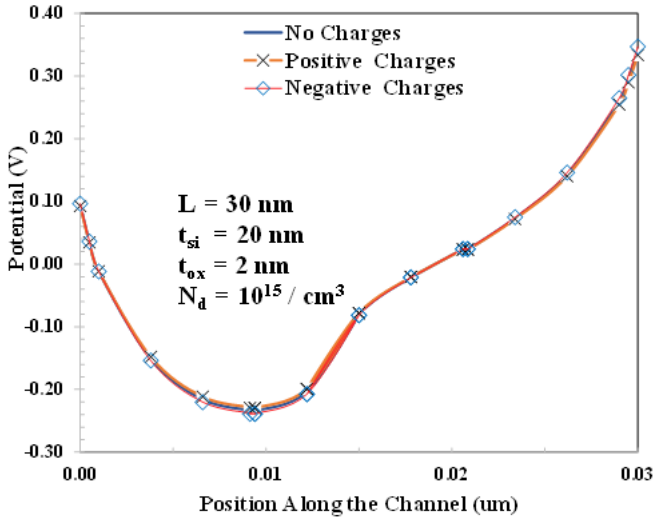


Fig.5(b). Trap Charges Impact on potential of DMG-JAM-NWFET

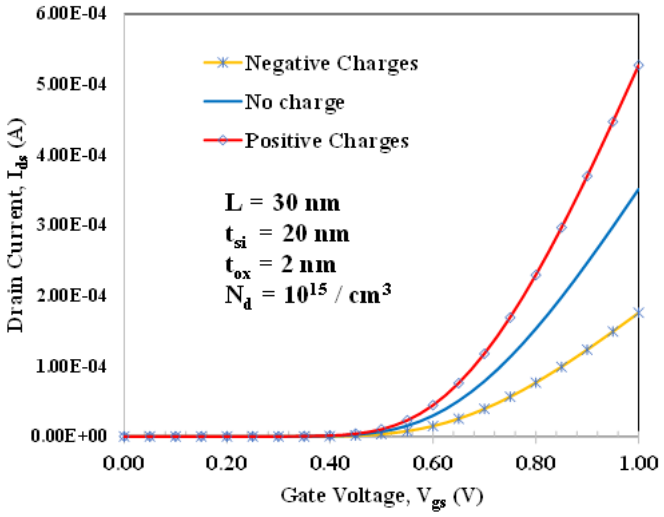


Fig.6 (a) Trap Charges Impact on I_{ds} of SMG-JAM-NWFET

The Fig.6 validates discrepancy of I_{ds} (drain current) regarding applied V_{gs} (gate voltage) for DMG-JAM-NWFET and SMG-JAM-NWFET. the impact ionization is reduced in the DMG-JAM-NWFET over SMG-JAM-NWFET. This reduction in impact ionization (due to dual metal gate ($\Phi_{m1}>\Phi_{m2}$) in SMG-JAM-NWFET) further manifests a minimal change in I_{ds} on application of trap charges in DMG-JAM-NWFET over SMG-JAM-NWFET and henceforth posing immunity against the trap charges.

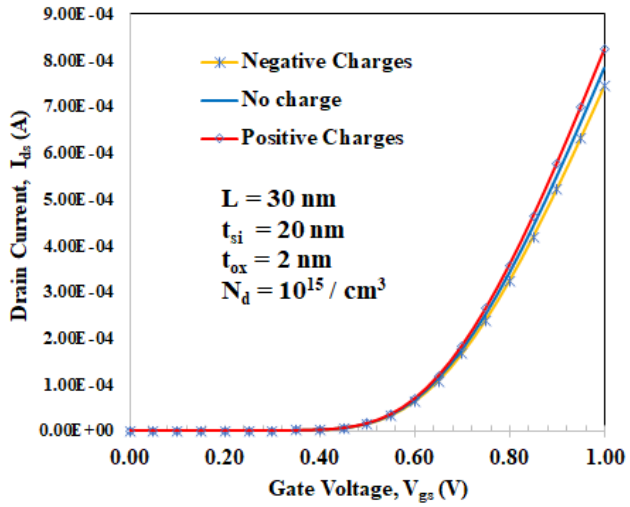


Fig.6 (b) Trap Charges Impact on I_{ds} of DMG-JAM-NWFET

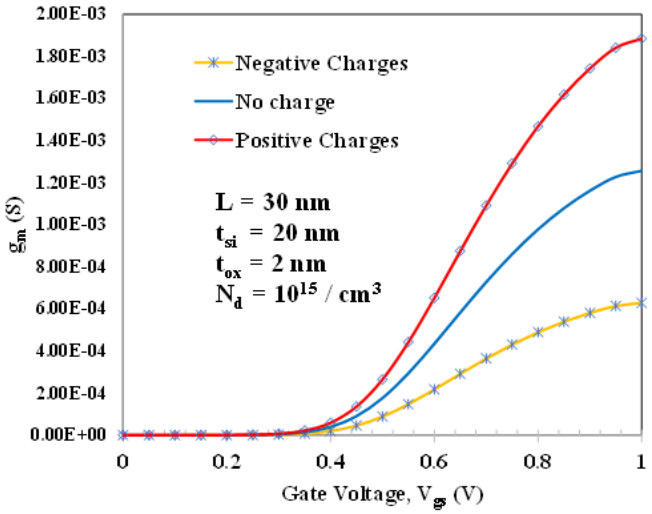


Fig.7(a). Trap Charges Impact on g_m of SMG-JAM-NWFET

The Fig.7(a) and Fig.7(b) displays transconductance, g_m, and gate voltage for both devices at V_{ds}=0.2V, showing that g_m is higher in ST-FET than Cylindrical SB-MOSFET. The high cut-off frequency of the device depends on its optimum bias point obtained from the device good transconductance value. Thus, the device is suitable for inflated frequency, inflated gain, and amplifier implementation. The transconductance is expressed as in [16]:

$$g_m = \left.\frac{\partial I_{ds}}{\partial I_{gs}}\right|_{V_{ds}} \quad (1)$$

The impact ionization is reduced in the DMG-JAM-NWFET over SMG-JAM-NWFET. This reduction in impact ionization (due to dual metal gate ($\Phi_{m1}>\Phi_{m2}$) in SMG-JAM-NWFET) further manifests a minimal change in potential on application of trap charges in DMG-JAM-NWFET over SMG-JAM-NWFET and henceforth posing immunity against the trap charges.

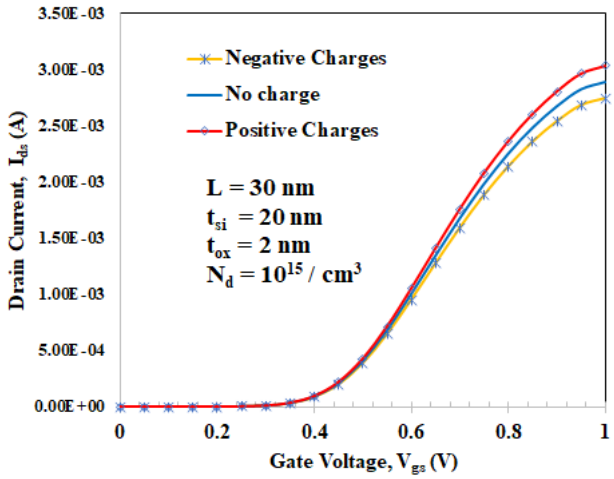


Fig.7 (b) Trap Charges Impact on g_m of DMG-JAM-NWFET

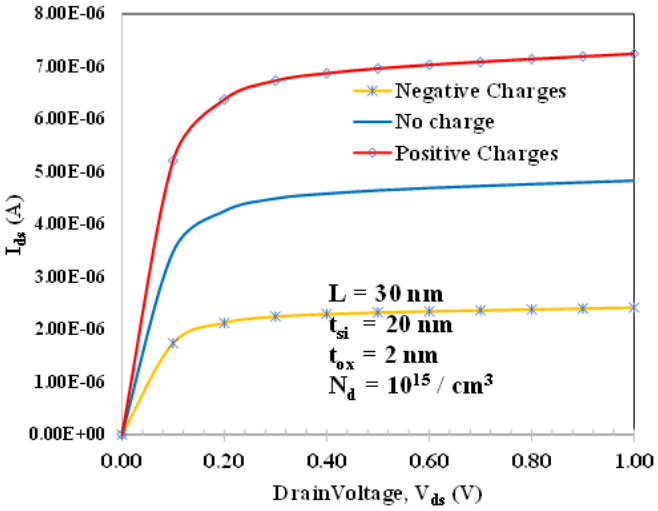


Fig.8(a). Trap Charges Impact on I_{ds} of SMG-JAM-NWFET

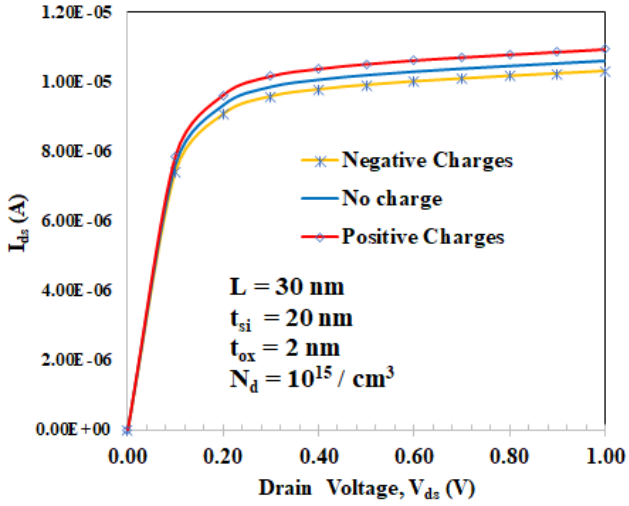


Fig.8(b). Trap Charges Impact on I_{ds} of DMG-JAM-NWFET

The Fig.8 shows characteristics intended for drain current (I_{ds}) along with drain voltage (V_{ds}) for both devices at V_{gs}=1.0V. The impact ionization is reduced in the DMG-JAM-NWFET over SMG-JAM-NWFET. This reduction in impact ionization (due to dual metal gate ($\Phi_{m1}>\Phi_{m2}$) in SMG-JAM-NWFET) further manifests a minimal change in potential on application of trap charges in DMG-JAM-NWFET over SMG-JAM-NWFET and henceforth posing immunity against the trap charges.

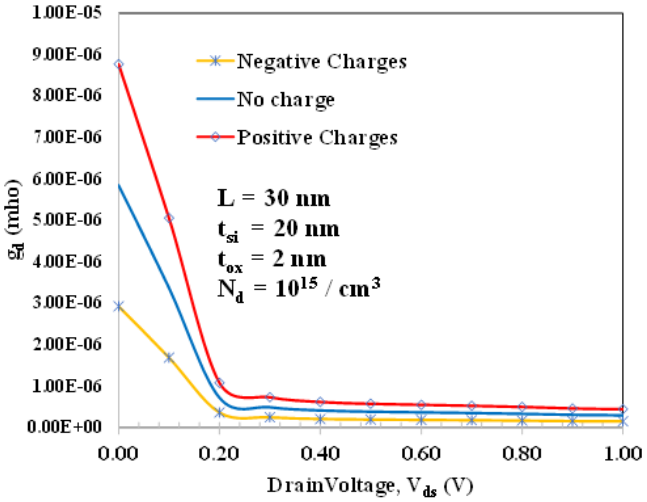


Fig.9(a) Trap Charges Impact on g_d of SMG-JAM-NWFET

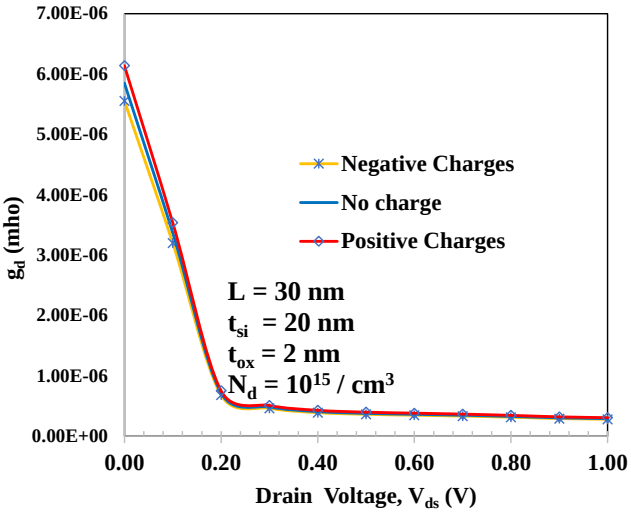


Fig.9(b). Trap Charges Impact on g_d of DMG-JAM-NWFET

The Fig.9 Displays output conductance (g_d) intended for both devices at V_{gs}= 1.0V. The device DMG-JAM-NWFET shows a higher value of output conductance when compared to the conventional cylindrical SMG-JAM-NWFET. The formula defines the output conductance of the device as [16]:

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}} \quad (2)$$

The impact ionization is reduced in the DMG-JAM-NWFET over SMG-JAM-NWFET. This reduction in impact ionization (due to dual metal gate ($\Phi_{m1}>\Phi_{m2}$) in SMG-JAM-NWFET) further manifests a minimal change in potential on application of trap charges in DMG-JAM-NWFET over SMG-JAM-NWFET and henceforth posing immunity against the trap charges.

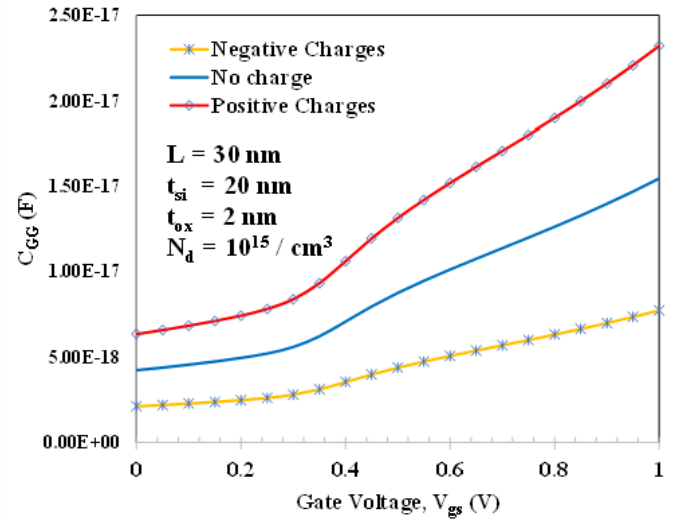


Fig.10(a). Trap Charges Impact on C_{GG} of SMG-JAM-NWFET

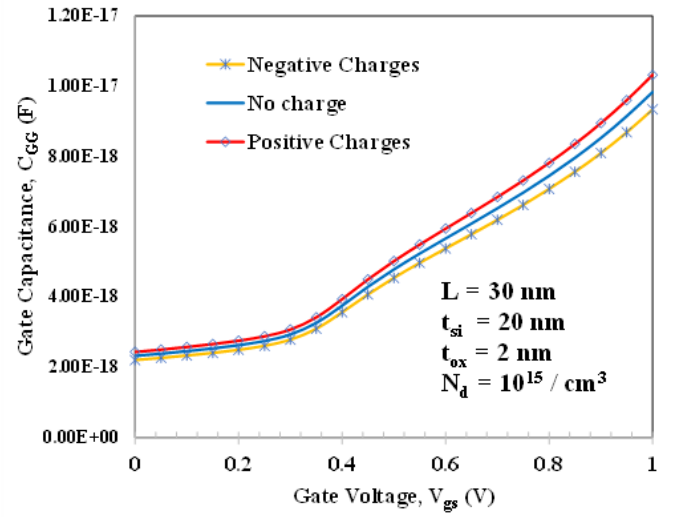


Fig.10(b). Trap Charges Impact on C_{GG} of DMG-JAM-NWFET

The Fig.10 Displays the capacitance (C_{GG}) intended for both devices at V_{gs}= 1.0V. The device DMG-JAM-NWFET shows a lower value of C_{GG} when compared to the conventional cylindrical SMG-JAM-NWFET. The impact ionization is reduced in the DMG-JAM-NWFET over SMG-JAM-NWFET. This reduction in impact ionization (due to dual metal gate ($\Phi_{m1}>\Phi_{m2}$) in SMG-JAM-NWFET) further manifests a minimal change in potential on application of trap charges in DMG-JAM-NWFET over SMG-JAM-NWFET and henceforth posing immunity against the trap charges.

The Fig.11 Displays cut off frequency (f_T) intended for both devices at V_{gs}= 1.0V. The device DMG-JAM-NWFET shows a higher value of f_T when compared to the conventional cylindrical SMG-JAM-NWFET. The impact ionization is reduced in the DMG-JAM-NWFET over SMG-JAM-NWFET. This reduction in impact ionization (due to dual metal gate ($\Phi_{m1}>\Phi_{m2}$) in SMG-JAM-NWFET) further manifests a minimal change in potential on application of trap charges in DMG-JAM-NWFET over SMG-JAM-NWFET and henceforth posing immunity against the trap charges.

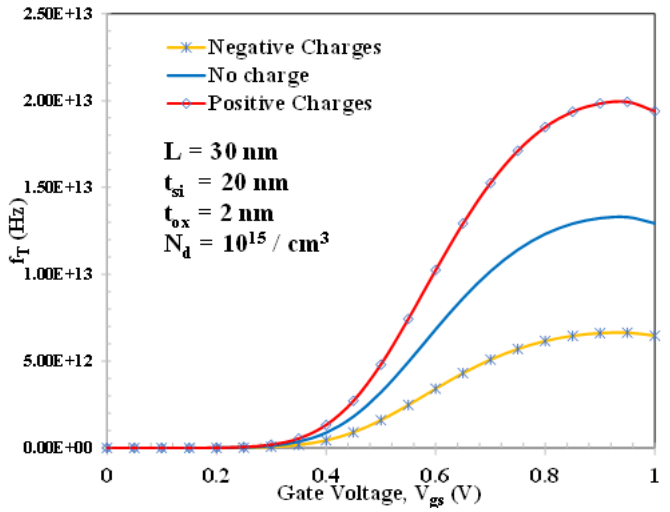


Fig.11(a). Trap Charges Impact on f_T of SMG-JAM-NWFET

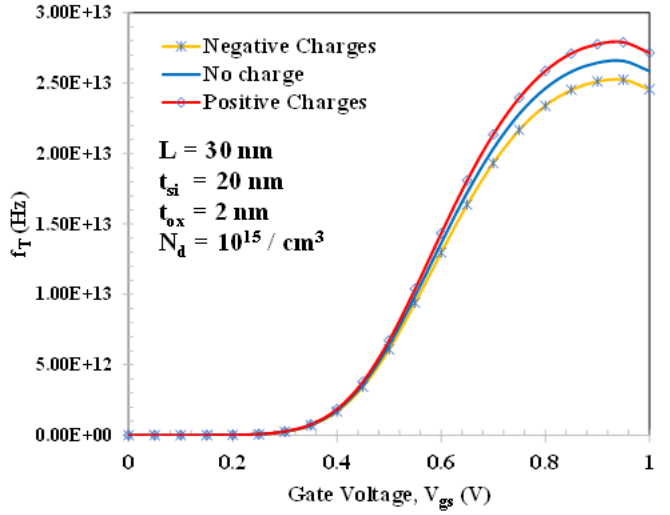


Fig.11(b). Trap Charges Impact on f_T of DMG-JAM-NWFET

The Fig.12 shows subthreshold slope (SS) for various devices. The subthreshold slope is the ratio of variation in gate voltage (V_{gs}) for a decade change in drain current (I_{ds}) and can be formulated as:

$$SS = \frac{\partial V_{gs}}{\partial \log_{10} I_{ds}} \quad (3)$$

SS can also be governed by the device capability to transfer from the off-state to the on-state. The ideal value of SS is 60mV/decade. The Fig. shows that DMG-JAM-NWFET has the closest to ideal value of the subthreshold slope along with the limited variation with charges. Owing to increased gate control over the channel offering high I_{on} and reduced I_{off}. The results also indicate that the device is highly immune to SCEs

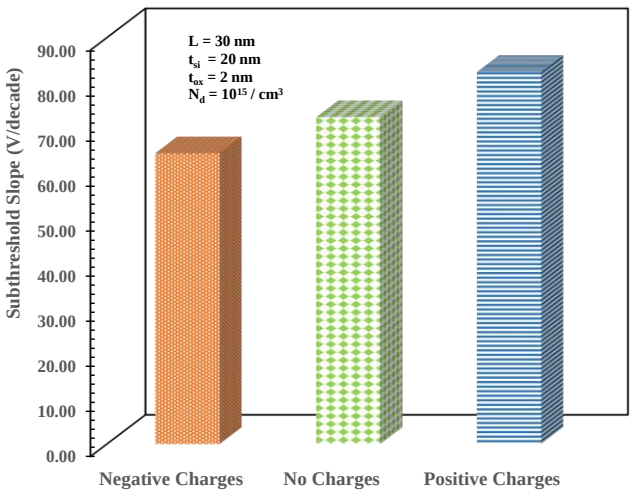


Fig.12(a). Trap Charges Impact on SS of SMG-JAM-NWFET

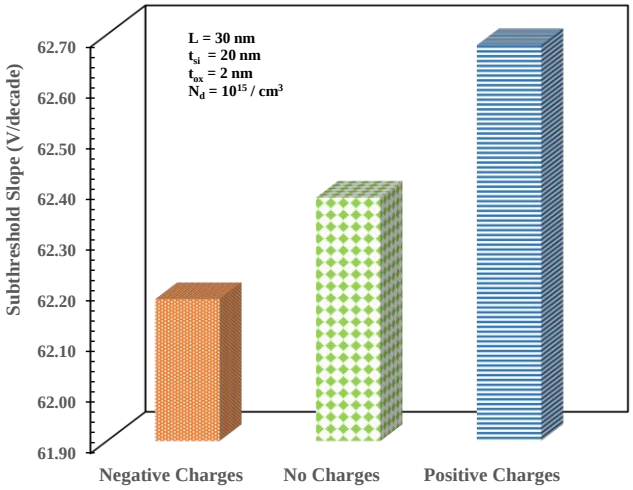


Fig.12(b). Trap Charges Impact on SS of DMG-JAM-NWFET

4. CONCLUSION

The Impact trap charges on the frequency response of Single Metal Gate Junctionless Accumulation Mode Nanowire FET (SMG-JAM-NWFET) and Dual Metal Gate Junctionless Accumulation Mode Nanowire FET (DMG-JAM-NWFET) for their immunity against the trap induced charges, which are precisely characterized by the measuring the aberration in parameters like drain characteristics, capacitances and cut-off frequency has also been studied deeply. It is so found that the DMG-JAM-NWFET poses much higher immunity against the trap charges as compared to the conventional SMG-JAM-NWFET in terms of much lower change in the aforesaid parameters. It is so because of the impact ionization effect, the resistance to trap charges in DMG-JAM-NWFET is much higher than SMG-JAM-NWFET.

REFERENCES

[1] G.E. Moore, "Cramming More Components onto Integrated Circuits", *Proceedings of the IEEE*, Vol. 86, pp. 82-85, 1998.

[2] F.D. Agostino and D. Quercia, "Introduction to VLSI Design (EECS 467), Short-Channel Effects in MOSFETs", Available at http://www0.cs.ucl.ac.uk/staff/ucacdxq/projects/vlsi/report.pdf, Accessed at 2000.

[3] R. Wang, J. Zhuge, R. Huang, Y. Tian, H. Xiao, L. Zhang, C. Li, X. Zhang and Y. Wang, "Analog/RF Performance of Si Nanowire MOSFETs and the Impact of Process Variation", *IEEE Transactions on Electron Devices*, Vol. 54, No. 6, pp. 1288-1294, 2007.

[4] L. Zhang, C. Ma, J. He, X. Lin and M. Chan, "Analytical Solution of Subthreshold Channel Potential of Gate Underlap Cylindrical Gate-all-Around MOSFET", *Solid-State Electronics*, Vol. 54, No. 8, pp. 806-808, 2010.

[5] H. Abd El Hamid, B. Iniguez and J.R. Guitart, "Analytical Model of the Threshold Voltage and Subthreshold Swing of undoped Cylindrical Gate-all-around-based MOSFETs", *IEEE Transactions on Electron Devices*, Vol. 54, No. 3, pp. 572-579, 2007.

[6] D. Kumar, S. Singh, "Analytical Model of Triple Metal Stack Engineered Pocket Dielectric Gate All Around (TMSEPDGAA) MOSFET for Improved Analog Applications", *Silicon*, Vol. 12, No. 2, pp. 1-15, 2021.

[7] Kyung Rok Kim, Byung-Gook Park and In Man Kang. "RF Performance and Small-Signal Parameter Extraction of Junctionless Silicon Nanowire MOSFETs", *IEEE Transactions on Electron Devices*, Vol. 58, No. 5, pp. 1388-1396, 2011.

[8] Tae Kyun, Dong Hyun Kim, Young Gwang Yoon, Jung Min Moon, Byeong Woon Hwang, Dong-Il Moon and Gi Seong Lee, "First Demonstration of Junctionless Accumulation-Mode Bulk FinFETs with Robust Junction Isolation", *IEEE Electron Device Letters*, Vol. 34, No. 12, pp. 1479-1481, 2013.

[9] Manoj Kumar, Subhasis Haldar, S.S. Deswal, Mridula Gupta and R.S. Gupta. "Analytical Modeling of Junctionless Accumulation Mode Cylindrical Surrounding Gate MOSFET (JAM-CSG)", *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, Vol. 29, No. 6, pp. 1036-1043, 2016.

[10] Anubha Goel, Sonam Rewari, Seema Verma and R.S. Gupta, "High-K Spacer Dual-Metal Gate Stack Underlap Junctionless Gate All Around (HK-DMGS-JGAA) MOSFET for High Frequency Applications", *Microsystem Technologies*, Vol. 26, pp. 1697-1705, 2020.

[11] Anubha Goel, Sonam Rewari, Seema Verma and R.S. Gupta, "Novel Dual-Metal Junctionless Nanotube Field-Effect Transistors for Improved Analog and Low-Noise Applications", *Journal of Electronic Materials*, Vol. 50, pp. 108-119, 2021.

[12] Anubha Goel, Sonam Rewari, Seema Verma and R.S. Gupta, "Physics-Based Analytic Modeling and Simulation of Gate-Induced Drain Leakage and Linearity Assessment in Dual-Metal Junctionless Accumulation Nano-Tube FET

(DM-JAM-TFET)", *Applied Physics A*, Vol. 126, pp. 1-14, 2020.

[13] Anubha Goel, Sonam Rewari, Seema Verma, S.S. Deswal and R.S. Gupta, "Dielectric Modulated Junctionless Biotube FET (DM-JL-BT-FET) Bio-Sensor", *IEEE Sensors*, Vol. 21, No. 15, pp. 16731-16743, 2021.

[14] Subhasis Haldar, Vandana Nath, S.S. Deswal and R.S. Gupta, "Numerical Modeling of Subthreshold Region of Junctionless Double Surrounding Gate MOSFET (JLDSG)", *Superlattices and Microstructures*, Vol. 90, pp. 8-19, 2016.

[15] Silvaco International, "Atlas User Manual: Device Simulator Software", Available at https://www.eng.buffalo.edu/~wie/silvaco/atlas_user_manual.pdf, Accessed at 2020.

[16] Anubha Goel, Sonam Rewari, Seema Verma and R.S. Gupta, "Shallow Extension Engineered Dual Material Surrounding Gate (SEE-DM-SG) MOSFET for Improved Gate Leakages, Analysis of Circuit and Noise Performance", *AEU-International Journal of Electronics and Communications*, Vol. 111, No. 1, pp. 1-18, 2019.