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SCHMITT-TRIGGER-BASED SINGLE-ENDED LOW-POWER 8T SRAM CELL

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Abstract

This article presents a new design of a single-ended low-power 8 transistor (8T) Static Random-Access Memory (SRAM) bitcell based on Schmitt-Trigger. The proposed cell is designed using a single bitline architecture that eradicates the conflict of design requirements on the access transistors. The proposed cell uses a Schmitt-Trigger based inverter which helps to increase the hold, read and write ability of the bitcell. A selective power gating transistor is also used which increases the write ability and also lowers the power consumption during write operations. Various parameters such as signal to noise margin (SNM), delay, read/write power and leakage power consumption of the proposed bit cell are compared against the conventional 6T SRAM bitcell and other bitcells. The simulations are performed using Cadence Virtuoso Software with a 180nm technology. The proposed bitcell has 1.3x larger area than the conventional bitcell. The results show that the proposed bitcell compares well against all the other considered bitcells and also is a better performer in many parameters.

Keywords:

Static Random-Access Memory (SRAM), Low-Power, Stability, Static Noise Margin (SNM), Schmitt-Trigger

1. INTRODUCTION

In the era of rapid development of portable devices, the battery life of the device is a major concern. As new devices like smartphones, smartwatches, biomedical instruments, etc. are being developed, energy efficient hardware is required. SRAM is widely used as the representative memory for digital systems. Therefore, the design of low-power SRAM bitcells have attracted a lot of research interest [1], [2]. CMOS scaling to deep sub-micron levels has led to threshold leakage, effects of short channel, leakage of gate dielectric, etc. So, leakage power has become a major source of power dissipation [3]. As per the ITRS statement, "the SRAM takes up the majority of the chip space" [4]. As most transistors in an SoC sit inside the SRAM unit so "power reduction in a single SRAM cell can have a huge impact on the overall power savings of the system" [5].

The standard 6T SRAM bit cell topology as shown in Fig.1 is the most widely used implementation of the cache memory in high-performance microprocessors and on-chip cache in SoCs. The structure of the bit cell consists of two identical CMOS inverters connected in a cross-coupled configuration forming a positive feedback loop formed by the two pull-up transistors P_1 and P_2, and two pull-down transistors N_1 and N_2. The transistors N_3 and N_4 are the NMOS transistors that connect the bitline BL and BLB to the cross-coupled inverters. These two transistors are also called access transistors.

Though the conventional SRAM cell has a simple architecture, "at scaled technology and reduced supply voltages, the stability of the circuit is deteriorated due to process, voltage, and temperature variations" [6] [7]. The SRAM array failures are due to:

- The process variations.
- On-Off current ratio (TON/TOFF) reduction [8], [9].

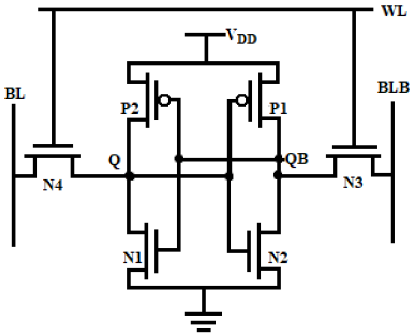


Fig.1. Schematic of conventional 6T SRAM bitcell

Read-disturb and conflicting read values affect the SRAM bitcells. Assuming that the cell stores bit '1' (Q=1), while reading the cell, the voltage division between the transistors N_3 and N_2 will result in an increase in voltage at node QB. If this increase in voltage is comparable to the threshold voltage of the inverter formed by the P_2-N_1 transistors, then bit flip will occur which will result in overwriting the data. This condition is known as read-disturb. So, "a careful design of the pull-up, pull-down, and access transistors is required" [10] [11].

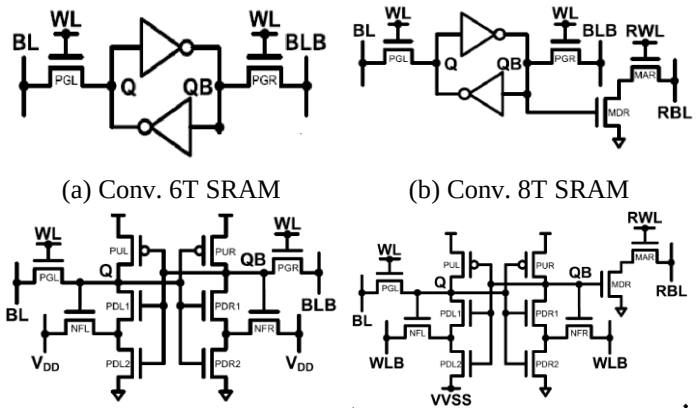
We propose a new Schmitt-Trigger based 8T SRAM bitcell in this article which occupies less area and has low energy consumption than other SRAM bitcells while simultaneously improving the read and write ability by incorporating the following features: (1) Reducing the area and energy consumption by using a single-ended bitline architecture, (2) improving write-ability and lower write power consumption using a selective power gating technique, and (3) improving the stability of the cell by using Schmitt-Trigger based inverter configuration.

The following is a breakdown of the paper structure: The bitcell topologies are briefly introduced in Section 2. The proposed 8T SRAM cell is introduced in Section 3, which covers its design and operation. Various design metrics of the proposed SRAM cell and the traditional SRAM cell are simulated and discussed in Section 4, and a comparison is made. Section 5 concludes the paper.

2. SRAM BITCELL TOPOLOGIES

As VDD scales, the conventional 6T SRAM bitcell suffers SNM degradation due to the read current disturbance. Also, the process variations caused due to low supply voltage degrade the read and write stability of the SRAM cell. To counter these challenges, various new SRAM topologies have been proposed such as 7-T, 8-T, 9-T, 10-T, and other multi-transistor cells [12]-[17]. These SRAM cells have drawbacks such as "requirements of the write-back scheme for bit-interleaving, large SRAM size,

or higher energy consumption". Chang et al. [18] have proposed a 10-T SRAM bit cell. However, the write circuit of this bitcell has series linked transistors which results in poor write-ability.



(a) Conv. 6T SRAM (b) Conv. 8T SRAM

(c) ST 10T SRAM (d) ST11T SRAM

Fig.2. SRAM bitcells used for comparison

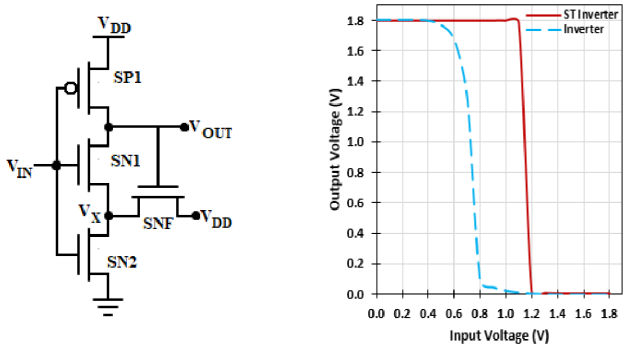
Single-ended SRAM topologies are advantageous for low-power applications. The use of a single-ended structure minimizes the leakage and switching power because, switching of the bitline in each read or write operation consumes considerable dynamic power. These types of SRAM architectures reduce the dynamic power of the cell by almost half. However, the write '1' SNM and delay of these cells is degraded at low supply voltages [2]. Various Schmitt-Trigger based SRAM cell designs have also been proposed to overcome the limitations of previous SRAM cell designs. Fig.2c shows the Schmitt-Trigger based 10T SRAM cell (ST10T) which uses Schmitt-trigger inverter instead of the conventional inverters which significantly improves the SNM of the cell. A single ended 11T SRAM cell (ST11T) using Schmitt Trigger inverters as proposed in [19] and shown in Fig.2d significantly improves the read and write static noise margin and consumes low power. Other Schmitt-Trigger based SRAM cell have similar features as proposed in [20], [21], [22].

3. PROPOSED SRAM BITCELL

3.1 SCHMITT-TRIGGER-BASED DESIGN

The traditional cross-coupled inverter design used in the conventional 6T SRAM cell is not very stable at low supply voltages. Hence, the power consumption of the cell is degraded due to the degraded inverter characteristics. A Schmitt-Trigger (ST) inverter as depicted in Fig.3(a) is utilized in the proposed design of the SRAM cell to alter the inverter characteristics.

The voltage transfer characteristics (VTC) of the standard inverter and the ST inverter is shown in Fig.3b. When the input voltage switches from logic level '0' to logic level '1', the feedback transistor SNF having the threshold voltage VTH, maintains the output level of the inverter at logic '1', raising the voltage at the node 'VX' where the voltage is now VDD - VTH. This will increase the minimum input voltage required at the input of the ST inverter for switching higher than VTH. This results in the switching characteristics of the ST inverter to be sharp as compared to the conventional CMOS inverter. Therefore, the ST inverter can be used to improve the performance of the SRAM cell.



(a) Schmitt Trigger (b) VTCs of inverter and ST inverter

Fig.3. ST inverter and VTC

3.2 PROPOSED 8T SRAM CELL

The Fig.4 depicts the schematic of the 8T SRAM bitcell that has been suggested. The proposed design of the SRAM cell consists of a Schmitt-Trigger (ST) inverter and a standard CMOS inverter in a cross-coupled configuration with a power gating transistor N1. The right-side inverter is an ST inverter that is formed by using the PMOS transistor P2 and NMOS transistors N3, N4, and N5. The left inverter is formed by the PMOS transistor P1 and NMOS transistor N2 with transistor N1 in between that functions as a power gating transistor. The feedback transistor N5 and the power gating transistor N1 are controlled by the signal WWL. The NMOS transistor N6 is used as an access transistor to read or write data from or into the cell using the bitline and is controlled by the control signal WL. A single bitline BL is used in the proposed cell to read or write the data controlled by the access transistor. The truth table for the operation of the proposed 8T SRAM cell is given in Table.1.

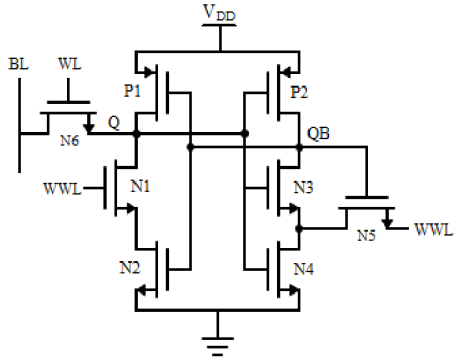


Fig.4. Schematic of proposed 8T SRAM cell

Table.1. Proposed 8T SRAM bitcell's truth table

Operation	WL	WWL	BL
Write '0'	1	1	0
Write '1'	1	0	1
Read	1	1	1
Hold	0	1	X

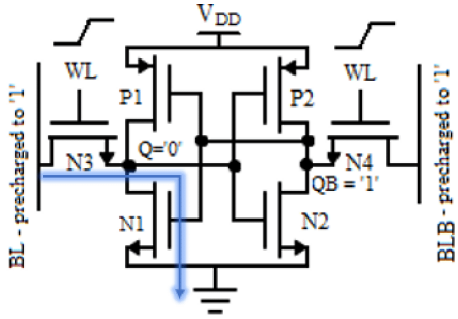
3.3 CELL OPERATION

3.3.1 Hold Operation:

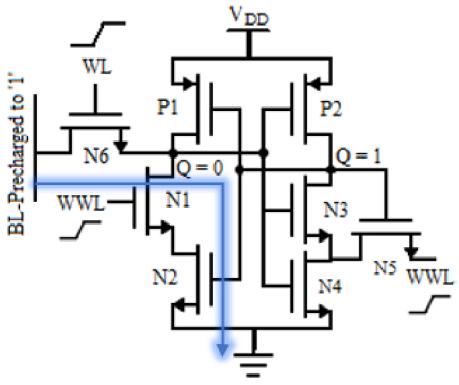
In the hold operation of the cell, the control signal WL is pulled to logic '0' or GND. This disables the access transistor N6 thus, disconnecting the bitline BL from the cell. The gating transistor N1 is also turned on in the hold mode by pulling the WWL signal to logic '1' or VDD. This makes the cell structure as the cross-coupled combination of standard CMOS and ST inverter. As the trip voltage of the inverter is higher than the standard inverter so, the data in the hold state is immune to the external disturbance when compared to the conventional 6T SRAM cell.

3.3.2 Read Operation:

During the read operation, the bitline BL is pre-charged to logic level '1' or V_{DD}. The signal *WWL* is already at the high logic level for the hold mode of the cell. The control signal *WL* is then pulled to logic '1' or V_{DD} which results in the access transistor N_6 to turn on and connects the bitline BL to the cell at node Q. Also, as WWL is high so the transistor N_1 is turned on, which connects the drain of the transistor P1 to the drain of the N_2 transistor thus forming a conventional inverter.



(a) Conventional 6T SRAM bitcell



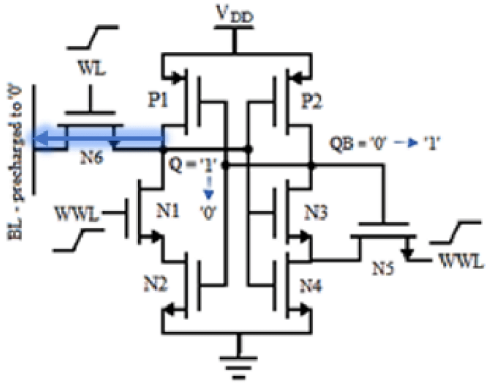
(b) Proposed 8T SRAM bitcell

Fig.5. Schematics for read operation

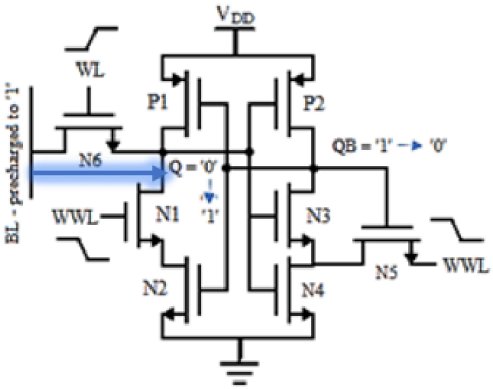
Now, depending on the logic value stored in the cell at node Q, the bitline BL is discharged or remains at the initial pre-charged level, i.e., the BL will only discharge if logic '0' (Q = 0) is stored at node Q. Otherwise, if logic '1' is stored, then the bitline will not be discharged. As compared to the conventional SRAM or other differential SRAM cells, when the storage node is disturbed by any read disturbance voltage or noise, the stored data cannot be flipped. This is because the proposed 8T SRAM cell uses a cross-coupled structure of the standard inverter and a Schmitt-Trigger (ST) inverter which results in a higher trip voltage as the strength of the N3 transistor is weakened by the voltage increased through the feedback transistors N5. Thus, the proposed SRAM cell is more robust and immune to read noise as compared to the conventional 6T SRAM cell. The read operations of the conventional and proposed SRAM cells are shown in Fig.5.

3.3.3 Write Operation:

The Fig.6 shows the schematics for the write '0' and write '1' operations for the proposed SRAM cell. The write operation control signals vary depending on whether the data to be written in the cell is logic '0' or logic '1'. During the write '0' operation, the bitline BL is pre-charged to logic '0' or discharged by connecting it to GND. Then the control signal WL is activated which turns on the access transistor N6 thereby connecting the bitline at the storage node Q. At the same time, the control signal WWL is also pulled high or to VDD and thus, the transistor N1 also turns on. As the data is being written in the cell, the voltage at node Q becomes low and the voltage at node QB becomes high. This results in the feedback transistor N5 for the ST inverter to turn on, which weakens the transistor N3 by increasing the voltage across it. This makes the trip voltage of the ST inverter higher than the standard inverter which results in better write ability when compared to the conventional 6T SRAM cell.



(a) Write '0' operation



(b) Write '1' operation

Fig.6. Write operation for the proposed 8T SRAM cell

During the write '1' operation, the bitline is pre-charged to logic '1' or VDD, and the access transistor is enabled by pulling the control signal WL to VDD. Also, the gating transistor N1 is disabled by pulling the WWL signal to GND. As the transistor N1 is disconnected from the GND node by turning off the WWL signal, so node Q is now power gated. As the voltage at node Q

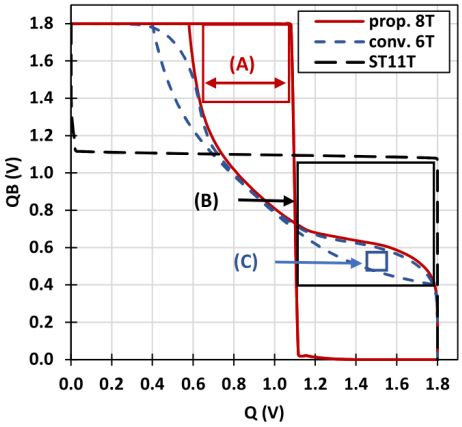
becomes high and the voltage at QB becomes low, the feedback transistor of the ST inverter is now turned off and the ST inverter functions just like the standard inverter. The write ability of the proposed cell, in this case, is expected to be similar to that of the conventional SRAM cell but, it will consume less power as compared to the conventional 6T SRAM cell because of the power gating scheme and stacking of transistors.

4. SIMULATION AND RESULTS

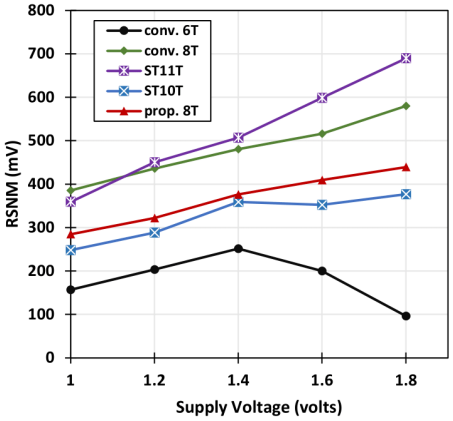
This section compares the proposed 8T SRAM bitcell against the conventional 6T SRAM cell and other previously described bitcells. The simulations were performed using Cadence Virtuoso Software using 180nm technology file. The various parameters such as Static Noise Margin (SNM) for reading, writing and hold operations, delay, power, energy consumption, leakage power, and area are commonly used to estimate the performance of the SRAM cells. A comparison of various performance parameters is presented in the following sub-sections.

4.1 READ STABILITY

The read stability of the SRAM bitcell is measured by Read Static Noise Margin or RSNM. The RSNM is defined as "the length of side of the largest square embedded inside the butterfly curves formed by the read voltage transfer characteristics of the two cross coupled inverters" [23]. The technique as described in [23] is used here to measure the RSNM at various supply voltages and process corners. The Fig.7(a) shows the butterfly curves for the proposed 8T SRAM cell along with the butterfly curves for the ST11T and conventional 6T SRAM cells. From the figure it can be noted that the conventional 6T SRAM cell has the least RSNM among all the bitcells because of rise in voltage at storage node during read operation. The ST11T SRAM cell which uses two ST inverters has the highest RSNM. The proposed 8T SRAM cell design uses one ST inverter in the right section which has a sharp VTC curve and a higher trip voltage as compared to the conventional 6T SRAM cell. Hence the proposed SRAM cell has a higher SNM as compared to the conventional 6T SRAM cell.



(a) Butterfly curves for RSNM measurement



(b) RSNM variation versus supply voltage

Fig.7. Read SNM measurement

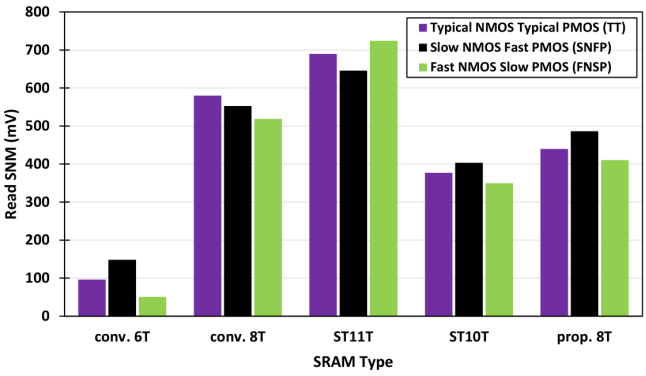
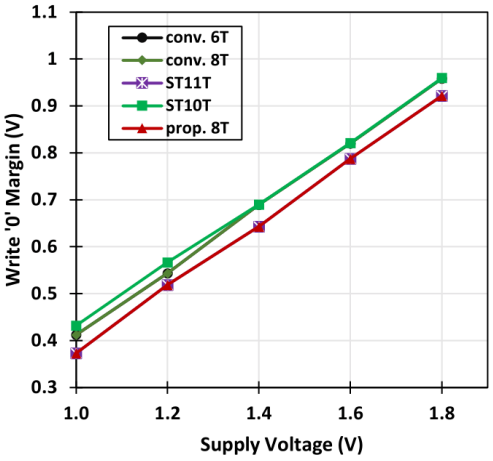


Fig.8. RSNM at different process corners

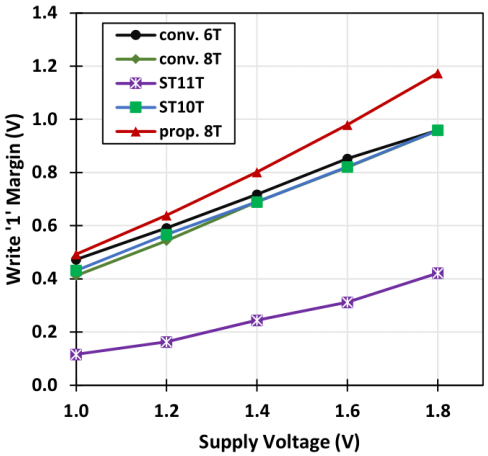
The Fig.7(b) shows the variation of the Read SNM at various supply voltages for different SRAM cells. It is observed that the proposed 8T SRAM cell has 4.56x larger RSNM as compared to the conventional 6T SRAM cell and 1.16x larger RSNM compared to the ST10T SRAM cell. Fig.8 shows the RSNM values calculated at process corners Typical PMOS Typical NMOS (TT), Fast NMOS Slow PMOS (FNSP) and Slow NMOS Fast PMOS (SNFP). From the data for the process corner it was observed that the proposed 8T SRAM cell has 4.56×, 3.28× and 8.11× larger RSNM at TT, SNFP, FNSP corners respectively when compared with the conventional 6T SRAM cell. The ST11T SRAM cell has the highest RSNM at all process corners because of the ST inverters in cross-coupled configuration and separate read circuitry.

4.2 WRITE ABILITY

The write ability of SRAM cell is measured using Write Margin which is defined as "the voltage difference between VDD and WL voltage at which the storage nodes Q and QB flip" as described in [24].



(a) Write ‘0’ margin

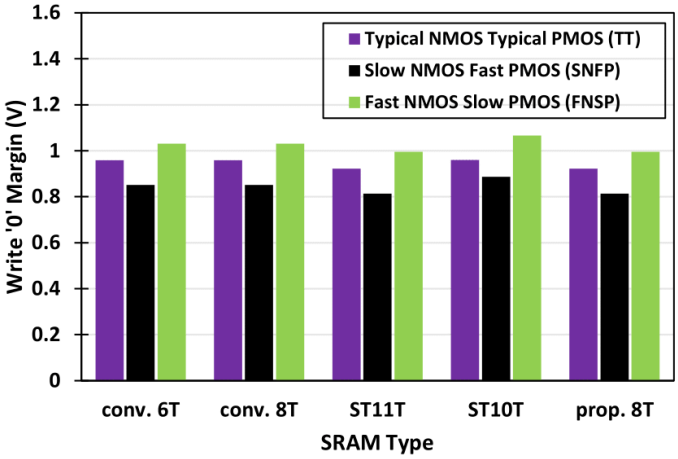


(b) Write ‘1’ margin

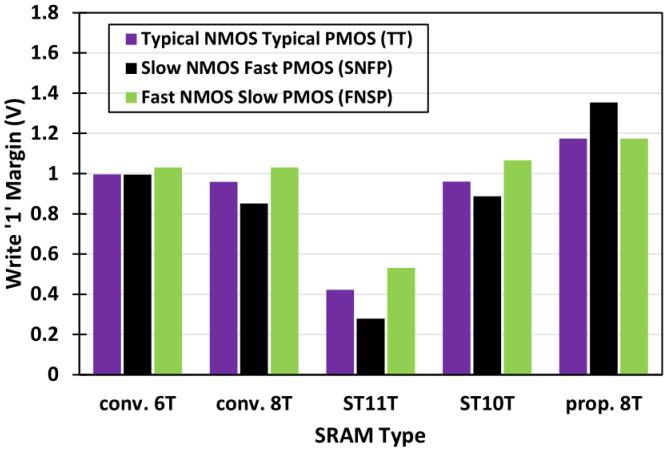
Fig.9. Write margin versus supply voltage

The write margin variation with supply voltage for write ‘0’ and write ‘1’ operations are shown in Fig.9(a) and Fig.9(b) respectively. The write ‘0’ SNM of the ST10T was found to be the highest among the bitcells compared. For the proposed 8T SRAM cell, the write ‘0’ SNM was similar to that of the conventional 6T, 8T and ST11T SRAM cells which is also clear from the overlapping of the write ‘0’ SNM lines in Fig.9(a). During the write ‘1’ operation, the proposed 8T SRAM cell showed the highest write margin value of 1.174V. The write ‘1’ margin of the proposed 8T SRAM cell was 1.2 times greater than the conventional 6T SRAM cell and 1.22 times better than the 8T and ST10T SRAM cells. The ST11T SRAM cell showed the lowest write ‘1’ margin value. The proposed 8T SRAM cell has almost 2.78 times greater write ‘1’ margin as compared to the ST11T SRAM cell.

The write margin variation for various process corners is shown in Fig.10. The values were obtained at TT, FNSP and SNFP process corners. Again, the write ‘1’ margin of the proposed 8T SRAM cell was highest and showed similar trend to the above discussion at all the process corners. As compared to the conventional 6T SRAM cell, the proposed 8T SRAM cell offers 1.2 times the write ‘1’ margin at all process corners at supply voltage of 1.8V.



(a) Write ‘0’ margin



(b) Write ‘1’ margin

Fig.10. Write margin at different process corners

4.3 HOLD STABILITY

The hold static noise margin (HSNM) quantifies the hold stability of SRAM bitcells in standby mode which is defined as the maximum value of the dc voltages the at the bitcell can tolerate without flipping the stored bit [25]. The ST inverter-based cells have higher HSNM compared to the conventional SRAM cells because of the higher trip voltage. However, RSNM is the parameter that actually describes the SRAM cell stability.

4.4 READ DELAY

The read delay for the differential bitline SRAM cells is defined as “the time duration between the activation of the control signal WL to the instant when 50mV voltage difference is developed between the bitlines BL and BLB” [26]. For single ended SRAM cell designs, the read delay is calculated as “the time interval between the assertion of WL and the discharging of bitline to VDD - 50mV” [19].

The read access time comparison for the proposed 8T SRAM cell and other bitcells with variation of supply voltage is shown in Fig.11. From the simulation results for the read operation, it is observed that the proposed 8T SRAM cell and the ST11T cells have almost the same read delay. The read delay of the conventional 8T SRAM cell and ST11T SRAM cells are same

because of the same read path used in both these cells. The read delay of the proposed 8T SRAM cell and ST11T SRAM cells is higher because of the single bitline operation. It is observed that the conventional 6T SRAM cell and ST10T SRAM cell offer the fastest read operation because of the differential bitline architecture and smaller bitline capacitance.

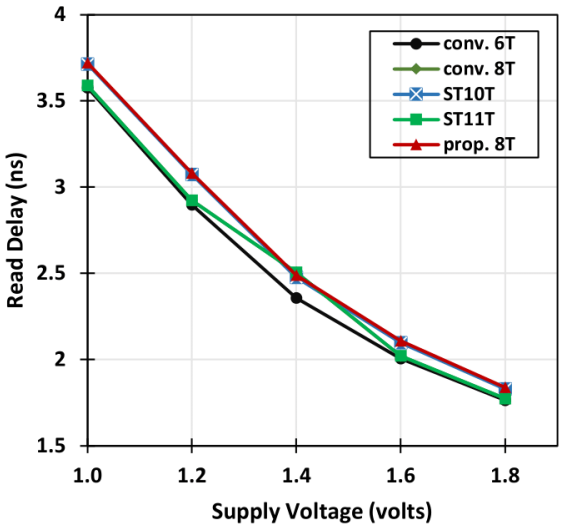
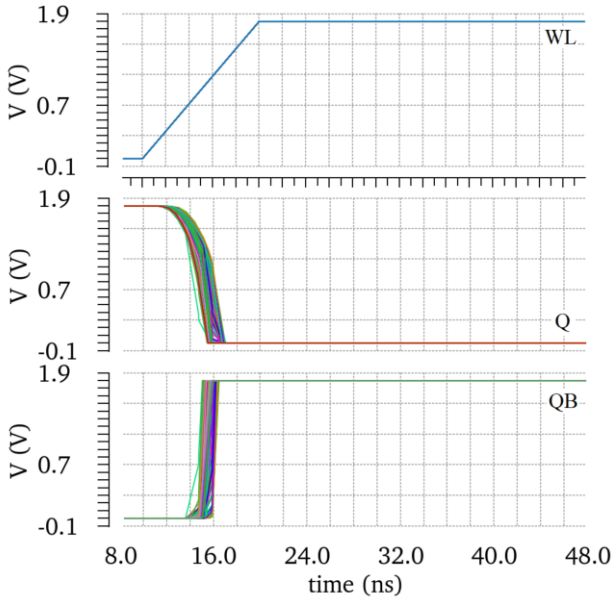


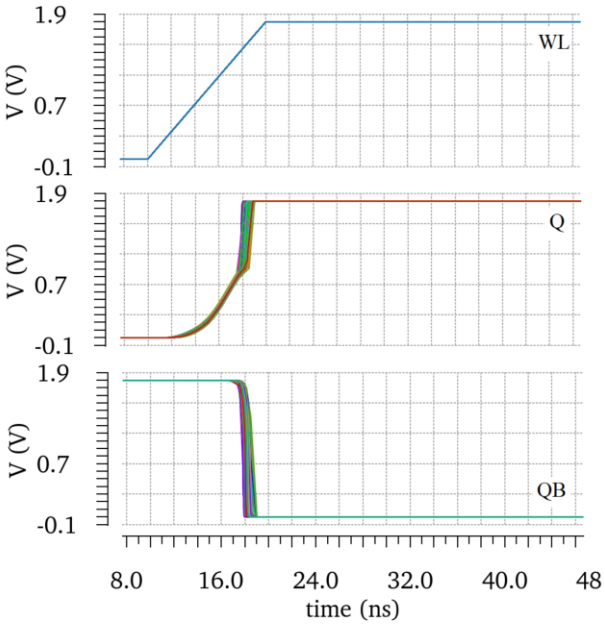
Fig.11. Read delay versus supply voltage

4.5 WRITE ACCESS TIME

The time interval between the activation of WL and the instant when the storage node Q (which was originally at a high voltage) drains to 10% of its initial voltage is known as the Write '0' delay. In a similar way, the write '1' delay is defined as the time duration between the activation of WL to the instant when the storage node which is initially at low voltage level charges to 90% of VDD value. For SRAM cells with differential bitlines, the write delays for write '0' as well as write '1' operations are the same but for single bitline SRAM cells, the write delay depends on the value that is being stored in the bitcell.



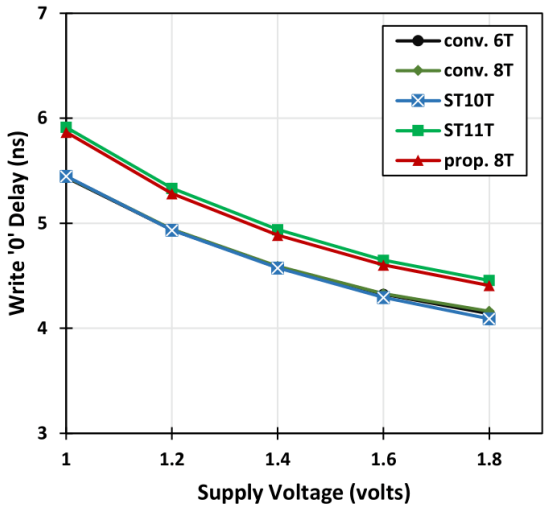
(a) Write '0'



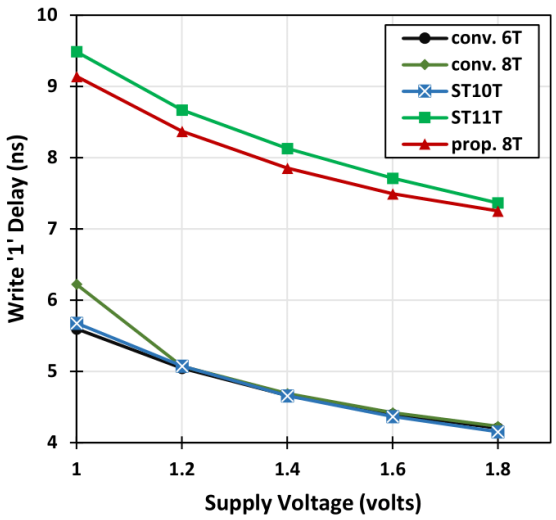
(b) Write '1'

Fig.12. MC simulation of write operation

The Fig.12 shows the Monte Carlo simulations for the write '1' and write '0' operations for 1000 samples each at TT, SNFP, FNSP process corners. Simulations show that the proposed 8T SRAM cell has no failed case and thus ensures a successful write operation at all the process corners considered. The MC simulations for write operations show a mean delay of 4.428ns for write '0' with standard deviation of 468.3ps and mean write '1' delay of 7.277ns with standard deviation of 177.1ps at nominal supply voltage of 1.8V across all process corners. The variation of the write delay with supply voltage is shown in Fig.13. The write '0' and write '1' delay for the differential bitline SRAM cells (conventional 6T, conventional 8T, ST10) was found similar while that of the ST11T and the proposed 8T SRAM cell was greater than the differential bitline cells as these cells use single bitline. The ST11T SRAM cell showed the highest write '1' delay while the delay of the proposed 8T SRAM cell was better than the ST11T SRAM cell because of the use of power gating transistor.



(a) Write '0'

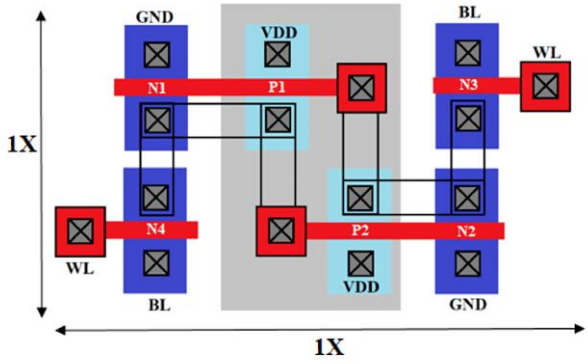


(b) Write '1'

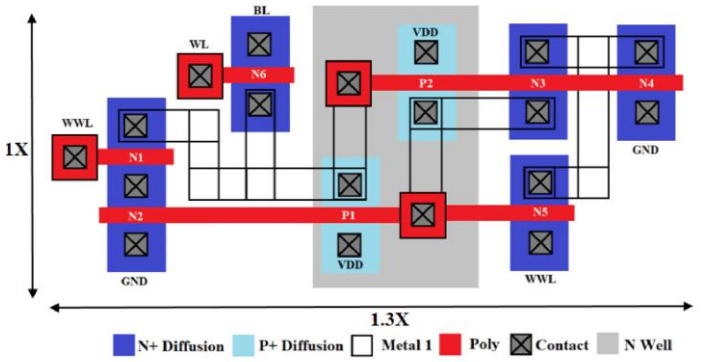
Fig.13. Write access time versus supply voltage

4.6 AREA

The layout of the proposed 8T SRAM cell using 180nm technology design rules is shown in Fig.14(a) and the layout of the conventional 6T SRAM cell is depicted in Fig.14(b). The cell area is normalized to that of the 6T SRAM cell. The proposed 8T SRAM cell layout shows an area overhead of 1.3× or 23% larger as compared to the traditional 6T SRAM cell. All the devices used in the design of the proposed cell and the conventional cell use the minimum dimensions for the technology file used. In the proposed SRAM cell, all the connections are made using metal 1 layer. The area comparison of other SRAM bit cells is shown in Fig.15 which shows that the proposed 8T SRAM bitcell occupies the least area when compared to other bitcells.



(a) Conventional 6T SRAM



(b) Proposed 8T SRAM

Fig.14. Layout of SRAM cells

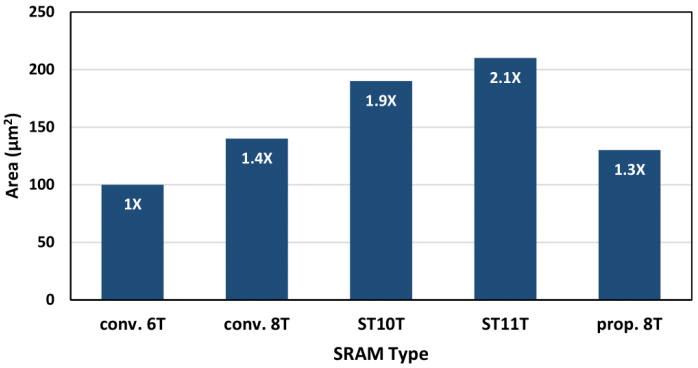
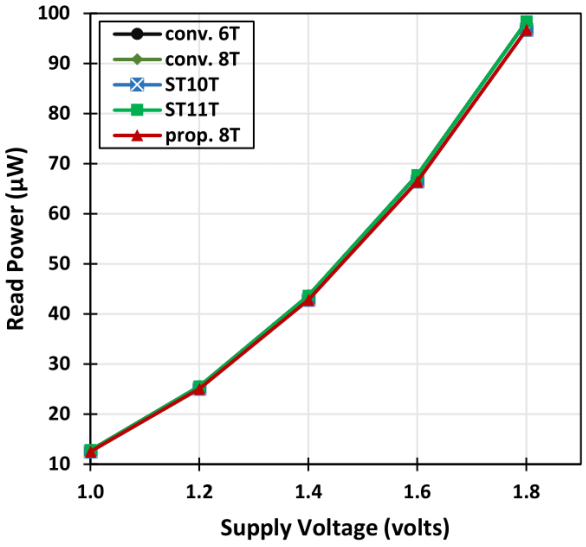


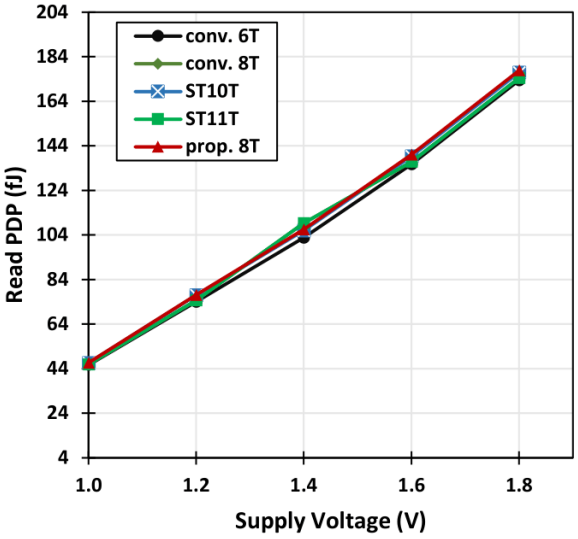
Fig.15. Area comparison

4.7 POWER CONSUMPTION

In comparison to the typical 6T SRAM bitcell, the proposed 8T SRAM bitcell employs a single bitline for read and write operations. When compared to the differential mode setup, this results in low power consumption while charging and discharging of the single bitline. "Half the number of write drivers as compared to differential bitline" [27] are required for the proposed 8T SRAM bitcell with a single-ended bitline architecture. Consequently, the power dissipation during the write operation is reduced when compared to the differential bitline design. Also, during the read operation, the bitline BL is discharged only if a logic '0' is stored in the bit cell and remains at its pre-charged value if logic '1' is stored in the bit cell. This behavior is contradictory to the differential bit cell mode where the bitline is always discharged. Thus, if we consider the equal probability of the read and write operations, the bitline in the proposed SRAM cell is discharged only 50% times as compared to the differential bitline mode in the conventional 6T SRAM cell.



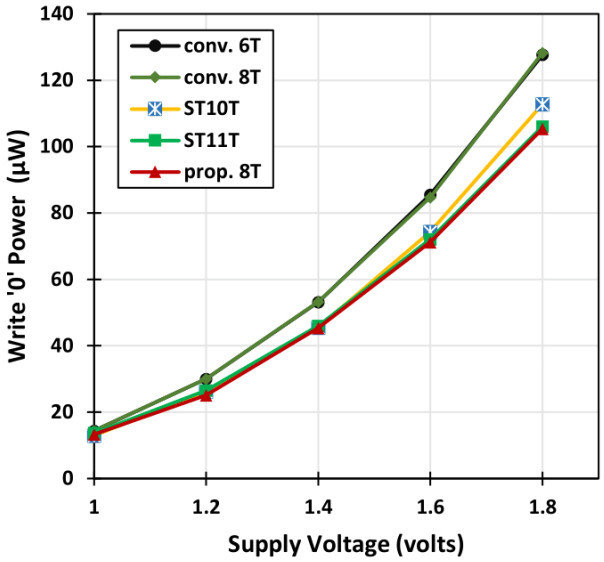
(a) Read '0' power



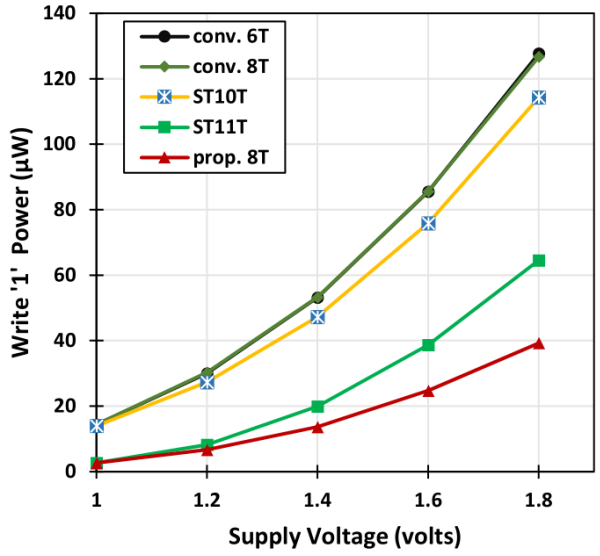
(b) Read PDP

Fig.16. Read power and PDP comparison

The read '0' power variation with the supply voltage is shown in Fig.16a. The results show that the power consumption during read '0' operation of all the considered SRAM cells is almost the same with the proposed 8T SRAM cell still consuming the least read power with an improvement of about 4% when compared to the conventional 6T SRAM cell while the conventional 8T and ST11T consume the maximum power because of the similar read path. Also, the proposed SRAM cell having single-ended design will only discharge the bitline only if a logic '0' is stored in the cell. Otherwise, it will maintain the pre-charged state and will only dissipate leakage power. While the differential bitline SRAM cells discharge the bitline in both logic '1' and logic '0' storage modes and so twice the power consumption. The read PDP comparison with supply voltage is shown in Fig.16b. The PDP values for all the SRAM cells overlap which shows a similar energy consumption for read operation.



(a) Write '0'

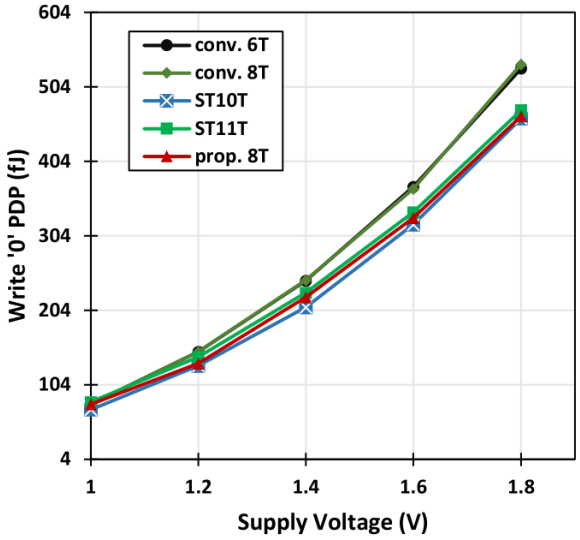


(b) Write '1'

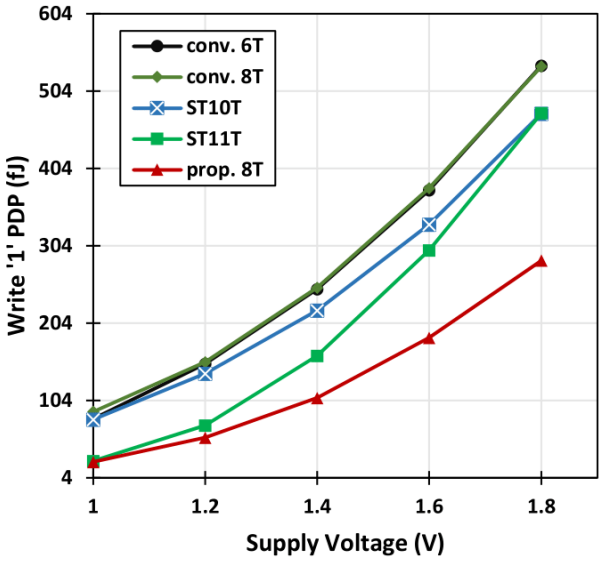
Fig.17. Write power consumption versus supply voltage

The power consumption versus supply voltage variation for write '0' and write '1' operations are shown in Fig.17a and Fig.17b respectively. It can be noted that the power consumed during write operations for the proposed 8T SRAM cell is the minimum among all the SRAM cells under consideration. It is observed that the conventional 6T and 8T SRAM cells which have the same mechanism for writing consume 1.22 times more power during write '0' operation when compared to the proposed 8T SRAM cell. The data also shows a similar power consumption between the proposed 8T and ST11T SRAM cells. From the simulation results of the write '1' operations, it is observed that the proposed 8T SRAM cell shows a significant reduction of power consumption. When compared with other SRAM cells, the conventional 6T and 8T SRAM cells consume 3.26 times, the ST10 consumes 2.91 times, and the ST11T consumes 1.64 times more power than the proposed 8T SRAM cell at supply voltage of 1.8V. This is attributed to the fact that the proposed 8T SRAM

cell uses one ST inverter and a power gated transistor in the write '1' path and hence the least power consumption.



(a) Write '0'



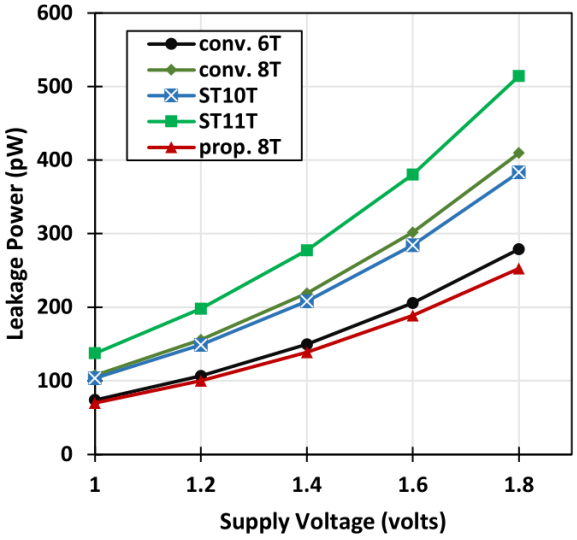
(b) Write '1'

Fig.18. Write PDP versus supply voltage

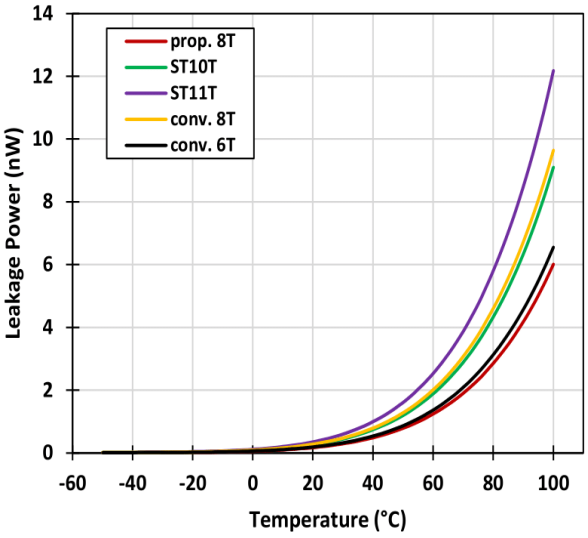
The PDP comparison at different supply voltages for the considered SRAM cells is shown in Fig.18 for write '0' and write '1' operations. The results show a significant improvement in PDP of the proposed 8T SRAM cell. The proposed 8T SRAM cell has the lowest PDP while the differential bitcells 6T and 8T have the highest PDP for all the supply voltage variations.

4.8 LEAKAGE POWER

Despite the fact that a large component of the SRAM bitcell is inactive for the majority of the time, there still is some leakage current flowing between the components of that idle section. The SRAM cells dissipate leakage power as a result of this leakage current [28]. "Sub-threshold leakage is the most dominant leakage current component among all the various leakage currents of the SRAM cell" [29]. In all the SRAM cells, the cross-coupled inverter is the main component that contributes to the leakage power dissipation. The proposed SRAM cell, during both hold '1' and hold '0' operations have multiple transistors in both left and right inverters connected in series which results in the transistor stacking.



(a) Leakage power versus supply voltage



(b) Leakage power versus temperature

Fig.19. Leakage power comparison

The leakage power variation of the SRAM cells with respect to supply voltage is shown in Fig.19a. From the figure it is observed that the leakage power of the proposed 8T SRAM cell is the lowest among all the SRAM cells considered. The conventional 6T SRAM cell consumes almost 10% more leakage power when compared to the proposed 8T SRAM cell. The leakage power of the ST11T SRAM cell is the highest among the cells compared which almost twice that of the proposed cell. The conventional 8T SRAM cell and the ST10T SRAM cells also consume 1.62x and 1.52x more power than the proposed 8T SRAM cell respectively. The variation of leakage power with respect to temperature is also shown in Fig.19b at nominal supply of 1.8V. Again, the proposed 8T SRAM cell has the lowest leakage power dissipation among all the SRAM cells considered

with ST11T having the highest leakage power consumption at all temperatures.

5. CONCLUSION

A novel single-ended 8T SRAM cell has been presented in this article. The proposed SRAM cell uses a Schmitt-Trigger-based inverter, a single bitline architecture, and the use of a power gating scheme. The proposed cell has significant improvement over the conventional 6T SRAM cell in terms of read and write stability. The proposed bitcell occupies 1.3× larger area than the conventional 6T SRAM cell. The process corner simulations along with Monte Carlo simulations show that the proposed bitcell performs better than the considered SRAM cells. The proposed SRAM cell has the least power consumption among all the considered bitcells. Rather being a poor performer in terms of write '1' delay, the proposed SRAM cell can be a good option where good SNM and low power is desired.

REFERENCES

[1] S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan and Y. Xie, "Low-Leakage Robust SRAM Cell Design for Sub-100nm Technologies", *Proceedings of Asia and South Pacific Conference on Design Automation*, pp. 1-8, 2005.

[2] B. Wang, T.Q. Nguyen, A.T. Do, J. Zhou, M. Je and T.T. Kim, "Design of an Ultra-low Voltage 9T SRAM With Equalized Bitline Leakage and CAM-Assisted Energy Efficiency Improvement", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 62, pp. 441-448, 2015.

[3] J.M. Rabaey, A. Chandrakasan and B. Nikolic, "*Digital Integrated Circuits- A Design Perspective*", 2nd Edition, Prentice Hall, 2004.

[4] International Technology Roadmap for Semiconductors, Available at http://www.itrs.net/links/2013/chapters/2013 Executive Summary.pdf, Accessed at 2013.

[5] S.R. Sridhara, M. DiRenzo, S. Lingam, S. Lee, R. Blazquez, J. Maxey, S. Ghanem, Y. Lee, R. Abdallah, P. Singh and M. Goe, "Microwatt Embedded Processor Platform for Medical System-on-Chip Applications", *Proceedings of International Symposium on VLSI Circuits*, 2010.

[6] S. Pal and A. Islam, "Variation Tolerant Differential 8T SRAM Cell for Ultralow Power Applications", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 35, pp. 549-558, 2016.

[7] A.J. Bhavnagarwala, X. Tang and J.D. Meindl, "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability", *IEEE Journal of Solid-State Circuits*, Vol. 36, pp. 658-665, 2001.

[8] T.H. Kim, J. Liu, J. Keane and C.H. Kim, "Circuit Techniques for Ultra-Low Power Subthreshold SRAMs", *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 1-14, 2008.

[9] F. Moradi, D. Wisland, Y. Berg, S. Aunet and T. V. Cao, "Process Variations in Sub-Threshold SRAM Cells in 65nm CMOS", *Proceedings of IEEE International Conference on Microelectronics*, pp. 121-129, 2010.

[10] Sung Mo Kang and Yousuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", 3rd Edition, Tata McGraw Hill, 2003.

[11] S. Ataei, J.E. Stine and M.R. Guthaus, "A 64 KB Differential Single-Port 12T SRAM Design with a Bit-Interleaving Scheme for Low-Voltage Operation in 32 nm SOI CMOS", *Proceedings of IEEE International Conference on Computer Design*, pp. 1-6, 2016.

[12] A. Venkatareddy, R. Sithara, Y.B.N. Kumar and M.H. Vasantha, "Characterization of a Novel Low Leakage Power and Area Efficient 7T SRAM Cell", *Proceedings of International Conference on VLSI Design*, pp. 337-343, 2016.

[13] B. Madiwalar and B.S. Kariyappa, "Single Bit-Line 7T SRAM Cell for Low Power and High SNM", Proceedings of International Multi-Conference on Automation, Computing, Communication, Control and Compressed Sensing, pp. 8881-8887, 2013.

[14] Z. Liu and V. Kursun, "Characterization of a Novel Nine-Transistor SRAM Cell", *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, Vol. 16, pp. 488-492, 2008.

[15] L. Chang, D.M. Fried, J. Hergenrother, J.W. Sleight, R.H. Dennard, R.K. Montoye, L. Sekaric, S. J. McNab, A.W. Topol, C.D. Adams, K.W. Guarini and W. Haensch, "Stable SRAM Cell Design for the 32 nm Node and Beyond", *Proceedings of International Conference on VLSI Technology*, pp. 1-14, 2005.

[16] S. Lin, Y.B. Kim and F. Lombardi, "Design and Analysis of a 32nm PVT tolerant CMOS SRAM Cell for Low Leakage and High Stability", *Integration*, Vol. 43, pp. 176-187, 2010.

[17] R.E. Aly and M.A. Bayoumi, "Low-Power Cache Design using 7T SRAM Cell", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 54, pp. 318-322, 2007.

[18] I.J. Chang, J. Kim, S.P. Park and K. Roy, "A 32 kb 10T Sub-Threshold SRAM Array with Bit-Interleaving and Differential Read Scheme in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, Vol. 44, pp. 650-658, 2009.

[19] S. Ahmad, M. K. Gupta, N. Alam and M. Hasan, "Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 24, pp. 2634-2642, 2016.

[20] C. Shalini and S. Rajendar, "CSI-SRAM: Design of CMOS Schmitt Trigger Inverter based SRAM Cell for Low Power Applications", *Proceedings of International Conference on Energy, Communication, Data Analytics and Soft Computing*, pp. 231-241, 2017.

[21] K. Cho, J. Park, T. W. Oh and S. Jung, "One-Sided Schmitt-Trigger-Based 9T SRAM Cell for Near-Threshold Operation", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 67, pp. 1551-1561, 2020.

[22] H. Rasekh, M. Sadeghi, A. Golmakani and M. Ali, "Design of Stable SRAM Cells based on Schmitt Trigger", *Proceedings of International Conference on Embedded Computing*, pp. 1-13, 2014.

[23] E. Seevinck, F.J. List and J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells", *IEEE Journal of Solid-State Circuits*, Vol. 22, pp. 748-754, 1987.

[24] H. Qiu, T. Mizutani, T. Saraya and T. Hiramoto, "Comparison and Statistical Analysis of Four Write Stability Metrics in Bulk CMOS Static Random Access Memory Cells", *Japanese Journal of Applied Physics*, Vol. 54, No. 2, pp. 4-9, 2015.

[25] E. Grossar, M. Stucchi, K. Maex and W. Dehaene, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies", *IEEE Journal of Solid-State Circuits*, Vol. 41, pp. 2577-2588, 2006.

[26] J.P. Kulkarni, K. Kim and K. Roy, "A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM", *IEEE Journal of Solid-State Circuits*, Vol. 42, pp. 2303-2313, 2007.

[27] G. Pasandi and S. M. Fakhraie, "A 256-kb 9T Near-Threshold SRAM With 1K Cells per Bitline and Enhanced Write and Read Operations", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, pp. 2438-2446, 2015.

[28] S. Akashe, S. Bhushan and S. Sharma, "Modeling and Simulation of High-Level Leakage Power Reduction Techniques for 7T SRAM Cell Design", *AIP Conference Proceedings*, Vol. 1476, pp. 35-41, 2012.

[29] S.R. Mansore, R.S. Gamad and D.K. Mishra, "A Single-Ended Read Decoupled 9T SRAM Cell for Low Power Applications", *Proceedings of IEEE International Symposium on Nanoelectronic and Information Systems*, pp. 1-12, 2017.