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COMPARATIVE ANALYSIS OF DIVERSE CARRIER TRANSPORTS IN MULTIGATE MOSFETS UNDER DIFFERENT CHANNEL LENGTH REGIMES

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Abstract

Multi-gate MOSFETs have successfully enabled the extension of CMOS technology scaling in the nanoscale regime. Suppression of short channel effects (SCEs) and carrier transport enhancement are the two prime factors that matter the most for the improvements in digital CMOS technology. Multi-gate transport leads to suppression of SCEs and mobility improvement leads to carrier transport enhancement. Continuous scaling of device channel length in the nanoscale regime invites for the inclusion of scattering theory physics. The proposed work discusses the diverse carrier transport mechanisms occurring in Multi-gate MOSFETs in different channel length regimes. Further, a comparative analysis of carrier transport in long, short and ultra-short channel Multi-gate devices is done. The work also discusses the validity of the transport models and their scaling restrictions in different regimes. The simulation results demonstrate physical accuracy and continuity of the proposed models in the respective channel length regimes.

Keywords:

Diffusion, Quasi-Ballistic Transport, Scaling, Carrier Scattering, Multi-Gate MOSFETs

1. INTRODUCTION

In the recent years, multi-gate MOSFETs have effectively replaced bulk MOSFETs in digital CMOS design due to their excellent scaling abilities in the nanoscale regime and reduction in short channel effects [1]. Multiple gate MOSFETs exhibit near ideal sub-threshold swing and a higher transconductance [2]. In MOSFETs, as the effective channel length L scales down from micron to nanoscale, the associated carrier transport physics changes [3], [4].

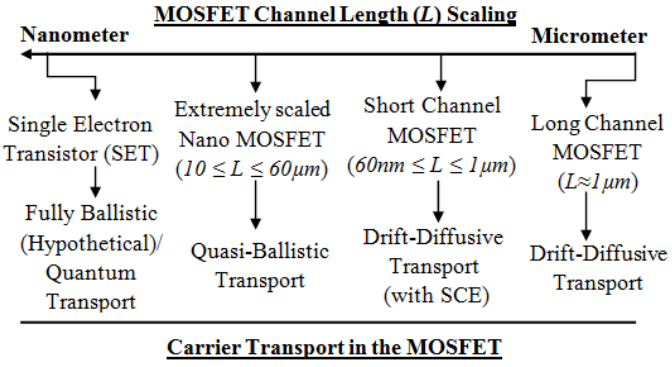

Fig.1. Different carrier transports in MOSFETs when channel length is scaled from micron to nanoscale regime

The Fig.1 illustrates the occurrence of diverse carrier transport mechanisms in different channel length regimes. In a long channel MOSFET (where $L \approx 1\mu m$), the carrier transport is completely drift-diffusive [5] [6]. As the device undergoes scaling, short channel effects (SCE) begin to affect the device performance. In such a case, the SCEs must be included in the drift-diffusion model equations. In a long channel device, the maximum drain current is limited by pinch-off, while in a short channel device it is first the velocity saturation and later the source injection velocity that limits the drain current [7]. In rigorously scaled nano devices, the carrier transport becomes quasi-ballistic [8]. The magnitude of quasi-ballistic nature is determined through the physics of scattering theory [9]. Under ideal conditions where the carrier scattering is ignored, the transport becomes fully ballistic [10], which is however a hypothetical case. In the extreme thin layered structures, quantum transport needs to be included appropriately.

Over the recent years, numerous multi-gate MOSFET models have been proposed, that describe the device physics. A Double Gate (DG) MOSFET shown in Fig.2 is the simplest variant amongst the family of various multi-gate structures proposed in literature [11]. Taur et al. [12]-[15] have proposed robust analytical models applicable for symmetric and asymmetric DG MOSFETs.

A DG MOSFET exhibits volume inversion that is found to aid in high speed digital design. The compact models proposed in [11]-[16] capture volume inversion effectively; however these models need to include short channel effects. As the channel length reduces from micron to sub-micron range, the drain current is limited by velocity saturation. The model proposed in [17] provides an analytical solution that includes SCEs. A complete velocity saturated DG model is given in [18], that gives explicit solutions. Natori [19] has proposed a ballistic transport model applicable for nanoscale MOSFETs for ideal case. However, current state-of-art devices exhibit quasi-ballistic nature. Few quasi-ballistic models [20]-[25] have been proposed in the recent past, which accurately predict the drain current behaviour at nanoscale. Murnal et al. [23]-[25] have recently proposed a nanoscale DG MOSFET model that accurately describes the quasi-ballistic transport by appropriately including scattering physics. Although such models have been proposed in the recent past, very less work has been done in terms of comparative analysis describing the validity and diverse physics. The proposed work qualitatively describes and compares the diverse transport mechanisms occurring in double gate MOSFETs in different channel length regimes. Since, a DG MOSFET is the simplest form of multi-gate MOSFET, the proposed work focuses on this device structure henceforth.

The outline of paper is given below: section 2 qualitatively describes the physical analysis and mathematical background of the proposed work. Further, the physical accuracy of the proposed work [24]-[25] is highlighted and compared with velocity saturation model [18] with proper illustrations and justifications.

Section 3 illustrates the model results obtained for the proposed work. Finally, the work is concluded in Section 4.

2. MODEL DESCRIPTION

This section proposes two DG MOSFET models that describe the diverse carrier transport mechanisms which occur when the channel length is scaled from micron to nanoscale. The first model proposed in sub-section 2.1 is a complete velocity saturated compact DG model [18] that is valid for long-to-short channel regime. This model is based on drift-diffusive transport formalism that further includes the short channel effects appropriately. The second model proposed in sub-section 2.2 is purely a nanoscale DG MOSFET model that is based on quasi-ballistic transport [23] [24]. Both analytical models are physically valid and capture the essential physics in their respective regimes.

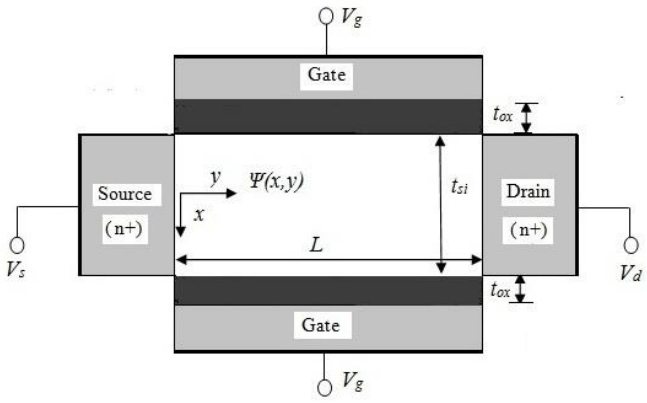

Fig.2. Schematic of the symmetric Double Gate (SDG) MOSFET structure.

2.1 FIRST PROPOSED MODEL

A symmetrical DG MOSFET (SDG) shown in Fig.2 is considered as the fundamental device structure for this work, as the symmetry greatly simplifies the mathematical analysis. The potential at any point in a lightly doped silicon film of DG MOSFET is given in Eq.(1) by Poisson's equation, with electrons as the only mobile carriers.

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q(\psi - V)}{kT}} \tag{1}$$

Here, n_i is the intrinsic carrier density, q is the electronic charge, ε_{si} is the permittivity of silicon, $\psi(x,y)$ is the electrostatic potential termed with respect to Fermi potential and $V(y)$ is the quasi-Fermi potential of electrons at y with respect to the source end. For the given structure, the hole density is considered to be negligible such that $q\psi/kT \gg 1$.

The general solution in terms of surface potential [26] is expressed as:

$$\psi(x) = V + 2v_T \ln\left(\frac{2\rho L_D}{t_{si}}\right) - 2v_T \ln\left[\cos\left(\frac{2\rho x}{t_{si}}\right)\right] \tag{1}$$

where, t_{si} is the silicon film thickness, $L_D \cong \sqrt{\frac{2\varepsilon_{si} v_T}{q n_i}}$ is the intrinsic Debye length, $v_T \equiv kT/q$ denotes the thermal voltage and ρ is an important intermediate parameter [26] expressed as:

$$\left(\frac{V_g - \Delta\varphi - V}{2v_T}\right) - \ln\left(\frac{2L_D}{t_{si}}\right) = \ln(\rho) - \ln\left[\cos(\rho)\right] + 2rp\tan(\rho) \tag{3}$$

Here, $\Delta\varphi$ is the work function difference between both the gates with respect to intrinsic silicon, $r \equiv (\varepsilon_{si} t_{ox})/(\varepsilon_{ox} t_{si})$ is the structural parameter, with t_{ox} being the oxide thickness, ε_{ox} being the permittivity of oxide layer, ε_{si} and t_{si} being the permittivity and thickness of silicon layer respectively. The inversion charge density is expressed by Gauss law as $Q_i = v_T((8\varepsilon_{si})/t_{si})\rho\tan(\rho)$. The current for a long channel SDG MOSFET is obtained by integrating the current continuity equation. The final expression is then given as

$$I_{ds} = \mu \frac{W}{L} \frac{8\varepsilon_{si}}{t_{si}} v_T^2 \left[f(\rho_d) - f(\rho_s) \right] \tag{4}$$

Here, the intermediate function f is defined as $f(\rho) \equiv -2\rho\tan(\rho) + \rho^2 - 2r\rho^2\tan^2(\rho)$. The intermediate parameters ρ_d (ρ at drain) and ρ_s (ρ at source) can be solved using boundary conditions with V corresponding to voltage at source or drain, depending on the position. Further, Yu et al. [16] has provided accurate explicit solutions for obtaining the above intermediary parameters. Referring to [27], the threshold voltage V_t is expressed as:

$$V_t = \Delta\varphi + 2v_T \ln\left[\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si} v_T}{q n_i}}\right] + 2v_T \ln\left[\frac{\varepsilon_{ox} t_{si}\left(V_{gs} - \Delta\varphi\right)}{2\pi\varepsilon_{si} t_{ox} v_T}\right] \tag{5}$$

For a gate with mid-gap work function, $\Delta\varphi = 0$ and for n+ polysilicon, $\Delta\varphi = -E_g/2q$. Here, n+ polysilicon is chosen as gate material to achieve lower threshold voltages. The drain current in Eq.(4) is applicable for long channel SDG MOSFETs only and hence fails to capture the velocity saturation effect and other SCEs. The model proposed in [18] addresses the above issue successfully. The concept of velocity-field relationship [28] for holes and electrons determines the critical field E_C, at which the velocity of electrons saturate due to scattering effects. This results in a lower saturation current. In short channels devices, there exists a lack of proportionality between drift velocity v_d and longitudinal component of electric field E_y, due to which the velocity of electrons in the channel saturates. So, the drain current I_{ds} saturates at a much lesser drain voltage unlike the saturation that happens in a long channel device due to pinch off. This important physics is effectively captured in the proposed model by means of velocity factor term P_{vsat} defined as:

$$P_{vsat} = 1 + \left(\frac{\mu_{eff}}{v_{sat}}\right)\frac{V_{ds}}{L} \tag{6}$$

where, saturation velocity $v = v_{sat} = \mu_{eff} E_c$ for high electric fields. E_c is the critical electric field that determines the velocity saturation, μ_{eff} is the effective mobility. For low electric fields, the velocity term is given as in Eq.(7).

$$v = \frac{\mu_{eff} E}{\left[1+\left(\frac{E}{E_C}\right)^n\right]^{1/n}} \quad (7)$$

where, n=2 for electrons and n=1 for holes. The velocity saturation factor P_{vsat} completely captures the above physics and is included here to calculate the drain current. The velocity saturated drain current I'_{ds} is expressed in Eq.(8) as:

$$I'_{ds} = \frac{I_{ds}}{P_{vsat}} \quad (8)$$

By solving $\frac{dI'_{ds}}{dV_{ds}} = 0$, the saturation drain voltage V'_{dsat} at which drain current saturates is obtained as in [18]. A key differentiation between velocity saturation in short channel device and pinch-off in long channel device is that in the former case, the inversion charge density at the drain does not vanish. Further, beyond the saturation point V'_{dsat}, carriers moving at the saturation velocity are no longer confined to both the surface channels of the DG structure. The results in the next section show that the drain current in a short channel DG MOSFET will continue to increase above the velocity saturation point with a non-zero magnitude of output conductance. The physical causes for such behaviour are channel length modulation (CLM), change in the threshold voltage and other SCEs. Hence, beyond the given condition $\left(V_{ds} > V'_{dsat}\right)$, the above effects must be included in Eq.(8). Firstly, the CLM effect is incorporated by replacing L with L-l_p, where the parameter l_p represents the distance between velocity saturation point and the drain [7]. The value of l_p is determined using pseudo-2D analysis [28]. As l_p increases with the drain voltage, the velocity saturated drain current also rises slowly with non-zero conductance even in the saturation region. Secondly, as the effective gate length L is rigorously scaled down towards the sub-micron regime, the threshold voltage roll-off effect becomes important. As the silicon film is lightly doped with p-type dopants, the first order effect is included as a positive voltage shift by a magnitude $\Delta V_t = \frac{qN_a t_{si}}{2c_{ox}}$. If the silicon film is lightly doped with n-type dopants, then the first order effect may be included as a negative voltage shift. Thus, the threshold voltage for n-channel DG MOSFET with SCEs can be expressed as:

$$V_{t,SCEs} = V_t + \Delta V_t \quad (9)$$

Eq.(6)-Eq.(9) clearly denote the inclusion of SCEs in the velocity saturated drain current model applicable for a symmetric DG MOSFET model. However, as the scaling approaches below 30nm, the carrier transport undergoes a fundamental physical change, due to which this model fails. In such scenario, the model must consider nanoscale carrier transport that is exhaustively described in the next sub-section.

2.2 SECOND PROPOSED MODEL

In rigorously nanoscaled devices with channel lengths of (L<30nm), the classical drift-diffusion transport alone is not sufficient to explain the complete physics. If the mean free path of the carriers τ is much smaller than the channel length L, then the transport is primarily drift-diffusive with carrier scattering. As per the ballistic MOSFET theory [30], carrier scattering does not occur if the channel length L is lesser than the mean free path λ and in such case where ($L << \lambda$), the drain current may not depend on L. Rigorously scaled multi-gate MOSFETs are strongly ballistic (close to the ballistic limit [31]) without significant carrier scattering. However, state of art DG MOSFETs exhibit quasi-ballistic nature, which suggests the need to include both ballistic and diffusive transports appropriately. The quasi-ballistic model in [25] considers only Boltzmann statistics and ignores carrier degeneracy. A comprehensive quasi-ballistic DG MOSFET model is proposed in [23] and [24] that includes Fermi-Dirac statistics and carrier degeneracy. This model partly evolves from the very well-known Natori's ballistic model, which is modified further from fully ballistic to a quasi-ballistic model by including scattering physics in terms of reflection and transmission coefficients.

The drain current for a fully ballistic symmetric DG MOSFET under non-equilibrium conditions [9] is expressed in Eq.(10) as:

$$I_{ds} = 2G\left[F_{1/2}(\xi) - F_{1/2}\left(\xi - \frac{V_{ds}}{v_T}\right)\right] \quad (10)$$

where

$\xi = \left(\frac{E_{fs} - E'_c - E_0}{kT}\right)$ and the parameter $G = \frac{2\sqrt{2m_t}qW(kT)^{3/2}}{h^2}$.

Eq.(10) is derived from the concept of flux theory. The expression in the brackets for ξ is taken from [9] and is given as

$$\left(\frac{E_{fs} - E'_c - E_0}{kT}\right) = \ln\left[0.5\left\{\sqrt{\left(e^{V_{ds}/v_T} - 1\right) + 4\exp(g)} - 1 - e^{V_{ds}/v_T}\right\}\right] \quad (11)$$

where g is another intermediate parameter expressed as

$$g = \left(\frac{h^2 \varepsilon_{ox}\left(V_{gs} - V_t\right)}{4\pi q k T t_{ox} m_t} + \frac{V_{ds}}{v_T}\right) \quad (12)$$

In Eq.(12), h is the Plank's constant, thermal voltage v_T=kT/q and electron effective mass in the transverse direction m_t=0.19m_0 where m_0 is the free electron mass. The Eq.(11) and Eq.(12) conceptually relate the energy band diagram of nanoscale MOSFET illustrated in Fig.3.

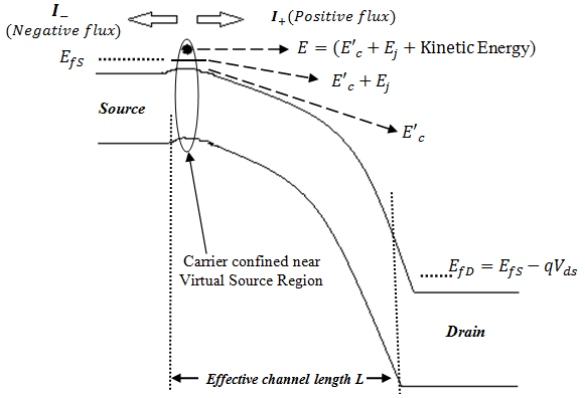

Fig.3. Schematic of a bulk nanoscale MOSFET band diagram under high-drain bias conditions [9]. For the proposed work of SDG MOSFET, a vertical mirror image of the above band diagram is to be considered due to bottom gate

In the schematic of Fig.3, E_{fS} and E_{fD} denote degenerately doped source and drain Fermi levels respectively (denoted by dotted lines), *I*- and *I*+ are left to right and right to left current components based on the concept of flux theory.

As per the ballistic transport theory [27], the highest potential barrier (shown in Fig.3) is near the source where the electrons populate with allowed discrete sub-bands. The velocity saturates at the top of the potential barrier where the vertical component of the electric field is nearly zero. Carriers confined in the inversion layer occupy discrete sub-bands with a minimum energy E_j above conduction band E_c'. The energy level E=(E_c'+E_j+Kinetic Energy). Eq.(10) represents the net drain to source current with one sub-band approximation (lowest being *j*=0 of un-primed valley). Using Blakemore's explicit analytical model [32], the Fermi-Dirac integral in Eq.(10) can be expressed as:

$$F_{1/2}(\xi) \approx 2/3(\xi)^{3/2} \tag{13}$$

Eq.(10) represents maximum current carrying ability of a fully ballistic hypothetical symmetric DG MOSFET, which is derived by ignoring all carrier scattering processes. As modern nanoscale devices exhibit quasi-ballistic nature, the inclusion of scattering effects in terms of transmission and reflection coefficients is necessary. The scattering equations in terms of transmission coefficient (T_C) and reflection coefficient (R_C) is given in Eq.(14) as

$$T_C+R_C=1 \tag{14}$$

where

$$T_C = \lambda/(\lambda+L) \text{ and } R_C = L/(\lambda+L) \tag{15}$$

In Eq.(15), λ represents the mean free path of the carriers calculated similarly as in [17]. The Eq.(14) and Eq.(15) provide a simple relation between diffusive and ballistic transport. The Table.1 lists the different carrier transports occurring in MOSFETs based on the concepts of scattering physics.

Table.1. Different carrier transport with conditions as per scattering theory

Condition	Type of carrier transport
T_C=1 and $L<\lambda$	Ballistic with no scattering
T_C=0 and $L\gg\lambda$	Drift-Diffusive with significant scattering
$0<T_C<1$ and $L\geq\lambda$ (low drain bias)	Quasi-Ballistic with uniform scattering throughout *L*
$0<T_C<1$ $L\approx\lambda$ and $\delta<\lambda$ (high drain bias)	Quasi-Ballistic with positional carrier scattering near virtual source

In realistic quasi-ballistic devices, the transmission co-efficient varies between 0 and 1. The device in the proposed work consists of a low field region near the source that is firmly controlled by gate voltage V_{gs} and a high field region near the drain that is controlled by drain voltage V_{ds}. For low drain bias, channel length *L* and the mean free path λ are sufficient to determine carrier transport. This condition is shown in Fig.4(a). The shaded data in Table.1 suggests that for very low drain voltages, the entire channel acts as critical channel length with uniform scattering throughout *L*. However, for high drain voltages (Fig.4(b)), the carrier scattering largely depends on the critical length δ that is positioned just near the virtual source. The parameter δ is a function of drain voltage V_{ds} and its dependency are given by a semi-empirical solution in [24].

Based on the preceding explanation and considering the condition for the critical scattering length near virtual source as $L\approx\lambda$ and $\delta<\lambda$, the transmission co-efficient and reflection terms in Eq.(15) are re-written by replacing *L* by δ and further expressed in Eq.(16) as:

$$T_C = \lambda/(\lambda+\delta) \text{ and } R_C = \delta/(\lambda+\delta) \tag{16}$$

Using Eq.(16), the drain current equation in Eq.(10) is finally modified and expressed in Eq.(17) as

$$I_{ds} = 2GT_C\left[F_{1/2}(\xi) - F_{1/2}\left(\xi - \frac{V_{ds}}{v_T}\right)\right] \tag{17}$$

Eq.(17) represents the drain current that includes quasi-ballistic transport in the presence of scattering and carrier degeneracy effects in nanoscale regime. This model however ignores quantum effects. In the next section, simulation results of both the models are illustrated and a comparative analysis is done that describes the diverse carrier transports arising due to channel length scaling.

3. RESULTS AND DISCUSSIONS

The results for the proposed velocity saturation based short channel DG model (section 2.1) and quasi-ballistic nanoscale model (section 2.2) are presented in this section. The DG device in Fig.2 is taken as reference considering different channel lengths. The feasible values considered for obtaining results are; channel width *W*=0.5 µm, silicon layer thickness t_{si}=5nm, oxide layer thickness t_{ox} = 1nm, doping density of Si film Na=1×10^{12} cm^{-3}, bulk electron mobility μ=300cm^2/Vs. Effective mobility for electrons μ_{eff} is computed as a function of surface potential ψ_s and gate voltage V_{gs} and the same is used to assess the mean free path λ. The mean free path λ and the thermal injection velocity v_{therm} with which the electrons travel is computed as in [23] and are found to be approximately 8-10nm and 1.24×10^7 cm/s, respectively.

The Fig.5 and Fig.6 represent the output and transfer characteristics for the model described in section 2.1 respectively. Equation (4) that gives the long channel drain current [13] is represented by dash lines. While, Eq.(8) represents velocity saturation-based model [18] is illustrated by lines with square symbols. This curve effectively captures the short channel effects. Here, the transport equations are drift-diffusive within the channel limits mentioned (*L*=100nm). Due to velocity saturation, the drain current I_{ds} saturate at a much lower drain voltage unlike the saturation in a long channel device due to pinch off. The drain current in a short channel MOSFET can still increase beyond the velocity saturation point with a non-zero output conductance. The prime causes are CLM and change in the threshold voltage. This signature effect is clearly observed in Fig.5.

The concept of ballistic transport in MOSFETs comes from the theory of scattering physics. Current state-of-art multi-gate MOSFETs undergo rigorous channel length scaling; exhibit quasi-ballistic transport. The Fig.7 and Fig.8 represent the output and transfer characteristics for the model described in section 2.2 respectively. In both the figures, the proposed quasi-ballistic DG model (line with symbols) [23] is compared with fully ballistic

DG model [10] (dots). Further, the curves apparently distinguish the quasi-ballistic currents with uniform scattering and positional scattering under low and high drain biases respectively. The proposed model considers the drain bias dependency on the critical scattering channel length δ. The magnitude of δ is calculated through a semi-empirical approach [24]. At the critical channel length δ, carriers cannot diffuse faster than the thermal injection velocity v_{therm}. This physically limits the maximum current. The drain current shown in Fig.7 and Fig.8 (line with diamond symbols) illustrates the transport model. Once the carriers diffusively cross the critical length δ, the transmission becomes ballistic. If δ increases above mean free path λ and approaches the effective channel length L, then the drain current scales down towards the quasi-ballistic phase with uniform scattering (represented by Lines with square symbols in Fig.7).

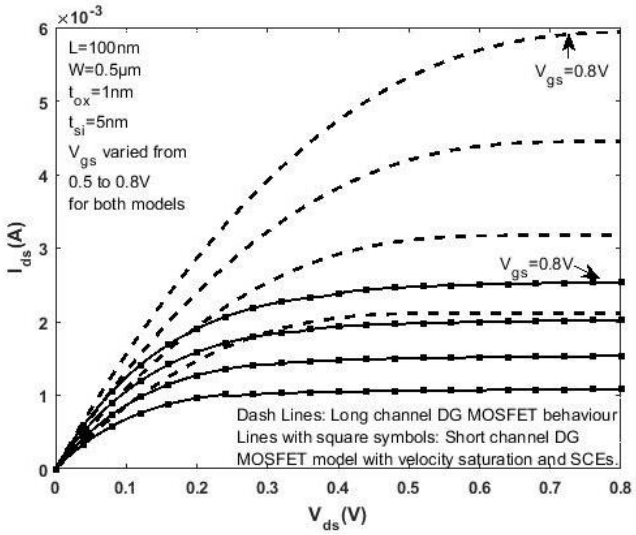

Fig.5. Drain current I_{ds} as a function of V_{ds} for different gate biases. The long channel DG model (Dash lines) fails to capture the SCEs and clearly over-predicts the current. The proposed velocity saturated model (Lines with square symbols) effectively captures the signature effect

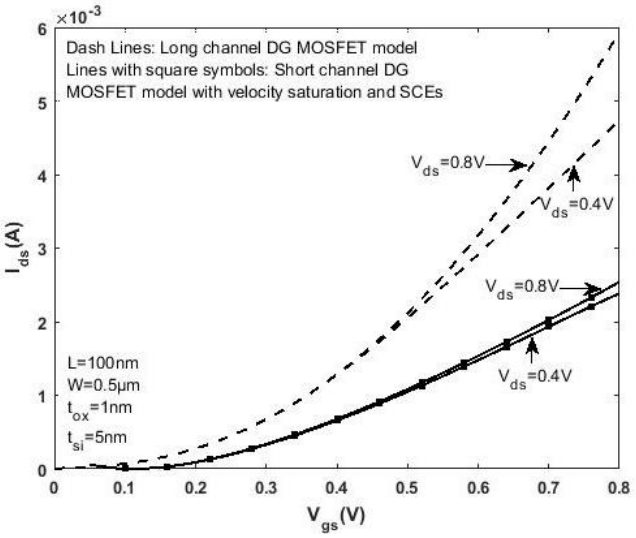

Fig.6. Drain current I_{ds} as a function of V_{gs} for different drain biases. The long channel DG model (Dash lines) over-predicts the current. The velocity saturated model (Lines with square symbols) includes SCEs and results in lesser current.

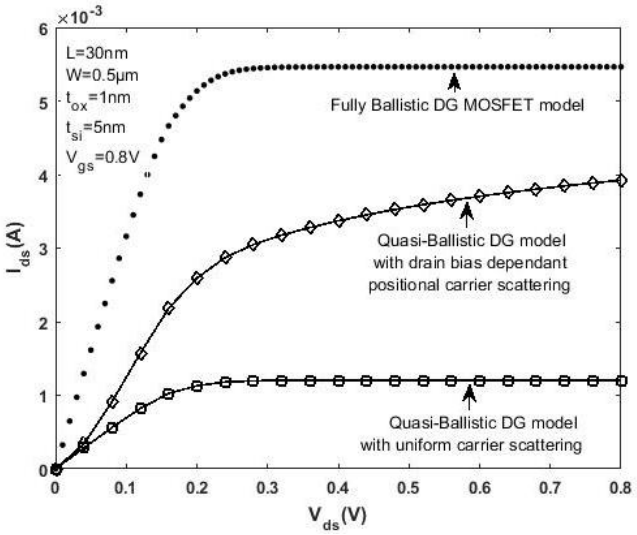

Fig.7. Drain current I_{ds} as a function of V_{ds} in the nanoscale regime under different scattering scenario. The proposed quasi-ballistic DG model (line with square symbols) clearly illustrates the carrier transport physics in the nanoscale regime. The fully ballistic current is mentioned for reference.

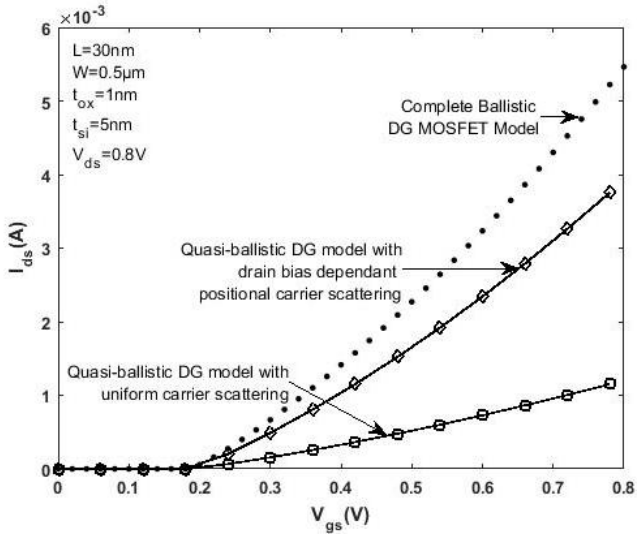

Fig.8. Drain current I_{ds} as a function of V_{gs} in the nanoscale regime under different scattering scenario. The proposed quasi-ballistic DG model (line with square symbols) effectively captures the essential physics

The real comparison of the models proposed in section 2.1 and 2.2 is done in Fig.9 and Fig.10. The velocity saturation model in Eq.(8) is perfectly valid when L≈100nm, however when the channel length is rigorously scaled down in the ranges L≈30nm, the model over predicts the current. In Fig.9, the velocity saturation model erroneously over-predicts the drain current beyond the ballistic limit. The same results are observed in Fig.10 also. On further scaling the error increases.

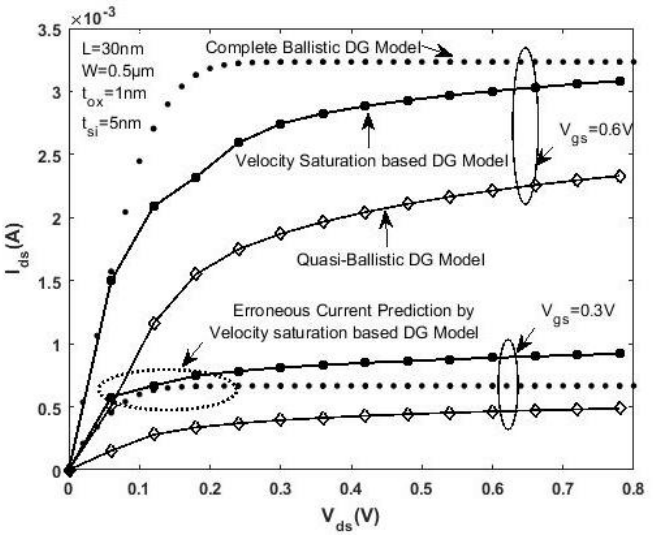

Fig.9. Comparison of output current characteristics for the proposed models. The quasi-ballistic DG model (Eq.(17)) clearly surpasses the velocity saturated DG model (Eq.(8)) in terms of physical accuracy. For V_{gs}=0.3V, the velocity saturation-based model erroneously over-predicts the drain current beyond the ballistic limit.

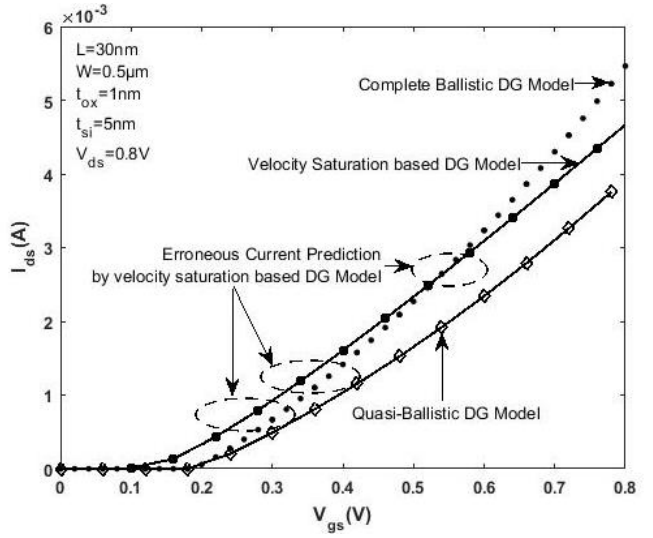

Fig.10. Comparison of transfer characteristics for the proposed models. The quasi-ballistic DG model (Eqn.17) is more physically accurate when compared with the velocity saturated DG model (Eq.(8)) in nanoscale regime. At V_{ds}=0.8V, the velocity saturation-based model erroneously over-predicts the drain current in the threshold limits

This fundamental physical difference between both the models is because of the way the scattering rate and scattering positions are applied to the channel. The velocity saturation model considers the scattering and carrier saturation at the drain end. However, the quasi-ballistic model considers the carrier scattering at the critical channel length δ near the virtual source. Such consideration is found to valid on comparison with device processes. This interesting physics strongly recommends the usage of quasi-ballistic model over the velocity saturation model in the nanoscale regime for circuit simulation applications. Further, in terms of model continuity also, the quasi-ballistic model supersedes the velocity saturation model in the nanoscale regime. Both the models ignore quantum mechanical tunnelling, as it is out of the context scope. However, for very narrow channel with L≈10nm, the quantum transport must be included. The proposed models are coded in MATLAB platform [33] and are numerically verified with simulation results of MOSFet-PADRE tool [34] [35].

To summarize, the proposed work discusses diverse carrier transport mechanisms occurring in multi-gate MOSFETs in different channel length regimes. The velocity saturated DG model is a short channel model that is valid in the sub-micron channel length range, while the quasi-ballistic model is a comprehensive nanoscale compact model that applies to current state-of-art realistic devices. Both the models exhibit continuity in terms of drain current. A comparative analysis of the proposed models in terms of different carrier transport is done through simulations, considering the scaling restrictions in different regimes. The simulation results also demonstrate the efficacy of the models in capturing the essential physics in different channel length regimes. Hence, the proposed multi-gate models may be suitably considered in the next generation circuit simulators for nanoscale modelling applications.

4. CONCLUSION

Multi-gate MOSFETs have enabled the extension of CMOS technology in the nanoscale regime. The proposed work describes velocity saturation-based DG model and quasi-ballistic DG model in the nanoscale regime. The work discusses the diverse carrier transport mechanisms occurring in multi-gate MOSFETs in different channel length regimes. Further, a qualitative comparative analysis of carrier transport for both long and rigorously scaled short channel DG devices is done. The work also discusses the validity of the proposed transport models and their scaling restrictions in different regimes. The simulation results demonstrate the continuity of the models without ignoring the essential physics. Such qualitative comparative analysis aids in the selection of suitable nanoscale compact models for circuit modeling applications.

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