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# VLSI USAGE OF A PRODUCTIVE MBIST ARCHITECTURE UTILIZING RLFSR

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***Abstract***

***This article introduces a power efficient application of FPGA created through a Memory Built in Self Test (MBIST). It has 2-bit Linear Feedback Shift Register (LFSR) array, which changes the direction of the previous process and creates high MBIST structures. This unwanted change affects all MBIST's power consumption. The proposed MBIST with LFSR ring reduces the power consumption problem. The 2-bit 2N bit model generator is connected to the 2-bit (N-2) and 2-bit 4-bit (N-2) LFSR model generator, which are separately controlled using two separate clocks with two different frequencies, creating each location address high memory test. The proposed architecture has been implemented on Vertex4 FPGA technology in Xilinx software. The results enhance proposed design's performance when compared it with the existing design.***

***Keywords:***

***Xilinx, FPGA, Switching Activity, 2D-LFSR, Ring LFSR (RLFSR), Memory Built in Self Test (MBIST)***

## 1. INTRODUCTION

. In memory test, there are many problems with the design generator and System-On-Chips (SOC), especially power dissipation. In general, system's power dissipation is greater in test mode when compared with normal mode [23]. This is due to, consecutive vectors used in normal circuit mode, there is a significant correlation and this may not apply to the test vectors used. The decrease in correlation between continuous test vectors increase the switching function and gradually dissipates the power in the circuit. Another reason for increasing performance during testing is that test engineers can test center in parallel for reducing test usage time. This extra performance (average or maximum) can lead to problems like immediate loss of performance, difficulty verifying the performance and overall performance of the product, and reducing costs [26]. The use of low power tests is important in designing and testing VLSI today.

Existing work involved in developing the 2-bit 4 pattern LFSR configuration changes the model and a clock signal to reduce the use of toggle function in proposed control signal. The generated 2*N*-bit format is controlled by two various clocks with two various frequencies in conjunction with conventional (*N*-2)-bit 2 $^{(N-2)}$, bit LFSR 2bit-4 pattern etc. The transition between the two modes is reduced to toggle mode is still significantly reduced due to the configuration of the 2-bit generator, as a result of which the proposed reduction of dynamic performance [9]. Apart from power dissipation in SOC [8], main issue that arises in the micronutrient technology, SOC design and leads to many thousands of gallons, especially in memories, but now integrated, together with the chip. From 2014, it is estimated that a typical 94% of the area occupied by the storage parts drawn thousands of gallons. In SOC, an important role is played by memory. Memory is a lack of a high probability of defect with regard to other types of customers and that the testing is required the remembrance. Best solution for solving small I/O pins count in circuit is BIST for Memory [2].

The BIST test pattern generator is used for generating write/read control, data bus and addresses bus signals in conventional MBIST and are applied to memory under test [1]. Memory location is indicated using address bus and in this specific memory location, operation to be performed are determined using Read/write control signal and data be to be written or read from the memory location pointed by address bus is included in data bus. The Fig.1 shows basic build in self-test structure.

In this paper highlighted the importance of models running fast and well to provide coverage for memory loss. Based on algorithms described using gallop, March, scan, etc., memory cell failure is tested using BIST engine architecture. In a MBIST, address generator is used for generating memory location address for testing faults [3]. According to the testing algorithm, address generator is designed. For MBIST, different address generators are utilized. A multiplexer and two counters combination is used in programmable MBIST as address generator [4];[10].

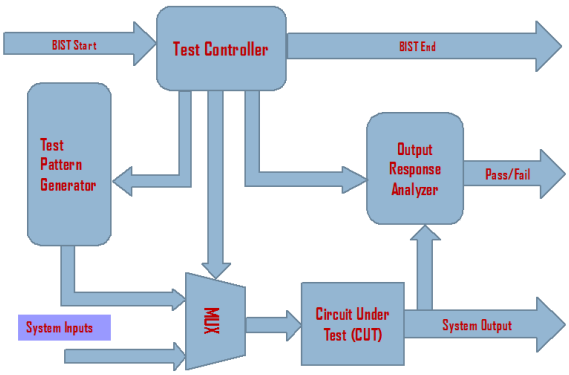


Fig.1. Basic MBIST Architecture

Built In Self-Test (BIST) engine design which is reusable is termed as joined example Generator and Checker (CPGC) [11] is executed on Intel 14nm 3DS IC. United alludes for joining MBIST and Interconnect BIST (IBIST) abilities into one BIST motor it's additionally portrayed an auto-fix innovation, which joined with deficiency discovery capacities, can actually re-map faulty memory be utilizing repetitive memory cells incorporated into DRAM [6]-[7]. It gives critical test time reserve funds in post bundle fabricating stream. CPGC additionally diminished SOC and stage power through On Die Termination (ODT)'s shut circle advancement as well as adjustment. This BIST types upholds IO, memory imperfection recognition, memory auto fix, IO interface preparing, power streamlining/preparing.

Software-Based Self-Test (SBST) is an adaptable as well as minimal effort answer for on-line March test application and blunder identification in little recollections. A SBST program

improvement approach is executed in [12] for on-line testing of little store recollections in chip. The improvement of huge scope reconciliation testing frameworks, explicitly the construction plan and streamlining of BIST plan dependent on two-dimensional (2-D) straight criticism move registers [13].

The 2-D LFSRs is producing pre-registered test designs (to identify irregular example safe deficiencies) and arbitrary examples (for recognizing irregular example discernible blames) and have benefits of high issue inclusion at-speed testing. STUMPS design includes Linear Finite State Machine (LFSM), for example, LFSRs of outside XOR or inward XOR class as well as Cellular Automata (CA) [14], is generally utilized as on-chip test design generator. It drives checked flip-flops chains in equal (2-D scan).

Low-transition LFSR which depends on bit trading LFSR (BT-LFSR) [15]-[16] is made using LFSR as well as 2×1 multiplexer. They are used for creating test designs to examine based underlying individual tests; it decreases changes quantity which happens during sweep chain contribution in filter move activity 50% by half with those examples delivered using regular LFSR. It diminishes the general exchanging movement in Circuit Under Test (CUT) in test applications. Modified LFSR is utilized for lessening advances quantity at CUT contributions by 25% utilizing a bit trading method [17]. For BIST, Test Pattern Generator (TPG) which diminishes exchanging movement in test application. TPG, called Double Speed LFSR (DS-LFSR) [18] has LFSRs, a moderate LFSR and ordinary speed LFSR. Moderate LFSR is driven using typical clock's moderate clock with (1/d) speed, which drives ordinary speed LFSR. The DS-LFSR utilization diminishes advances recurrence at circuit inputs driven using moderate LFSR, prompting a decrease in exchanging movement in test application. DS-LFSR is for accomplishing high shortcoming inclusion by guaranteeing that examples produced by it are special and consistently dispersed.

Another significant test design age procedure called Low-Transition summed up straight input move register (LT-GLFSR) with Bipartite [18]-[20], Bit-Insertion and its yield bits positions are traded via trading methods (Bit-Swapping). It presents moderate examples in the middle of sequential test vectors created using GLFSR which is empowered using non covering clock plot. Limited state machine performs this and produces control signals grouping. LT-GLFSR is utilized in CUT for diminishing normal and pinnacle power during changes. LT-GLFSR designs serious irregularity level and improves connection between continuous examples. LT-GLFSR doesn't rely upon CUT and thus it is utilized for BIST and sweep based BIST models.

In this paper, a productive and low force MBIST utilizing altered location generator called Ring LFSR (RLFSR) is introduced in our work. By and large location generator for MBIST has 2-digit LFSR units, a preferred RLFSR position over traditional 2 cycle LFSR is for producing four potential 2-bit mix including '00' and furthermore territory and force proficient than 2D LFSR. For executing proposed address generator plan in Xilinx ISE configuration apparatus and dissected unique force and furthermore absolute force utilization utilizing XPOWER analyzer. Also, further planned MBIST engineering is contrasted and 2D LFSR and touch trading LFSR based MBIST introduced [21]-[25] [30].

In a following order, this paper is organized. In Section 2, works related to MBIST and LFSR with its concern are presented. Their arrangement is available in section 3. Proposed territory design and force proficient MBIST including RLFSR is talked about in area 4. Section V presents simulation results. Conclusion is given in section 5.

## 2. LITERATURE SURVEY

Using reconfigurable Linear Feedback Shift Registers (RLFSR), Pseudo chaos signal generator implementation is presented by Sreenath et al. [5]. Over the generated pseudo-random sequence, employed one dimensional mapping methods like twisted-tent, ship, tent mapping with LFSR to implement design.

Two techniques are presented by Gopalan, et al. [26]. One technique is implemented on memory BIST to check memory array circuit. For repairing fault memory cell, an optimized BISR is used in second technique which is based on Built-in redundancy analysis. Two fault injection methods namely mutants with optimized test pattern logic and saboteurs are used for injecting faults into memory in this proposed BIST technique. For BISR scheme, proposed counting threshold algorithm is used for repairing fault memory once faults are injected into memory cell.

A public key encryption is investigated by Zhou, et al. [27]. For security applications, for sequence computation, an effective algorithm is provided by this. In special environments which requires semantic security, it is used directly where secrete candidate names, 1 or 0's encryption is done. Also provided, this encryption techniques security analysis. Higher resolution problem in LFSR corresponds to its one-way module and LFSR decisional higher resolution problem corresponds to its semantic security.

In conventional verification sequence, low power consumption and fault coverage are not ensured. For this, Twofold State Skip (TFSS) logic is proposed by Mukherjee et al. [28]. In digital circuits, problem with large stuck-at-fault errors are avoided using this and long scan chains are skipped for achieving low scan power and minimizing switching activities. In an arbitrary finite field with GF($2^m$) form which are defined using arbitrary irreducible polynomial $f(x)$, implemented a LFSR based on Montgomery multiplier. The LFSR is a major component in this design.

A LFSR is a major component in design as shown by Dąbrowski, et al. [29]. In automatic test pattern generator based on ring counter, Ring based LFSR is used for minimizing switching activity. Between test patterns with less correlation, test vectors are inserted for minimizing vertical switching transitions. Multiplexers, full adders and XOR gates are included in the external circuits.

Between consecutive test patterns, total transitions count are computed. External circuit is generated, if its value is high and between two test patterns, test vectors are inserted. Between test patterns, correlation is enhanced using this test vector insertion and it also minimizes dynamic power dissipation. A type of linear finite state machine is ring generator which is formed by a circle with memory elements and feedback connections are added slowly which are corresponding to characteristic polynomial's successive terms.

A Twisted-Ring Counter (TRC) based test set embedding approach is used for minimizing test power consumption, test application time and test data storage with few seeds. In deterministic test set, for exploiting high density unspecified bits, an effective seed-selection algorithm is utilized. For complete single stuck-at faults as well as application coverage, data storage and time are minimized.

## 3. PROPOSED METHODOLOGY

Our inspiration is for implementing low-energy self-test memory built into the floor, which is a 2-bit LFSR array**.** However, in general, the MBIST algorithm for modifying the plan has not yet been developed. MBIST technology was found in the middle of external testing in the form of materials compared to test analysis and test generation chip to reduce test cost and time limit. During test patterns application to CUT's input, excessive amount of power is drawn by MBIST, which is major disadvantage of this system. When compared with normal model, there will be a high amount of switching activity in testing modes, which leads to excessive power consumption. The LFRS design is added with some new techniques. With respect to area, they are not providing better results.

In this work, MBIST is implemented using ring LFSR, which is used for preventing transition process. The conventional (*N*-2)-bit 2 (*N*-2) LFSR is connected to the 2-bit 4 model generator and is controlled using two separate meters in the form of two different frequencies. The location of the memory address is MUT. The constant between 2 and the alternative format is greatly reduced and its functionality decreases with changes in the format of the service 2-bit generator configuration, thus enabling the implementation of the MBIST framework. Bit swapping using the new 2D-LFSR fixes the power consumption defects of our previous MBIST framework using LFSR and MBIST.

## 4. MBIST ARCHITECTURE

The LFSR structure of the cycle proposed in this section and its functions are represented using the state map and its logic control design is represented using time charts.

### 4.1. MBIST ADDRESS GENERATOR

Proposed MBIST array has 2-bit LFSR generator units that have already been redesigned generate the entire city. Each RLFSR is activated by a suitable enable signal unit, according to its requirements, the power of which is designed for use in the FSM logic is abated. Based on enable signal from FSM, single bit is generated (1 or 0) in MSB generator. A single clock signal is used for clocking MSB generator and all RLFSR. In interfacing buffer, loaded the selected MSB generator and RLFSR outputs. Then, they are given to memory block as memory address. Output of memory are analyzed using response analyzer and this analysis is done based on MBIST configuration. The Fig.2 shows the overall architecture.

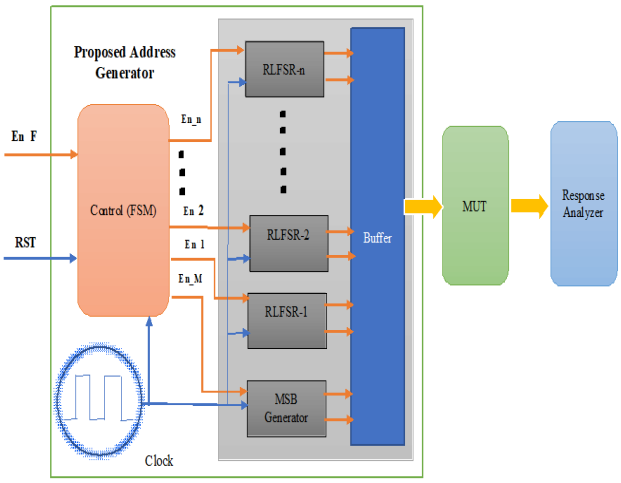


Fig.2. MBIST Architecture

Consider a testing assignment *J* address area inside a memory in test mode. To create *J* these location areas, we need a location generator with bit length *P* and henceforth complete areas *J* and *P* are connected as,

$$J = 2^P \tag{1}$$

In location generators with ordinary LFSRs, the location areas are produced haphazardly. Entropy has been utilized as a boundary for characterizing the haphazardness in example age by a large portion of the researchers. This can be given as,

$$N = -\sum_{k=1}^{J} \gamma_k . \log 2\gamma_k \tag{2}$$

where, $\gamma_k$ is a probability that sign is in pattern *k* and *J* signifies complete example's count.

This measurement can evaluate how pseudorandom characteristics esteems crumble if there is a one-sided change in sequencing or piece determination. All the more explicitly, for an *P*-bit wonderful arbitrary generator we have $J = 2^P$ and $\gamma_k = -\frac{1}{J}$ henceforth and subsequently, the entropy will be $N = P$ mirroring the most extreme haphazardness. An ideal arbitrary created can be addressed as $0 < N < P$. Customary LFSR(CLFSR) units are relied upon for creating pseudorandom designs that act very near ideal irregular numbers $(N \approx P)$. The RLFSR is an 2-digit ordinary LFSR's alteration for producing all four potential 2- bit blend with '00'. In this criticism is given for principal flip-flop contribution via reversing subsequent flip-flop yield as demonstrated in Fig.3. In this example generator when underlying incentive to FF-1 will be '1', FF-2 is '1' at that point criticism esteem is '0' (FF-2 yield's reversal) so yield for next clock beat is Q1=0, Q2=1. Table for conceivable next state is referenced in Table.1.

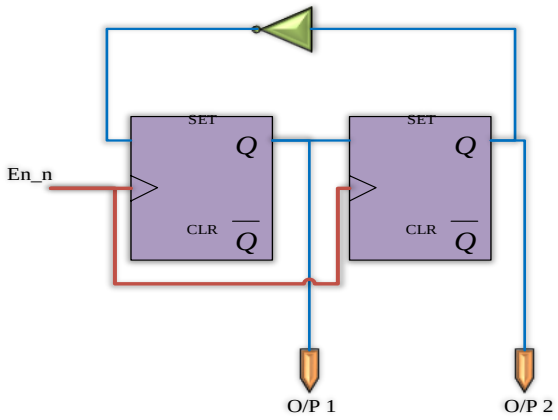


Fig.3. Proposed RLFSR

Table.1. 2-Bit CLFSR Data Flow

| Present Output | | NOT Gate | Next Output | |
|---|---|---|---|---|
| O/P1 | O/P2 | Output | O/P1 | O/P2 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |

The Table.1 classifies, information course through RLFSR for every check cycle. This information stream is unmistakably investigated through a state outline appeared in Fig.4.

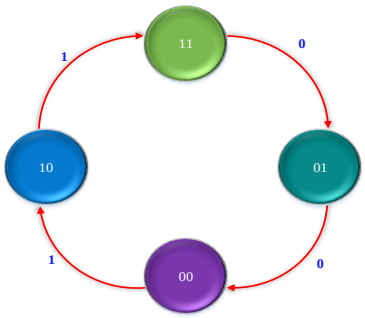


Fig.4. State Diagram for RLFSR

In the event that underlying condition of 2 bits is '11' at that point input delivered by FA is '0', which thusly is put away in FF 1 by moving current state to right and consequently in following positive clock yield from CLFSR is '01'. Consequently, at whatever point positive clock beat is applied state change with 1digit distinction from current worth is acquired. Consider a location generator for areas *J*. Henceforth the location generator ought to be of spot size *P*. All in all, the pattern created by a *P* bit address generator is expressed as,

$$A = a^1 a^2 a^3 .....a^J \tag{3}$$

where, *J* is the quantity of memory areas. Every individual example produced by the location created is addressed as,

$$a^y = a_1^y a_2^y a_3^y .....a_P^y \tag{4}$$

where, $y = 1, 2, .....J$

Considering $J$ patterns created by location generator as a $J \times P$ matrix, with lines addressing every individual pattern $a^y$ and segments are addressing all produced designs *A*.

$$A_{J\times P} = \begin{bmatrix} a_1^1 & a_2^1 & \cdots & a_P^1 \\ a_1^2 & a_2^2 & \cdots & a_P^2 \\ \vdots & \vdots & \cdots & \vdots \\ a_1^l & a_2^l & \cdots & a_P^l \end{bmatrix} \tag{5}$$

In our work, every address design $a^y$ is produced by consolidating yields from RLFSR yields progression and MSB generator. Every pattern created using proposed address generator is addressed as,

$$a^y = \beta C_1^X C_2^X C_3^X .....C_h^X \tag{6}$$

where, $X = 1, 2, .....J$

The RLFSR blocks quantity required *P* to create a pattern with *P* bit size is expressed as,

$$h = \begin{cases} \dfrac{P}{2} & if\ P\ is\ even \\ \dfrac{P-1}{2} & if\ P\ is\ odd \end{cases} \tag{7}$$

Every RLFSR blocks ($C_H$) produces 2-bit design addressed as,

$$Ch = D_K D_O \tag{8}$$

where, $K = 1, 3, 5.....h-1$ and $O = 2, 4, 6.....h$

Parameter $\beta$ in condition, addresses created design's MSB, which is expressed as,

$$\beta = \begin{cases} 1 or\ 0\ , & if\ \ P\ is\ odd \\ \varnothing\ , & if\ \ P\ is\ even \end{cases} \tag{9}$$

## 4.2. CONTROL LOGIC DESIGN

Address patterns along these lines produced because of the techniques portrayed in the before segment incorporate an irregular tally of changes between each yield designs if not arranged appropriately. To defeat this appropriate control signals must be produced by utilizing FSM rationale. The FSM is empowered by an empower signal $Bh\_W$ and introduced by $CDZ$ (reset) signal. In light of the worth, individual empower signals $(Bh\_1, Bh\_2....Bh\_h)$ are empowered by the FSM regarding the info check signal as demonstrated. The circumstance chart appeared in Fig.5 underneath grandstand the FSM empower signal age regarding the info clock signals for $P = 4$

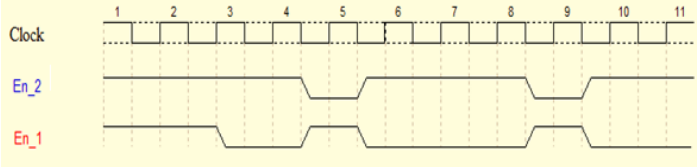


Fig.5. FSM Enable Signal Generation's Timing Diagram with Input Clock Signals Reference for *P*=4 (even)

For a memory with area *J*=16 with *P*=4 (even) address generation based on proposed address generator is presented here.

For $P$=4 (even), there is no requirement for MSB and subsequently $\beta = \varnothing$ and since $h = 2$, 2 RLFSR blocks must be incorporated and examples in this way produced is organized in Table.2.

Table.2. Pattern Generation of Two RLFSR

| $C_1$ | $C_2$ |
|---|---|
| 11 | 11 |
| 11 | 01 |
| 11 | 00 |
| 11 | 10 |
| 01 | 10 |
| 01 | 11 |
| 01 | 01 |
| 01 | 00 |
| 00 | 00 |
| 00 | 10 |
| 00 | 11 |
| 00 | 01 |
| 10 | 01 |
| 10 | 00 |
| 10 | 10 |
| 10 | 11 |

On account of memory with area $J$=32, $P$=5, since $P$ is odd, MSB generator is empowered using FSM. In this way producing the progressive location designs with one hamming distance. Circumstance graph for $P$=5 is as demonstrated in Fig.6

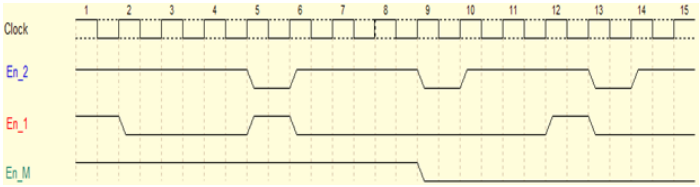


Fig.6. FSM Enable Signal Generation's Timing Diagram with Input Clock Signals Reference for $P$=5 (odd)

Empower signal for $C_h$ is produced via upsetting overall Eq.(10) while any remaining empower signal age from FSM follows Eq.(11) along these lines permitting a state change in the RLFSR.

$$\overline{B}(C_h) = 2^0(4y)+1 \tag{10}$$

$$B(C_{H-X}) = 2^X(4y)+1 \tag{11}$$

where, $y = 0,1,2,3.....i$ and $X = 1,2,3....h-1$

$$I = \begin{cases} \dfrac{2^P}{P-1} & if\ \ P\ is\ odd \\ \dfrac{2^P}{P} & if\ \ P\ is\ even \end{cases}$$

From condition in Eq.(10), plainly that for each $\overline{B}(C_h)^{th}$ clock signal, empower signal for $C_h$ become low which makes piece change in location generator's MSB, by '$m$' is odd in MSB generator then $B_P$ empowers clock signal dependent on condition [12].

$$B(MSB) = 2^{\left(\frac{2^P}{P-1}\right)}(4y)+1 \tag{12}$$

## 5. EXPERIMENTAL RESULT

In this segment starts with MBIST engineering's VLSI execution's concise review with $P$ = 4, 5 digit are clarified via related RTL chart and afterward followed by individual results discussion. Proposed zone, power productive MBIST having RLFSR are effective than MBIST having other LFSR methods.

Proposed zone productive MBIST is actualized on FPGA innovations specifically Vertex4 (xc4vlx200-11-ff1513 gadget) utilizing Xilinx devices forms 14.5. Plan is executed on Vertex4 advancements for taking into consideration a reasonable correlation with most pertinent work.

Vertex-4 is set as target gadget with zone and force advancement. The XST devices in Xilinx blend plans and guide for objective gadget. Inbuilt ISIM test system is utilized for planned design cycle's confirmation. Investigations are completed in PC with windows 7 working framework with 4 GB smash, center i3 Intel processor.

### 5.1. AREA OF PROPOSED M BIT MBIST

The RTL specialized schematic for MBIST with P=4, 5 are actualized in Xilinx ISE apparatus and shown in Fig.7 and Fig.8 separately.

RTL schematic graph, gadget recreation synopsis used for organizing proposed plan's zone prerequisite is shown in Table.3. Also, experimental results are appeared in Fig.9 and Fig.10.

Table.3. Proposed $P$ bit MBIST's Area Requirement

| Cell usage | $P$=4 | $P$=5 |
|---|---|---|
| Basic Elements (LUT, inverter) | 8 | 12 |
| Latches/ Flip-flops | 14 | 18 |
| Clock buffers | 1 | 1 |
| Output/ Input buffers | 11 | 12 |

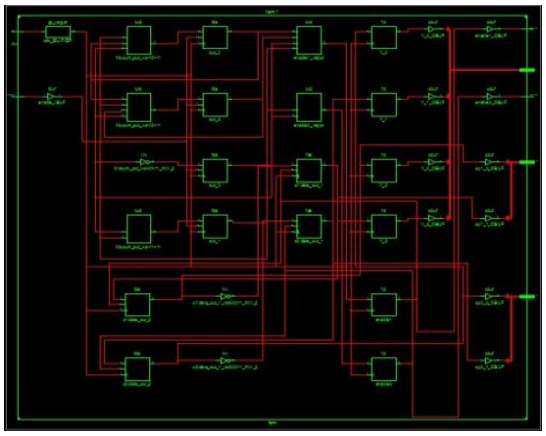

Fig.7.MBIST's RTL Schematic ($P$=4)

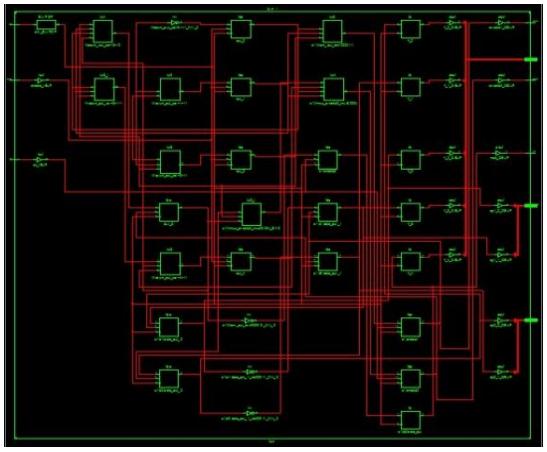

Fig.8. MBIST's RTL Schematic (*P*=5)

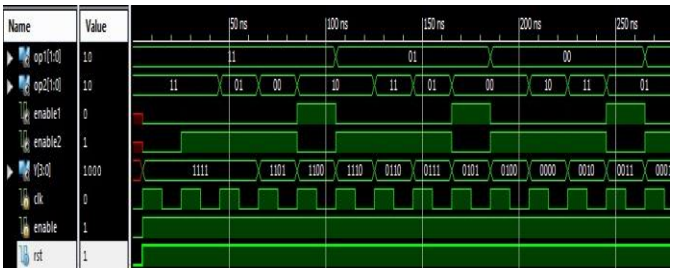

Fig.9.MBIST's Simulation Results (*P*=4)

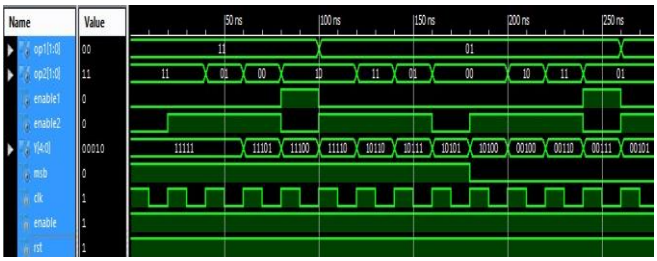

Fig.10. MBIST's Simulation Results (*P*=5)

Proposed model's zone prerequisite is more proficient than MBIST design having other LFSR like Bit trading LFSR and 2D-LFSR which are available by graphical portrayal in Table.4.

Table.4. Area Comparison between Proposed MBIST using RLFSR and MBIST using 2D-LFSR

| Parameters | MBIST RLFSR | MBIST 2D-LFSR |
|---|---|---|
| Leakage Power | 1.36 | 9.32 |

Proposed MBSIT's dynamic force is decreased by abstaining from exchanging movement utilizing RLFSR, which are appeared by graphical portrayal in Table.1.

## 6. CONCLUSION

Through this work, we have endeavored for presenting new engineering for MBIST utilizing RLFSR, where in testing significant piece of force utilization is involved. Control rationale configuration used for beating control signals produced by FSM logic.

Location designs accordingly created because of the systems depicted in groups of an irregular check of advances between each yield designs if not arranged appropriately. The proposed MBIST engineering is power proficient than past location generators, in light of the fact that RLFSR used to decrease exchanging action when utilized in MBIST.

There by utilizing this low force BIST structures on-chip, power consumption is minimized in test application. We demonstrated that proposed design is region and force productive than past LFSRs.

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