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ROBUST AND SCALABLE HYBRID 1-BIT FULL ADDER CIRCUIT FOR VLSI APPLICATIONS

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Abstract

This research paper presents a novel 22-transistors (22T), 1-bit 'full-adder' (FA) for 'Very-large-scale-integration' (VLSI) applications. The proposed FA is derived from the hybrid logic, which is a combination of 'gate-diffusion-input' (GDI) technique, 'transmission gate' (TG) and 'static CMOS' (SCMOS) logic. To assess the performance of the proposed FA, it is compared with state-of-the-art FAs in terms of 'Design Metrics' (DMs) such as power, delay, 'power-delay-product' (PDP), and 'transistor count' (TC). For a fair comparison, all FAs under consideration have been designed and simulated under common 'process-voltage-temperature' (PVT) conditions. The simulations have been conducted using Cadences' Spectre simulator using45 nm 'predictive-technology-model' (PTM). The simulations indicate that the proposed FA dissipates an 'average power dissipation' (APD) of 1.21 μW at an input signal frequency, fin=200 MHz and supply voltage, V_{dd}=1 V. It has a 'worst case delay' (WCD) of 135 ps and has a 'power-delay-product' (PDP) =0.163 fJ. Further to assess the scalability the proposed FA in terms of V_{dd} and input signal operand size, it is embedded in 64-bit(64b) 'ripple carry adder' (RCA) chain and simulations were conducted by scaling down the V_{dd} from 1.2 V to 0.4 V in steps of 0.2 V. The simulation results show that, only the proposed FA and other 2 reported as have the ability to operate in 64b RCA under different values of V_{dd}, without using any intermediate buffers. Further, it is observed that the proposed FA has a better power, delay, and TC as compared to the other 2 FAs.

Keywords:

Full Adder, PDP, Low Power, Static CMOS, Gate-Diffusion-Input, Transmission-Gate-Logic

1. INTRODUCTION

The future generation of battery-operated portable electronic gadgets such as cellphones, laptops, etc. need to handle a huge amount of computationally intensive data related to multimedia applications [4] [5]. The broad range of multimedia applications is audio, speech, video, and image processing, etc. One unique requirement in all these systems is to enhance the battery life by lowering their power consumption. This naturally demands the design of energy-efficient arithmetic systems. The arithmetic systems that handle these multimedia applications generally use the 'Digital-Signal-Processing' (DSP) blocks as a core to process various arithmetic operations [7] [15]-[16]. The most basic arithmetic operation in these systems is an addition, the adder circuit being a critical element plays an important role to determine the overall accuracy and performance of a system. Thus, in the context of DSP, the design and optimization of an adder circuit with an optimized performance always finds the center of interest for researchers [15]. The state-of-the-art literature has focused on the optimization of FA circuit for different applications in terms of PDP and 'transistor count' (TC). The optimization of FA in terms of PDP and TC can be achieved through the combination of various logic styles. The state-of-the-art energy-efficient FAs have been designed by combining the best features of conventional logic styles such as static 'complementary-Metal-oxide-semiconductor' (SCMOS), 'pass transistor' (PT), 'transmission gate' (TG) [18] [23], and 'gate diffusion input' (GDI) [14]. The conventional 28T CMOS adder is designed using SCMOS [23]. The 'transmission function' (TF) [2]-[3] and TG [19]-[21] FAs have been designed using TG logic. Both TF and TG FAs conceive a total of 16 and 20 transistors respectively. The PT-based FA reported in [24] consumes a total of 38T and is designed using 'complementary PT logic' (CPL). All other adders that were reported [1-3] [7]-[13] [16]-[17], [19]-[22] have been designed using a combination of SCMOS, PT, TG, and GDI logic styles.

The rest of this paper is organized as follows. Section-2 discusses the proposed FA circuit. Section-3 presents the simulation methodology and environment. Section-4 details simulation results and discussion. Section-5 concludes this paper.

2. PROPOSED 1-BIT FULL ADDER CIRCUIT

The proposed FA circuit shown in Fig.1 is derived based on Table.1. This schematic has *Sum* and C_{out} circuits. The circuit of Sum output is derived from the logic expression:

$$Sum = H \cdot \bar{C}_{in} + \bar{C}_{in} \cdot \bar{H} \quad (1)$$

where

$H = \bar{A} \cdot B + A \cdot \bar{B}$ represents an XOR operation of *A* and *B*. It is designed using GDI, SCMOS, and TG logic styles [13]. This Sum circuit requires only 14T.

Table.1. Truth Table of 1-bit Full Adder

Inputs			**Outputs**	
A	***B***	C_{in}	***Sum***	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The circuit of C_{out} is derived from Table.1, observing the C_{out} column and the input signal columns, the following logic equations can be derived:

if A=B=0, then C_{out} = 0.

if A=B=1, then C_{out} = 1.

if A=B (or H=1), then C_{out} = C_{in}.

Using the aforementioned concept, the logic expression for C_{out} is derived as

$$C_{out}=H.C_{in}+\left(\bar{A}\cdot\bar{B}\right).0+\left(A\cdot B\right).1$$

Based on Eq.(2), the proposed circuit for C_{out} has been derived using SCMOS and TG logic styles. The unique feature of the proposed circuit, C_{out} is that it requires only 8T, has rail-to-rail output, and good driving strength.

Thus, to implement the proposed 1-bit FA using the circuits of *Sum* and C_{out}, we need only 22T.

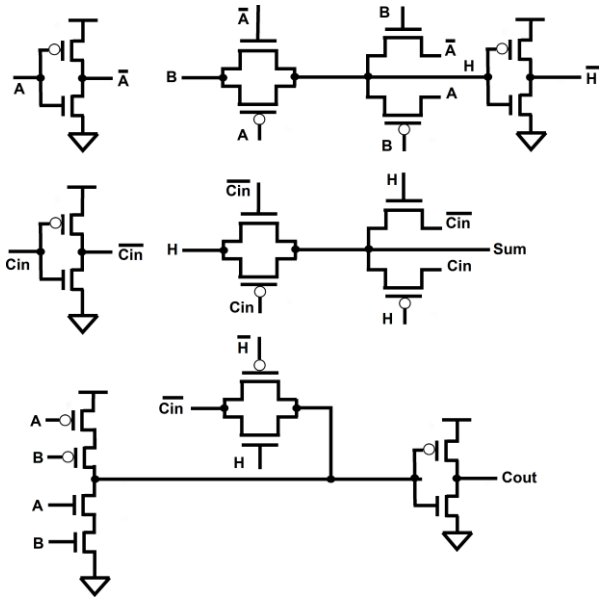

Fig.1. Schematic of the proposed 1-bit FA circuit

2.1. TRANSISTOR SIZING

To assess and compare the performance in terms of DMs. The schematics of the proposed FA and other reported adders have been designed using PTM 45 nm technology node with the minimum transistor channel length, L_{min}= 45 nm, and width, W_{min} =90 nm. Accordingly, for all schematics under consideration, the 'aspect ratio' (AR) has been chosen for n-channel MOSFET (NMOS) as $(W/L)n$=90nm/45nm and p-channel MOSFET (PMOS) as $(W/L)p=2\times(W/L)n$=180nm/45nm.

2.1.1 Test Bench and Simulation Environment:

To assess and compare the performance of the proposed FA with other adders, a common test bench shown in Fig.2 [11-12] is used. The Fig.2 consists of 'circuit-under-test' (CUT), input buffers, and output load capacitance. The CUT is a FA for which the DMs need to be extracted. The input buffers with the specified AR (numbers next to the inverter) are used to introduce the required signal distortion at the input of CUT. At the output, a load capacitance equivalent to 4 'fan-out inverters' (FO4), which is approximately equal to 6fF [12]-[13] is used. The 'average power dissipation' (APD) and 'worst case delay' (WCD) have been extracted using the standard test input patterns [21].

To extract the WCD, the maximum delay at each output of a CUT is first determined. Then, the WCD is taken as the maximum of the delays at *Sum* and C_{out}. To calculate, the maximum delay at each output, a total of 64 input vector to vector transitions ($ABC_{in}\rightarrow ABC_{in}$) are applied at 3 inputs of a CUT, where 'A' is the 'most significant bit' (MSB) and *Cin* is the 'least significant bit' (LSB) inputs. To generate these 64 transitions, an input signal frequency of 200 MHz with V_{dd}=1 V is used. Out of these 64 transitions, only 32 transitions are significant [16] and the remaining 32 transitions are insignificant. Among these 32 insignificant transitions, 24 transitions are represented as 'Not Applicable' (NA) and 8 are represented as *. For all insignificant transitions, there are no valid output transitions and hence there is no need to extract delay. Thus only 32 delays need to be extracted against all valid transitions at each output. In total about 64 delays need to be extracted at both outputs of a CUT. And the WCD of a CUT is selected as the maximum delay among 64 significant delays. For a proposed FA, about 64 significant delays have been extracted both at *Sum* and C_{out}, using the simulation results shown in the Fig.3. And the extracted results are tabulated in Table.2 and Table.3 respectively.

Further, to extract the power, the input signals with variable combinations of frequency are applied at the three inputs of a CUT. The frequency combinations for each input signal (f_{in}) is selected in such a way that it should include low frequency (f_l), medium frequency (f_m), and high frequency (f_h) signals. Thus, the fin is a concatenation of f_l, f_m, and f_h, where fin represents the input signal frequency of either '*A*' or '*B*' or 'C_{in}' inputs. The number of frequency combinations used is based on the pattern suggested in [19]-[21]. In this research the values of f_l, f_m, and f_h are chosen as 50 MHz, 100 MHz, and 200 MHz respectively with V_{dd}=1V. Thus, the APD of a CUT is the power dissipated over these combinations of frequencies. The simulated waveforms to extract the APD of the proposed 1-bit FA is shown in Fig.4.

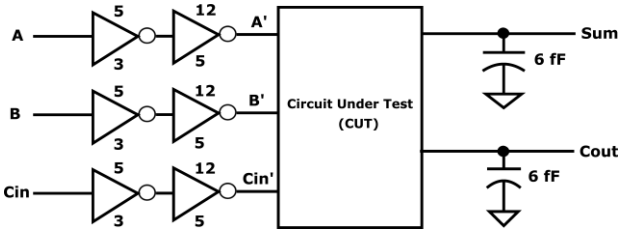

Fig.2. Test bench to extract DMs of proposed and reported FAs

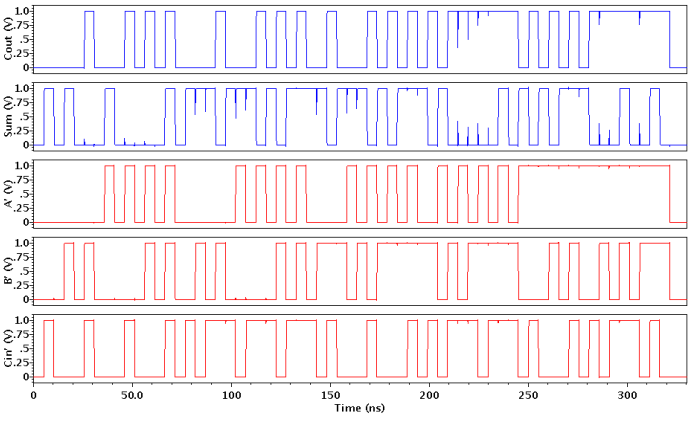

Fig.3. Simulation waveforms of the proposed 1-bit FA circuit to extract delay

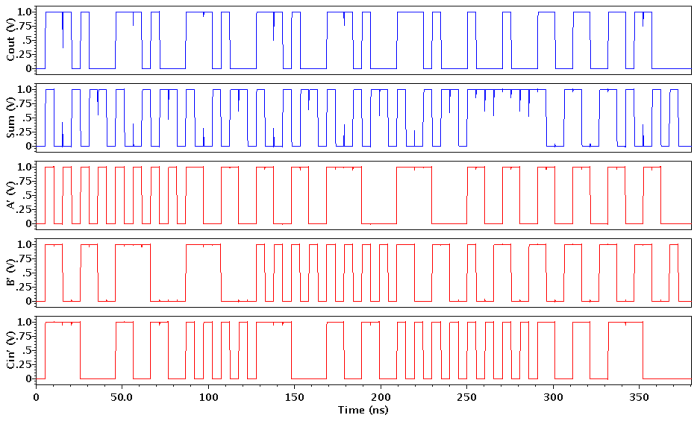

Fig.4 Simulation waveforms of the proposed 1-bit FA circuit to extract Power

Table.2. Extracted Delay of the proposed FA at output, *Sum*.

ABC	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
000	*	52	67	NA	87	NA	NA	53
001	41	*	NA	80	NA	95	58	NA
010	53	NA	*	75	NA	88	91	NA
011	NA	63	70	*	**131**	NA	NA	81
100	56	NA	NA	84	*	81	87	NA
101	NA	65	114	NA	71	*	NA	76
110	NA	96	81	NA	89	NA	*	53
111	44	NA	NA	79	NA	84	59	*

Table.3. Extracted Delay of the proposed FA at output, C_{out}

ABC	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
000	*	NA	NA	73	NA	85	61	61
001	NA	*	NA	87	NA	101	102	60
010	NA	NA	*	81	NA	**135**	67	53
011	57	58	71	*	55	NA	NA	NA
100	NA	NA	NA	123	*	85	68	56
101	59	61	55	NA	77	*	NA	NA
110	60	60	84	NA	96	NA	*	NA
111	60	60	64	NA	70	NA	NA	*

3. SIMULATION RESULTS AND DISCUSSION

This section presents the comparison results of the proposed FA and other reported adders in terms of their DMs. The comparison is carried out under two different simulation environments namely: i) Single-Cell ii) Multi-Cell environments. The DMs under consideration are delay, power, PDP, and TC. For a fair comparison, all FA schematics under consideration have been designed in Cadence's Virtuoso tool. The circuit simulations were conducted using Spectre simulator based on PTM 45 nm technology node. To assess the performance of all these FAs, the DMs have been extracted under common PVT conditions.

3.1. COMPARISON OF DMS UNDER SINGLE-CELL ENVIRONMENT

To compare the performance of the proposed FA and other reported adders under 'single-cell environment' (SCE), the DMs have been extracted using the test bench shown in Fig.2 and the same is tabulated in Table.4. The DMs of FAs that show best performance are highlighted in the bold text. The simulated input and output waveforms used to extract the DMs under SCE are shown in Fig.3 and Fig.4. The Fig.3 shows the simulated results used to extract WCD and Fig.4 is used to extract APD. From Table.4, the following inferences can be drawn:

Considering the APD column, the average power of the proposed FA is found to be 1.21 µW which is comparable with low power adders. This power advantage can be attributed to the underlying architecture of the proposed adder. The CPL (3.06 µW) and Hybrid3 (3.66 µW) FAs are found to dissipate the highest power. This is because the CPL requires more TC and Hybrid3 has more glitches in its outputs.

Considering the 'Delay' column, it is found that the WCD of the proposed FA is '135 ps' (Table.2 and Table.3), which is smaller and comparable among other reported lower delay FAs. This delay is due to the critical path that exists between the input signal '*A*' and output '*Sum'*. This delay occurs when the input signal vector ABC_{in} makes a transition from '010' → '101'.

From the PDP column, it is found that the proposed FA is having PDP metric of 0.156 fJ which is 4th lowest among all other FAs considered for the comparison. This PDP value is smaller and comparably larger than the other lowest PDP adders. The lowest PDP can be attributed to the low power and smaller delay features of the proposed adder.

Table.4. Comparison of DMs of Proposed and reported FAs under single-cell environment

Full Adder Circuit	**Average Power (µW)**	**Worst case Delay (ps)**	**PDP (fJ)**	**Area (TC)**	**Ref.**
CCMOS	1.16	111	0.129	28	[23]
CPL	3.05	173	0.530	38	[24]
TGA	1.28	138	0.177	20	[20]
TFA	1.14	155	0.177	16	[3]
HPSC1	1.32	123	0.162	22	[10]
HPSC2	1.44	124	0.178	26	[11]
DPL	1.31	149	0.195	28	[1]
SRCPL	1.40	138	0.193	26	[1]
Hybrid1	1.08	143	0.154	16	[7]
Hybrid2	1.51	165	0.250	16	[16]
Hybrid3	3.66	238	0.871	24	[12]
Hybrid4	1.15	136	0.156	22	[13]
Proposed	**1.23**	**122**	**0.156**	**24**	**-**

Again, from the TC column, it is found that the proposed FA has TC=22T, the advantage in less TC can be attributed to underlying logic structures. Considering the overall inferences, the PDP and TC of the proposed adder is found to be smaller and

comparable with other reported FAs. Though the CCMOS is having a smaller delay and PDP, it requires more TC.

3.1.1 Performance Comparison Under Scalable Supply Voltage:

This section presents the scalability of performance of proposed FA in SCE, under various supply voltages. To analyze the scalability of the performance, the simulations have been carried out by varying the V_{dd}, starting from 0.4 V to 1.2 V in steps of 0.2V. The extracted APD, WCD, and PDP are tabulated in Table.5 - Table.7 respectively. Since the CPL and Hybrid3 FAs fail to perform at the supply voltage 0.4 V and hence these two FAs have not been considered for the performance comparison. From these tables the following observations can be noted: From Table.5, Table.6, and Table.7, it is found that, all FAs except Hybrid3 and CPL demonstrate excellent performance scalability under various V_{dd} values.

- Considering Table.5, the APD of Hybrid1 FA under various values of V_{dd} is found to be the lowest as compared to other FAs. This advantage in power dissipation can be attributed to its underlying architecture and logic style used.
- Considering Table.6 and Table.7, as compared to other FAs the CCMOS shows excellent performance in terms of WCD except at V_{dd}=0.6 V and has the best
- PDP under various supply voltages except at V_{dd}=0.4 V and 0.6 V, but it has more area overhead in terms of TC.

The proposed FA exhibits the best and comparable performance in terms of DMs against the CCMOS and Hybrid1 FA. The area overhead of the proposed FA in terms of TC is less than the CCMOS and more than the Hybrid1 FA.

Table.5. Comparison of APD under scalable supply

FA	Power(μW)				
	0.4 V	**0.6 V**	**0.8 V**	**1.0 V**	**1.2 V**
CCMOS	0.145	0.34	0.654	1.161	1.878
TGA	0.166	0.396	0.764	1.284	2.072
TFA	0.142	0.346	0.671	1.142	1.845
HPSC1	0.144	0.428	0.765	1.32	2.202
HPSC2	0.169	0.396	0.795	1.44	2.36
DPL	0.163	0.407	0.778	1.31	2.13
SRCPL	0.174	0.422	0.818	1.4	2.3
Hybrid1	**0.139**	**0.333**	**0.636**	**1.08**	**1.727**
Hybrid2	0.141	0.366	0.754	1.514	2.934
Hybrid4	0.149	0.359	0.688	1.154	1.83
Proposed	0.151	0.364	0.707	1.21	1.99

Table.6. Comparison of WCD under scalable supply

FA	Delay(ps)				
	0.4 V	**0.6 V**	**0.8 V**	**1.0 V**	**1.2 V**
CCMOS	**1840**	251	**127**	**111**	**95**
TGA	2200	353	187	138	117
TFA	1950	364	202	155	134
HPSC1	1330	**209**	135	123	108
HPSC2	1340	212	152	124	110
DPL	3240	430	204	149	125
SRCPL	1900	298	178	138	120
Hybrid1	3330	440	207	143	114
Hybrid2	3260	464	243	165	131
Hybrid4	1936	343	182	136	116
Proposed	1938	323	177	135	116

Table.7. Comparison of PDP under scalable supply

FA	PDP(aJ)				
	0.4 V	**0.6 V**	**0.8 V**	**1.0 V**	**1.2 V**
CCMOS	266.8	85.34	**83.06**	**128.87**	**178.41**
TGA	365.2	139.79	142.87	177.19	242.42
TFA	276.9	125.94	135.54	177.01	247.23
HPSC1	**191.52**	89.45	103.28	162.36	237.82
HPSC2	226.46	**83.95**	120.84	178.56	259.6
DPL	528.12	175.01	158.71	195.19	266.25
SRCPL	330.6	125.76	145.6	193.2	276
Hybrid1	462.87	146.52	131.65	154.44	196.88
Hybrid2	459.66	169.82	183.22	249.81	384.35
Hybrid4	288.46	123.14	125.22	156.94	212.28
Proposed	292.64	117.57	125.14	163.35	230.84

3.2. COMPARISON OF DMS UNDER MULTI-CELL ENVIRONMENT

This section discusses the performance scalability of the proposed FA against the reported adders under MCE. It is noted from the state-of-the-art literature, many FAs that show excellent performance under SCE, failed to perform under MCE [12-13] [19]. To analyze this, the proposed FA and other FAs are embedded in a 64-bit RCA shown in Fig.5, and simulations were conducted under various supply voltages. And the extracted DMs against the simulations have been tabulated in Table.8. From this table, the following inferences can be noted.

- It is found that, among the 13 FAs, only the proposed and the other 2 FAs can operate in a 64b RCA chain without using any intermediate buffers.
- Among these 3 adders, only the proposed and CCMOS FA can operate and scalable their performance from V_{dd}=1.2 V to 0.4 V.
- The Hybrid4 FA, though it exhibits excellent performance in terms of delay and PDP as compared to the proposed FA, has failed to operate at V_{dd}=0.4 V.
- The CCMOS shows an excellent performance over the Proposed and Hybrid4 FAs, but has a large area overhead in terms of TC.
- The proposed FA has an excellent APD over Hybrid4 FA. It has a better performance in terms of delay as compared to CCMOS except at V_{dd}=0.4 V. Further it is more efficient in terms of TC as compared to CCMOS FA.

Thus, the proposed FA can be considered as a choice for energy-efficient and area-efficient VLSI applications, where

scalability in terms of supply voltage and input signal operand size are a paramount concern.

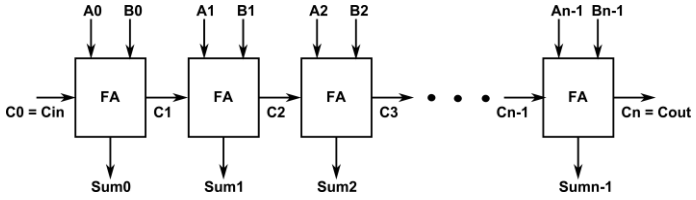

Fig.5. Test bench to extract DMs of Proposed and reported FAs under multi-cell environment

Table.8. Comparison of DMs of proposed and other adders operating in MCE using 64b RCA chain

FA/ V_{dd}	Hybrid4			CCMOS			Proposed		
	Power (µW)	Delay (ns)	PDP (fJ)	Power (µW)	Delay (ns)	PDP (fJ)	Power (µW)	Delay (ns)	PDP (fJ)
0.4	Failed			0.333	70.95	23.62	0.423	73.34	31.02
0.6	1.626	9.578	15.57	0.974	13.15	12.80	1.276	13.09	16.70
0.8	4.35	7.175	31.21	2.53	8.453	21.38	3.311	8.3	27.48
1.0	10.84	6.494	70.39	6.458	7.293	47.09	8.462	7.106	60.13
1.2	27.1	6.191	167.77	17.31	6.844	118.46	22.44	6.634	148.86
TC	1408			1792			1408		

4. CONCLUSION

This research paper presented a novel 22T 1-bit FA circuit. The proposed FA has been designed using hybrid logic styles such as GDI, TG, and SCMOS. The performance scalability of the proposed FA was compared and analyzed under a single and multi-cell environment, against other reported adders. The comparison was done in terms of DMs such as power, delay, PDP, and TC, under the single as well as multi-cell environments by scaling-down the supply voltage from 1.2 V to 0.4 V in steps of 0.2 V. All circuit simulation was carried out under common PVT conditions using Cadence's toolset based on PTM 45 nm technology. From the simulation results, it was found that the proposed FA can operate up to 0.4 V in a 64b RCA chain without using any intermediate buffers. Also, from the comparison results, it is found that the proposed FA has better and comparable performance under a single-cell environment, and excellent performance under a multi-cell environment against the reported adders. Thus, the proposed FA circuit can be considered as a choice for energy and area-efficient VLSI applications, where scalability in terms of supply voltage and input signal operand size are a paramount concern.

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