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ANALYSIS OF LOW POWER CONDITIONAL FLIP FLOP IN 32NM CMOS TECHNOLOGY FOR POWER CONSTRAINT AND SPEED SENSITIVE APPLICATIONS

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Abstract

In this paper, various conditional flip flops topologies are simulated in 32nm CMOS technology using BSMv4 model and compared on the basis of Power consumption, delay (Clk to Q) and Power delay Product. In Various designs of conditional flip flops, our main objective is to optimize the best design on the basis of delay and power. Simulation results showed that by using Pulse Enhancement Scheme (PES) in flip flop, power dissipation is reduced to 59.43% when compared with conditional feed through flip flop technique and further reduction of 43.34% was observed in delay at room temperature. On increasing the temperature PES technique still have less power consumption of 35.95% when compare to conditional feed through flip flop technique. It was also observed that PES technique can be used at lower voltage levels. So that dissipation and delay both reduced. In terms of delay among all designs, Single ended conditional capturing energy recovery (SCCER) has minimum delay of 2.4865ns at room temperature and 2.4843ns at 1.5V power supply. Power delay product (PDP) at room temperature of SCCER is 0.7177aJ. These results of flip flop using conditional techniques at different temperature consideration and at different voltage give us an idea to choose which scheme is better in terms of delay, power consumption and PDP.

Keywords:

Pulse Enhancement Scheme, SCCER, PDP, Power Dissipation

1. INTRODUCTION

Main objective of High-performance VLSI design chips is to reduce the power consumption and scaling down the device area based on Moore's Law [1]-[4]. With the advancement of CMOS technology, semiconductor devices and chips are becoming smaller and smaller day by day. The Very Large Scale Integration (VLSI) low power designs are categorised as: analysis and optimization [5]. Analysis being related to the calculation of energy and power dissipation at different stages of design. The precision of analysis depends on utility of design information. Optimization is the method of creating the best design, without disturbing the specification of design. It should also be noted that delay affects the speed and performance of chip which is directly proportional to the cost of manufacturing. With progressive evolution of high performance VLSI SOC designs, power dissipation is major issue in modern chips. Mostly consumption of power is due to the clock and the latches used for storage of data. It can be reduced by using innovative clocking techniques for low power design [5]. Flip Flops are the basic building blocks to store the data. Latches and flip flops dissipate 80% of total clock power [6]. Pulse flip flops are mostly used in high-speed application due to their simple structure in comparison with master slave flip flop [7] [8]. Therefore, performance can be improved by improving the characteristics of flip flops. Among the various techniques available for low power design some Conditional Techniques are analysis here:

Techniques such as conditional recharge, conditional discharge, conditional capturing and conditional data mapping applied earlier but suffered from speed degradation[9]-[12]. Dashan pan [13] proposed pulse flip flop using energy efficient conditional feed through with shared pulse generation. The delay (*Clk* to *Q*) is reduced by balancing rising and falling output edges and reduction in internal power consumption by using output controlled storage node keeper.

The average power consumption is given by [14]:

$$P_{avrg.} = P_d + P_{Short} + P_{Leak} \quad (1)$$

where,

P_d = Dynamic power

P_{Leak} = Leakage power

P_{Short} = Short circuit power

In CPSLFF [14], sources P_d and P_{Leak} are main dominant factors for power dissipation. Various solutions have been suggested to reduce the switching activity of transistor which helps to reduce both types of power dissipation and also the number of transistor for silicon area.

As a consequence, large transistors of pulse generator logic used to assure that the pulse has sufficient width to trigger the data capture of flip flop [15], this may enlarge the problem in large capacitive load. Author [15] present a conditional pulse enhancement scheme(PES) which increase the number of transistor, transistor of pulse generator logic benefit from size reductions and whole area even slightly reduced which results in slight rise in power with temperature rise and PDP against other.

Energy Recovery and clock gating [16], can achieve low energy dissipation by stopping the current to flow from device with low drop of voltage. Clock gating solutions are provided for energy recover clock. Applying energy recovery technique at internal node is quite risky because of short circuit power within the flip flop.

In this paper, section 2 describes all these conditional technique of flip flop and their working. Section 3 shows the simulation and results of all four conditional flip flops with fair comparison at different temperature and different voltage level. Section 4 gives the conclusion of the paper which gives us an idea of choosing flip fop at different conditions.

2. DIFFERENT CONDITIONAL TECHNIQUE FLIP FLOP

2.1 CONDITIONAL FEED-THROUGH PULSED FLIP FLOP

In conventional pulse flip flops, large delay (low to high) due to unbalanced pull down and pull up paths by which needless

internal switching node changing input data results in decreasing energy efficiency of chip. Dashan Pan [13] proposed a design and addressed with two issues parallel. First is to reduce the number of transistor stacking in pull down path and second is that to add MP_4 and MN_4 (additional paths added). *D* to *Q* latency can be reduced further by complementary conditional signal feedthrough scheme (as shown in Fig.by red circle). Some points are given below to show how proposed design offers more advantages as compare to existing designs. They are:

- MN_3 known as data controlled discharge transistor is connected near to ground than MN_1 known as clock controlled discharge transistor. These rearrangements of stacked discharge transistors reduce the *D*-to-*Q* delay.
- MN_7, MP_7, MN_8 and MN_9 transistors i.e. output controlled transmission gate allows input data to directly feed to the output.
- To enhance design driving capability, internal node controlled i.e. MN_4 transistor and pulse clock controlled i.e. MN_2 transistor connected.
- Along with clock mesh to reduce the clock power and area, a shared width programmable pulse generator used.

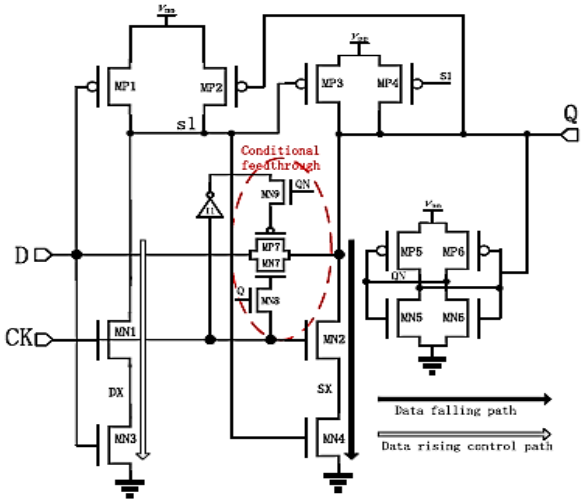

Fig.1. Pulse flip flop (PP) [13]

The working of this proposed design is described as:

- When input *D*=0, *clock*=0 and *output*=0. Node S_1 becomes 1 due to MP_2. MP_3, MN_2, MN_8, MN_1, MP_4 are turned off. Node *SX* and *DX* becomes 0 by MN_3 and MN_4, while MN_6, MP_6, MN_5, MP_5 secure the value of Q. When positive edge applied, MN_9, MN_1, MP_7, MN_2 switched on. Input directly fed output *Q*. Node S_1 is parallel discharging through MN_3 and MN_1. Due to delay, by time MP_7 switched on, and MN_4 has been switched off. This ignores the direct current from *Q* to 0. MP_3 and MP_4 are switched on, and node *Q* level suddenly enhance.
- When *D*=0, *clock*=0 and *output*=1. Node S_1=1 by MP_1. Then MN_4 switched on to pre discharge *SX* to 0. When positive edge of clock comes, MN_2, MN_8 and MN_7 are switched on and node *Q* suddenly discharged to 0.
- When *D*=0, *clock*=0 and *output*=0. Internal node S_1 switched 1 by MP_2 and MP_1. MN_4 switched on to pre discharge *SX* to 0. When positive edge of clock arrives, MP_7, MN_2 and MN_9 are switched on and output *Q* remains at 0.

Output showed a small screw at balance rising and falling edges. In high speed applications, using mesh method a distribution network of low skew and low latency were implemented. This permits for distinguish and share of pulse generator.

2.2 CONDITIONAL PASS TRANSISTOR LOGIC STATIC D FLIP FLOP

Murugasami [14] proposed a CPLSDFF design. In this design, after triggering state of internal node X_2 depend on both input and feedback from intermediate node X_2. This architecture employs the single phase of clock input signal whereas previous designs consist of master and slave phase with intermediate dissimulate dynamic node and a static output node.

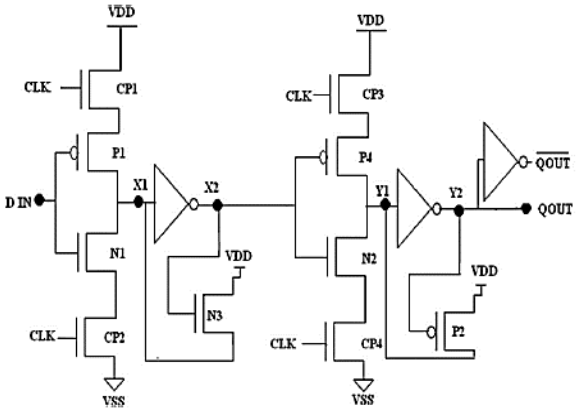

Fig.2. CPLSDFF [14]

The intermediate state nodes Y_2 and X_2 is maintained with weak P_2 (PMOS) and N_3 (NMOS) transistors respectively. In this, only 1 transistor in each stage is used when compare with existing circuits where 4 transistors are used in each stage of flip flop results in increasing of the chip area. Similarly, by removing unnecessary switching at power can be reduce, when X_1 node is at 0 and clock at 1 as well as clock at high and inverted output also at high in master stage. It averts the charge sharing in both stages.

Working of this proposed design as given below:

- When *D* is 0 and clock is 1, node X_1 becomes 1. Conditional transistor (CP_1) and PMOS transistor (P_1) makes node X_1 pre charged to high. When *D* is 1 and clock is also 1, conditional pass transistor (CP_2) and NMOS transistor (N_1) maintain the node X_1 in evaluation phase and X_2 at 0. As more one than NMOS are connected in series, there is no direct charge leakage. If the node X_2 is at 1, it will switch on N_3 (NMOS) and make X_1 dynamically 1 and then X_2 change from 1 to 0. Similarly, if node X_2 is at 0, it remains at same level. No unnecessary switching and charge leakage occurs in this. Proposed circuit has only 1 transistor in charge keeper circuit which helps to save power and area due to less number of transistors in the path. In clock network, number of transistor count is 4 which is also less as compare to previous designs results in less load on clock network power.

- When D is 0 and clock is 1, node X_1 becomes 1 and X_2 at 0. P_4 (PMOS) drived by X_2 node and turn it on and conditional pass transistor CP_3 (NMOS) make the node Y_1 at 1 and output node Y_2 to 0. This keep the output of flip flop Q_{out} in 0 state.
- When D is 1 and *clock* is 1, node X_1 goes to precharge and X_2 at 0. This turn on the P_4 (PMOS). Conditional pass transistor (CP3) turned on as clock is at 1, gives internal node Y_1 to 1 and static output node Y_2 to 1. This maintains the output of flip flop Qout in 1 state.

Number of transistor turned on by clock are 4 compared with 8 in previous design. As results in proposed design, net critical path switching of transistor is (Ts=12) when correlate with input D is kept at either logic 0 or 1. (Ts=18)

2.3 CONDITIONAL PULSE ENHANCEMENT SCHEME IN PULSED FLIP FLOP

Hwang [15] describes about the pulsed triggered flip flop using conditional pulse enhancement scheme which helped to reduce the number of transistors in discharging path. Secondly it also conditionally increases the pull down strength when input D is at high. Two NMOS N_2 and N_3 of Pass transistor Logic (PTL) style AND gate are used to control the discharging of transistor. Inputs to both of these transistors are complementary which maintain the output Z at low level most of the time. In his design, when Data is high, while Q_{bar} output is high, longest discharging path formed. PMOS Transistor P_3 is added to enhance discharging under this condition. Internal node X most of the time turns at 1. So, P3 normally at off condition. When intermediate node X is discharge to threshold voltage below supply voltage, it will provide boosting to internal node Z. The generated pulse is taller, which increase pull down strength of NMOS N_1.

After positive edge of input clock, delay of inverter I_1 drive the internal node Z reverse to 0 through NMOS transistor N_3 to close the discharging path.

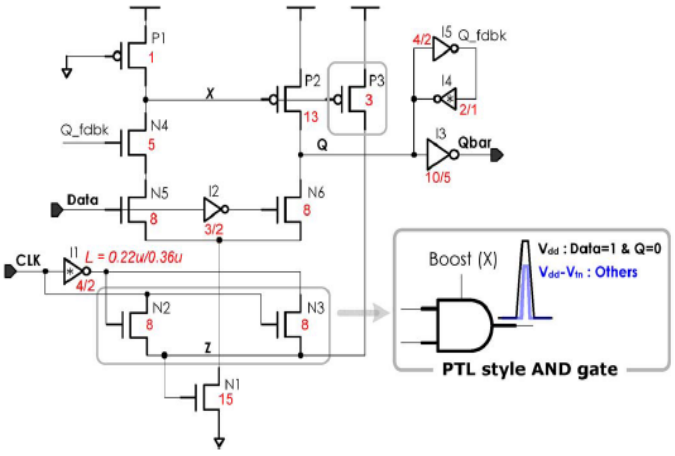

Fig.3. Pulse flip flop using PES [15]

The internal node X voltage level rises and switched off the PMOS transistor (P_3) at the end. With the interference of PMOS transistor (P_3), width of proposed discharging pulse is stretched out which means to make a pulse with sufficient width to collect data correct capturing. So that a stacked inverter designs takes more power consumption not necessary in pulse generation. It is noted that when flip flop output change from low (0) to high (1) then only pulse enhancement scheme effective. Advantages of using this scheme are to reduce the power due to shrunken transistor in discharging path and in delay inverter.

2.4 CLOCKING SCHEME USING ENERGY RECOVERY AND CLOCK GATING IN FLIP FLOP

Mahmoodi [16] describes Energy recovery and clock gating are the techniques for decreasing the clock power. With this technique, we can achieve low energy dissipation by stopping the current to flow from device with low drop of voltage. Clock gating solutions are provided for energy recover clock. By applying the proposed clock gating technique, power reduces by 1000 x in sleep mode operation. Some added feature in flip flop has only negligible power and delay when flip flop is in active mode.

Best way for energy recovery clocked flip flop is to generate square wave clock from sine wave clock. In this, extra energy is required. Applying energy recovery technique at internal node is quite risky because of short circuit power within the flip flop. By considering these entire factor, author designed energy recovery from clock input capacitance only, other things i.e. internal node and flip flops are powered by constant supply.

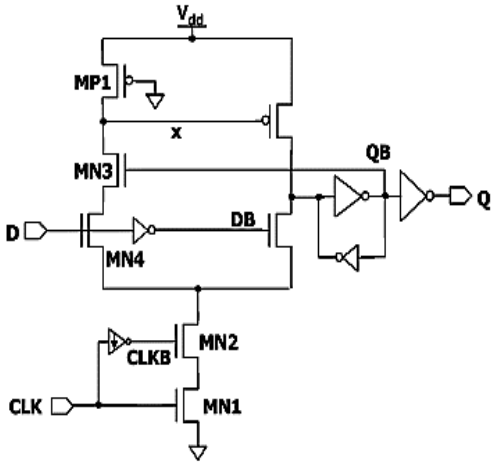

Fig.4. SCCER flip flop [16]

It shows a single ended conditional capturing energy recovery (SCCER) flip flop. As the name indicate only for a single side conditional capturing used and on other side (right hand side) evaluation path is static, so don't need conditional capturing. NMOS (MN_3) transistor providing the conditional capturing as its gate is connected to the output QB.

By placing the MN_3 before MN_4 in the arrangement reduce the charge sharing. MN_1 and MN_2 both are connected to *CLK* and *CLKB* respectively. Serial combination of these stack transistor operate for a short period of time during positive edge of clock when both *CLK* and *CLKB* signal voltage above threshold voltage of NMOS transistors. Conducting only at positive edge of clock, not on negative edge of clock because clock inverter is skewed for high (1) to low (0) level. Cascading of one inverter instead of three inverters, gives reduction in power and delay. The static nature tells that their internal node statically maintain the states of flip flop, if data remains constant. PMOS transistor (MP_1) is used to

pre charge the internal node. A feedback path is provided at the output of flip flop. It exhibits smallest minimum Data- to- output delay.

3. SIMULATION AND RESULTS

In this section, analyzing the performance of different conditional flip flop at 32nm CMOS library of BSIM4v45 model and comparing the parameters of each design at different supply voltage and various temperatures. The testing and simulation are processed in the Tanner EDA tool of version 2019.2.

Powers at different temperatures and at different V_{dd} are calculated for comparing the different existing design. Power calculation is done by using the T spice code report generator. The clock frequency was 33.3 MHz with a rise and fall time of 50ps for each. The data used for simulation is of 12 bit (110011100011) with a rise and fall time of 50ps each.

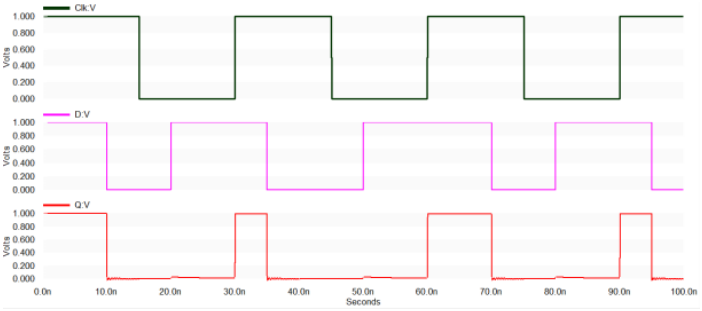

Fig.5. Output waveform

3.1 POWER ANALYSIS

In the given below table as it is shown the comparison between different existing proposed designs. The Table.1 represents the power consumption of different design at different temperatures and Table.2 shows the power at different voltage supply. With this calculation of power, we can choose which design work better at maximum high temperature with minimum dissipation of power. It also shows the variation of voltage to judge which design behave perfect at low voltage.

Table.1. Temperature vs. power (in uW)

Design	Temp (˚C)				
	25	35	45	55	65
PES [15]	24.5368	26.3805	27.8248	28.667	30.4373
SCEER [16]	28.8677	30.4946	32.9373	32.9905	33.1783
CPLSDFF [14]	42.6876	41.2257	39.2683	37.7102	36.2786
PP [13]	60.4858	57.389	52.8824	50.3573	46.7961

As shown in the Table.1, Pulse Enhancement Scheme (PES) [15] has minimum dissipation of average power among all other designs at room temperature. As we increase the temperature, dissipation increases but still it is better in case of Pulse Enhancement Scheme (PES).

The Table.2 shows that at a supply voltage of 0.7V, minimum dissipation of power occurs which support designs to use for low power applications.

Table.2. Voltage vs. power (in uW)

Design	Temp (˚C)				
	25	35	45	55	65
PES [15]	6.7084	14.7824	39.7951	144.961	607.457
SCEER [16]	10.0233	19.6277	45.1426	137.394	538.461
CPLSDFF [14]	9.627	28.7774	60.9094	109.511	185.061
PP [13]	8.1595	31.6494	102.282	240.982	545.710

3.2 DELAY ANALYSIS

The delay of different designs calculated which shows how much time is taken to change the state of output w.r.t data.

Table.3. Temperature vs. delay (in ns)

Design	Temp (˚C)				
	25	35	45	55	65
PES [15]	42.4858	42.4864	42.4868	42.4875	42.4879
SCEER [16]	2.4865	2.4869	2.4873	2.4878	2.4882
CPLSDFF [14]	85.1029	85.1052	85.1074	85.1091	85.1108
PP [13]	74.9969	75.0018	74.985	75.0021	75.0088

In Table.3 it is clearly showed SCEER has minimum delay even on increase of temperature delay slightly increased only.

Table.4. Voltage vs. delay (in ns)

Design	Temp (˚C)				
	25	35	45	55	65
PES [15]	42.4994	42.4887	42.4843	42.4876	42.4851
SCEER [16]	12.4965	12.4877	2.4843	2.4873	2.4843
CPLSDFF [14]	86.2118	85.22	85.0457	85.0073	85.0042
PP [13]	85.0368	74.985	74.9887	74.9764	74.9764

On increase the power supply voltage clock to *Q* delay increases. Minimum delay can be seen at 0.7V in SCEER [16] design. In case of PP [13] flip flop, delay decreasing as we are going to high supply voltage which implies it is better to use this technique [13] where high supply voltage is required. In Conditional Pulse static D flip flop *Clk* to D delay decreasing on increasing the power supply voltage.

3.3 POWER DELAY PRODUCT (PDP)

Power delay product is the product of power and delay. The Table.5 shown below indicates that SCEER has minimum PDP of 0.7177 at room temperature.

Table.5. PDP vs. Temperature

Design	Temp (˚C)				
	25	35	45	55	65
PES [15]	1.0424	1.1208	1.1821	1.2179	1.2932
SCEER [16]	0.7177	0.7583	0.8192	0.8456	0.8255
CPLSDFF [14]	3.6328	3.5085	3.342	3.2094	3.0877
PP [13]	4.5362	4.3042	3.9653	3.7769	3.5101

Another PDP vs. voltage shown in Table.6.

Table.6. PDP vs. Voltage

Design	Temp (˚C)				
	25	35	45	55	65
PES [15]	0.2851	0.628	1.6906	6.159	25.8079
SCEER [16]	0.1252	0.2451	0.1121	0.341	1.3376
CPLSDFF [14]	0.8299	2.4524	5.18	9.3092	15.731
PP [13]	0.6938	2.3732	7.67	18.069	40.915

4. CONCLUSION

In this paper, various conditional techniques flip flop are simulated at 32nm CMOS technology on T Spice. On the basis of results obtained, we can conclude that PES has minimum power dissipation but with increased transistor count. On terms of delay, SCEER has minimum *Clk* to *Q* delay of 2.4865ns at room temperature. Lesser the amount of delay more is the benefit for high speed applications. It also have minimum PDP which is 84.178% reduced as compared to PP design. This showed that at low power supply CPLSDFF has minimum power dissipation but maximum delay.

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