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CMOS BASED DRIVER TREE DESIGN FOR MICROPROCESSOR CLOCK DISTRIBUTION UNITS IN BIOMEDICAL IMAGE PROCESSING CIRCUITS

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Abstract

The transmission of clock signal is done across the integrated circuit in the presence of buffers and wires in synchronous biomedical systems on-chip architectures. This paper presents the investigation of the driver tree architecture to be used in microprocessor and DSP processors for biomedical image processing applications for clock distribution. In system on chip architecture this design plays an important role. Several clock distribution units like parallel, H-Bridge configurations were implemented in past. A new buffer is designed for the improvement of driving capability in clock distribution. This paper presents the CMOS based clock distribution circuit with better power and drive current. The parameters like power and current are investigated. Predictive technology models for CMOS 90nm technology are used.

Keywords:

CMOS, Current Driver, Clock Driver, H-Bridge, Buffer, Power

1. INTRODUCTION

The basic building blocks in FFT algorithms include the DSP based system like voice recognition, digital image (HD), receiver filter applications, radar-sonar signal processing and analyzing. The process that we do in mobile communications contains DSP within it along with FFT blocks. Similarly the FFT architectures were used by ECG, EEG, MRI, CT scan etc.

These applications can be employed to observe and study about the audio, video, sensor output, data from the web and all type of information. Thus processing information with the help of discrete Fourier transforms are helpful in the observation of the frequency components of a signal. 1-D (audio, sensor output) and 2-D (images and video) signals can be processed in DSP [1]-[2].

These FFTs forms the basic blocks of digital biosignal processing circuits. The signals from the different parts of the IC are synchronized by the clock signals. There occurs mismatch in clock arrival time due to the interconnect impedances. These mismatches results in clock skews.

Clock jitter are the noise in the clock signals that arises due to various reasons in the circuit. The clock distribution network must be designed in such a way to eliminate the clock skews and clock jitters. The construction of clock networks can be accomplished by various methods such as H-tree, buffered clock trees and meshed clock network. The speed of the system is determined by the physical composition, temperature and path length of the network.

2. LITERATURE SURVEY

The major part of power consumption is consumed by clock distribution network (CDN) due to its higher activity factor on chip [3]-[5]. Leakage current, short-circuit current, dynamic switching in parasitic capacitors are the different factors that affect the power consumption [6]-[8]. Among them dynamic switching power consumption is the main factor [9]-[11].

By reducing the capacitive load (C), power supply voltage (V_{dd}) and switching frequency (f) the power consumed in switching can be reduced [12]-[14]. The sub-threshold conduction caused leakage currents. Based on the supply voltage and frequency of operation the power consumption can be increased leading to the overall increase in power consumption.

3D ICs were implemented and the clock distribution circuits were different. The current driving capacity of the circuits is higher for biomedical applications. The current required by biomedical application is organ dependent [16]-[17]. The circuits show different characteristics so amplifiers can be adopted [18]-[19]. In future FinFET based circuits will replace the CMOS circuits but it depends once again on the biomedical application [20]-[22].

3. BACKGROUND METHODOLOGY. CLOCK DISTRIBUTION NETWORKS

For designing the clock distribution network the design methodology and the structural topology are to be considered for the development of system. The speed of the system, die area and power dissipation are influenced to a certain extend in the design of clock distribution network.

3.1 METHODOLOGIES

In buffered clock distribution the relative phased between the two clocking element is crucial, whereas in achieve zero skew routing the clock edges will arrive at a same time as the colock route to destination

The Fig.1 shows the types. In **s**ingle driver type the interconnect resistance of the buffer at the clock source is less when compared with the buffer output resistance. The signal should have short transition times. Delay computation should be done for delay paths and that has to be balanced. In convention driver methods the major drawback is its increased delay and

lower drive capability. The paths can be balanced by applying equipotential clock distribution with the help of buffered trees. Also the addition of buffers at either clock source or along the path of formation of tree structure may be advantageous. In clock signals the distribution of buffers are used in double function of amplifying it. The design methodology includes Analysis of capacitance in all node, Resistance should be checked in all branch, the buffer load must be fixed and the buffers must be positioned optimally.

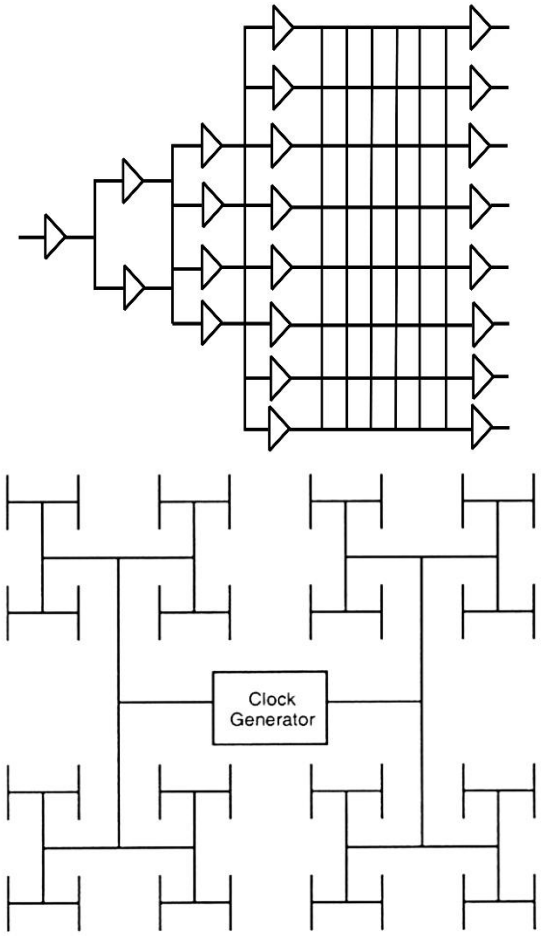


Fig.1(a). Buffered Clock Distribution Network and (b) H bridge network

3.2 H-BRIDGE CLOCK DISTRIBUTION

If there is no clock skews then the CDN increases. The route lengths are increased by the application of delay matching in case of delay occurrence. This also leads to complicated circuit design. By the use of series H-shaped routes from the centre of the chip as shown in the Fig.4 a zero skew clock routing can be achieved. When scaling the interconnect impedance the reflections are minimized at every junction.

4. DESIGN OF CMOS DRIVER STRUCTURES FOR PROCESSORS

For biomedical signal processing units, Fast Fourier Transform (FFT) architecture usage of buffer plays a significant role in the functioning block of FFT. The FFT architecture had used buffer of 3 category types namely, Input buffer, Delay buffer and Output buffer respectively. These Buffers differs with their processing styles such that FFT block inputs are obtained from input buffer. Then Input of FFT block are passed to output buffer where it can process fanouts (group of outputs) and stages. The Delay Buffer was placed in the processing function blocks done at Fast Fourier Transform architecture.

The Designing of digital circuits such as clock and flops/latch places major responsibilities at output design where these leads to a parameter analysis namely, speed, dimension, area, power to efficient one. The Main purpose of clock was to make link with signal also with its time. Based on the hold state nature of clock roles of latches/flip flops determined. The Usage of clock may leads to lowering overhead at latch/flop and clock skews. The Clock has two state namely Low state was used on functioning with latch because it data stored at flow and High state where data of flipflop are stored. The Delay parameter will be same for every path and the stage in storing data in the gates and the wires at that stage used by clock was eliminated. The wave pipelining was done where signal relates with clock. The System are stored at signal but not processed because of practical difficulties. The Structure design of signal are done from successor to predecessor for rapid functions and 2 latches are connected back to back flip flop was constructed but clock delay across it can slower down the paths. In clock distribution consists of 2 issues namely, 1) latch/flip flop delay and 2) clock skews but in latch/flip flops delay will be approximately be 1.5 FO4. If two latches per cycle was higher than 15% of a cycle at that case clock skews are constant in pc be harder at weaker cycle timings. A Radical approach was used when design complication of clocks gets higher. Local information can adopted and sequence of collected data about bundled state with signals are known as self-timed design.

The Usage of clocks local information to sequence the data are done because where a circuit can process by its own speed level. The Analysis of input values and next state logic stage of sequence be done with pipeline logic. By using this clock local information can leads to a further faults and then decision authority comes under local information. At that case it enters a process with maximum delays, higher timings, larger in area, more in power consumption at the transfer of decisions to logic gates. In order to hide that parameter such as delay matching approach was utilized son that status quo will present for a sometimes. The skew effect on clock distribution can be lowered by minimizing skew which reduces buffer and wire delay but particular levels delay can't be minimized. In that case delays are tuned low to balance the delay at every path but escapes from total delay problem and captured at matching problem. The parameter such T should be small when compared to T_{drive}. The Technique called clock trees can reduce skews. The Chosen delay was matched with various branches of trees. This Efficient result can be obtained when buffer and wire delay gets matched with skew value of zero.

For the preservation of area, a delay buffer of the memory module is added in form of SRAM cell within the input/output data bus. A unique read/write circuitry is designed as a sense amplifier for doing operations in high-speed and low power consumption. The whole memory cell can be described in two words. The first one is the written input data and the other was the

read output data. The whole memory cell are consuming most of the power which seems to be power consuming and inefficient. The memory elements were grouped into blocks. Clock tree technique is used in memory module of delay buffer. The elements in the each memory blocks are linked with one of the output which is used as a read-out memory words.

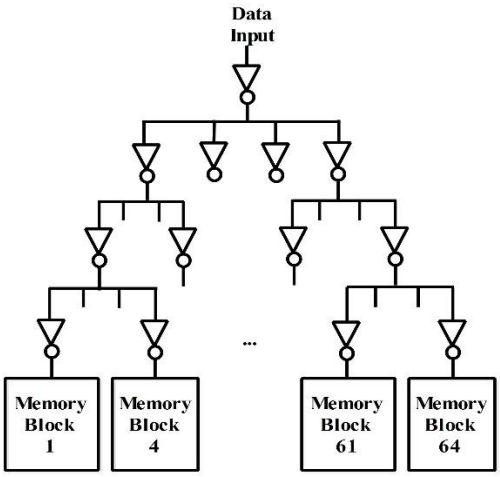


Fig.2. Architecture of the distribution unit

The input word to the memory word can be distributed by using the tree-structured hierarchy of tri-state inverter illustrates in Fig.2 and then it shows one input bit were only the driver tree. The loading of the input write circuitry can be estimated, it is

$$N \times L_{Latch} + \frac{4}{3}(M-1) \times L_{Tri} \quad (1)$$

where, L_{Latch} refers to parameter which loads of the one latch and L_{Tri} parameter refers to i^{th} buffer.

While loading state logarithmical decrement occurs at that case consumption of power gets lowered. So that driving capability of a circuit at simulation for buffer sizing should be enclosed for extra loadings.

The Fig.2 was same as that of circuit in output sensing circuit but it has a reversed signal flow direction. The Passed levels of buffer via addressed memory element acts as multiplexer. The variable length delay buffer and alternative signals paths are chosen at multiplexers are then enclosed with it. On Other side are placements of buffers at clock/driver tree of the control signal. It also enclosed with I/O driver trees and latches to get an entire setup of delay buffer with variable length and then it was made to implement at hardware related to a maximum length. The Proposed Method was designed with delay buffer and simulated by using 90nm CMOS technology.

A Standard 6-T SRAM cells has been used at delay buffer. Eight DET flip-flops, eight memory words and also with control logics are used at structure. The Proposed system can be simulated with different lengths on same CMOS technology. It uses 8bit word length and parameter such as layout, dimensions, power which are evaluated and then compared with commercial SRAM compiler with same technology values at each clock cycle. The operational parameter should include with one to read and another to write operations for the *N* length delay buffer or sometimes used for one two-port SRAM with *N* words or two one-port SRAMs of everyone with *N*/2 words

5. RESULTS AND DISCUSSION

For the implementation of the driver tree, the proposed buffer with different values in each stage for the Gated Driver tree for FFT architecture is done. The implementation carried out in standard cells of 90nm CMOS technology. The simulation and experimental results are shown below. The designed buffer is shown below in Fig.3. Predictive technology models were used for the implementation of the circuits.

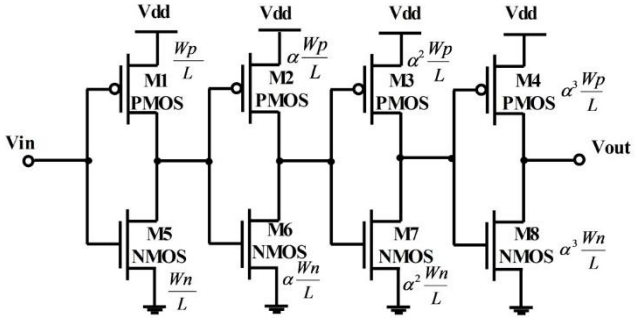
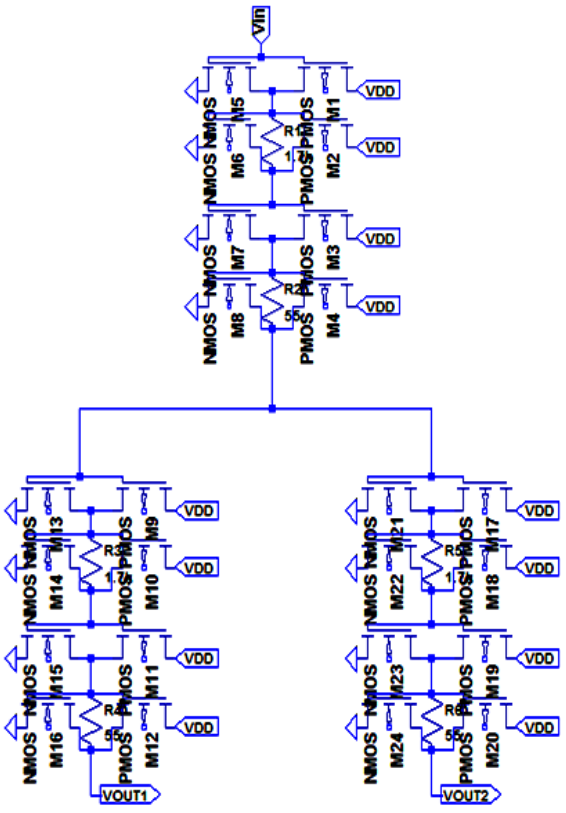


Fig.3. Proposed buffer circuit

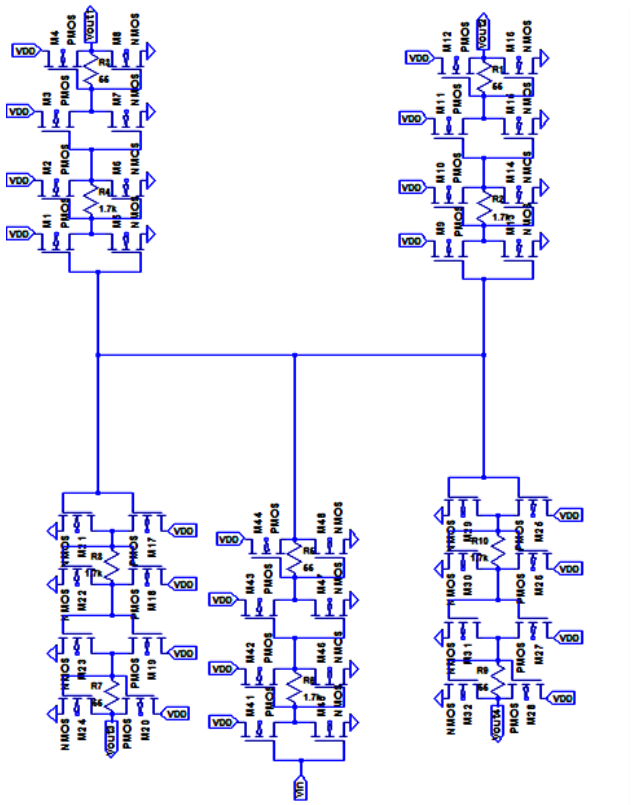
The designed buffer with α value is 3.68 and Rf_1=1.7kΩ, Rf_2=55Ω.

Table.1. Parameters of PMOS and CMOS

PMOS	M_1	M_2	M_3	M_4
W/L	180n/90n	660n/90n	2400n/90n	8900n/90n
NMOS	M_5	M_6	M_7	M_8
W/L	90n/90n	330n/90n	1200n/90n	4400n/90n



(a)



(b)

Fig.4. Proposed buffer circuit in clock distribution unit (a) clock tree (b) H-Bridge

Table.2. Results of Tree (Fig.4(a))

V_{in} (V)	V_{out1} (mV)	V_{out2} (mV)	Average Power (mW)	Peak Power (mW)	Average Current (mA)
0	567	567	19.4	19.5	0.701
1	595	595	19.3	19.4	0.702

Table.3. Results of H-bridge with proposed buffer (Fig.4(b))

V_{in} (V)	V_{out1} (mV)	V_{out2} (mV)	Average Power (mW)	Peak Power (mW)	Average Current (mA)
0	590	590	33	33	1.3
1	592	592	34	34	1.4

6. CONCLUSION

The paper presents the design of a clock distribution unit using clock tree and H-Bridge circuit. The average power and current are measured and plotted. The clock tree circuit using bridge architecture is designed and implemented using proposed circuit. From the analysis it has been found that for the clock tree the power consumption is less in but current driving capacity is higher for H-bridge circuit. Both simulation and experimental results shows great improvement in power consumption.

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