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# A COMPARATIVE EVALUATION AND ANALYSIS OF D FLIP FLOP FOR HIGH SPEED AND LOW POWER APPLICATION

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***Abstract***

***This paper presents comparative analysis of various flip-flops in CMOS technology. We simulated dual dynamic node hybrid flip flop (DDFF), Hybrid latch flip-flop (HLFF), Modified hybrid latch flip flop (MHLFF), and modified transmission gate flip flop (TGFF). The average power of various flip flops are calculated at 0%, 25%, 50% and 100% data activity, at temperature 25-100 ºC and different voltages 0.7, 0.9, 1 and 1.5. The average delay is also calculated at room temperature. All of these parameters are calculated in 32nm CMOS technology with the help of TSPICE. It was observed that MHLFF is the flop-flop that consumes less power compared to other flip flops. We are comparing performance and power dissipation and also compared transistor count of each flip flop.***

***Keywords:***

***Average Power, Data Activity, Transistors, Average Delay, Edge Triggered Flip Flop***

## 1. INTRODUCTION

In present scenario, technology is moving forward day by day from low to high scale [1]-[3]. In VLSI circuits, power consumption is the most valuable factor for low-power application. To minimize the power, optimization at the logic level is most important task. Logic components, flip flops and latches are critical for the performance of digital system [4]-[5]. D type flip flops are generally used in test applications and memory designs [6-7]. In electronics, chip size reduces due to remove the unnecessary transistors for reduce the weight and size of equipment. The hundreds of millions of transistors are present on a single chip to integrate the system on chip (SoC) design. Where cooling and packaging only have limited ability to remove excess heat [8]. So heavy amount of heat should not be dissipated. The low power design is also needed for laptops, mobile phones, calculators, wrist watch etc. The life of battery is main factors in low power [9]. Flip flop is one type of basic storage element that used extensively in all type of digital designs.

In edge triggered change the states either at positive or negative edge of clock pulse on the control input. When changes the state at positive edge that will be rising edge and at negative edge that will be falling edge.

In this paper, we are simulating various D flip-flops and comparing the performance of flip flops at different data activities and at different voltage level [10]. The operation of a D flip flop is not complicated. It is easier than other flip flops. D flip flop has only single input addition to the clock. This is very helpful when single bit data to be stored and data would be 0 or 1. When clock is applied there is HIGH on the D input, then flip-flop stores and SETs a 1. When clock is applied there is LOW on the D input, then flip-flop stores and RESETs a 0.

Here we have four circuits simulated with the fair results. All these circuits are Dual dynamic node hybrid flip flop (DDFF), Hybrid latch flip flop (HLFF), modified hybrid latch flip flop (MHLFF) and modified transmission gate flip flop (TGFF).

Whole paper contains in four parts. First part introduction already discussed. In second part, we are discussing about the working of all these flip flops. In third part we discussed simulation and comparison results and in last part discussed conclusion.

## 2. ANALYSIS OF FLIP FLOP ARCHITECTURE

In this section, we are explaining the working of all flip-flops. We have simulated D flip flop in different architecture and using 32nm CMOS technology for all.

### 2.1 DUAL DYNAMIC NODE HYBRID LATCH FLIP-FLOP

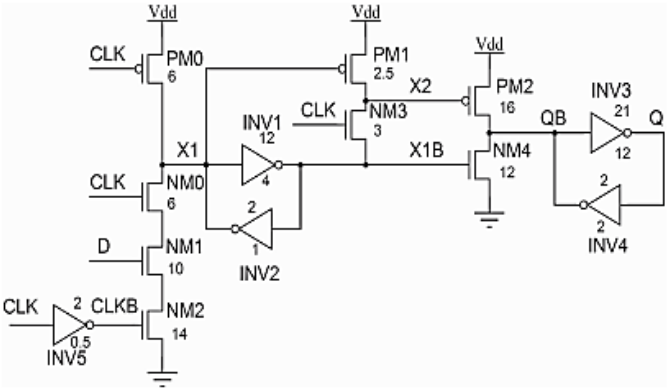


Fig.1. Circuit Diagram of DDFF

In Fig.1 shows the DDFF architecture. Here node $X_1$ is pseudo-dynamic, it is acting as a keeper with a weak inverter, and $X_2$ is purely dynamic in the new architecture. We can be divided into two phases of operations of the flip flops: 1) In the evaluation phase, the *CLK* is HIGH and 2) In the pre-charge phase, the *CLK* is LOW. If both are 1-1 then *CLK* and *CLKB* will overlap when actual latching occurs during the evaluation phase. Under this overlap period if *D* is high then through $NM_0$-$NM_2$ node $X_1$ is discharged. These all switches are state of cross-coupled inverter pair $INV_1$-$INV_2$ determining the node $X_{1B}$ raised and $Q_B$ is output, it discharged through $NM_4$. Here node $X_1$ is owned by inverter pair $INV_1$-$INV_2$ where no latching occurs at a low level for the rest of the evaluation phase. Accordingly, the node $X_2$ carried a high evaluation period by the PMOS transistor $PM_1$. When the circuit is coming in the pre-charge phase then our *CLK* is low, and node $X_1$ draws up high through $PM_0$, and there is a switching state of $INV_1$-$INV_2$. Till this period the node $X_2$ is not an active condition by any transistor and stored the charge. The voltage stages maintain through $INV_3$-$INV_4$ and outputs at node $Q_B$. In the

overlap period, *D* is high, then $X_1$ node will also be high and node $X_2$ pulled low via $NM_3$ as CLK goes high. Hereby $NM_4$ is off and node $Q_B$ is fully charged high via $PM_2$. At the last of the assessment phase, as the *CLK* falls, the node $X_1$ similarly high, and node $X_2$ stores the charge dynamically. This architecture shows negative setup time since short translucency period, it is defined by the 1-1 overlap period *CLK* and $CLK_B$ permits the data to be sampled after the rising edge of the *CLK* before $CLK_B$ falls down [10].

## 2.2 HYBRID LATCH FLIP-FLOP ARCHITECTURE

We can see architecture of hybrid latch flip flop in Fig.2 [11]. This is very easy to operate and it is very simple. If our clock is low, then node *X* is charged too high and $MN_2$, as well as $MN_1$, are in on condition. When the clock builds the transition from low to high then, $MN_5$ and $MN_6$ are turn on and remain also in on condition. These three inverters are used for equal periods of delay.

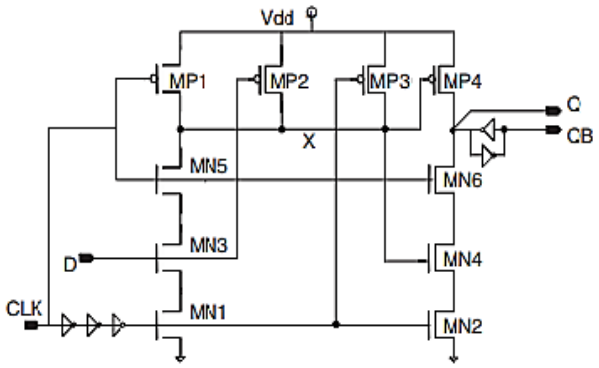


Fig.2. Circuit Diagram of HLFF

Here are all four transistors in one condition simultaneously, (MN1, MN2, MN5, and MN6) and a window of transparency will be formed. Under this window, where D is high (low), then the X node is discharged (remains charge), and pressuring the output should be high (low). If *D* is high for two back-to-back clock periods, node Q and node *X* both make an unessential high to low transition. It increases the total energy use of the flip flop and increases the dynamic [13]-[14]. Additionally, the excess of the transistors in the discharging output path ($MN_2$, $MN_4$, and $MN_4$) reduces the performance of the logic. Where we need low power and or high speed is required then HLFF is not a suitable application for that. [11].

## 2.3 MODIFIED TRANSMISSION GATE FLIP-FLOP

Here we are explaining TGFFv2 in Fig.3. Here TGFFv2 stands for modified transmission gate flip flop. This circuit is working on 32 nm and predictive technology used.

All size transistors are *L* equals 32nm for MNOS and PMOS [12]. In the topologies the transistor size has not been examined to reduce the spread of analysis, and because the primary objective of our analysis is the relation degradation through the circuits. Here in each aging mechanism, the maximum $V_{th}$ degradation is equal to 50 mV, and the lowest resistance carries values of tens of *kX*. These values speculate nearly five years of degradation at 100 ºC in nanometer technologies.

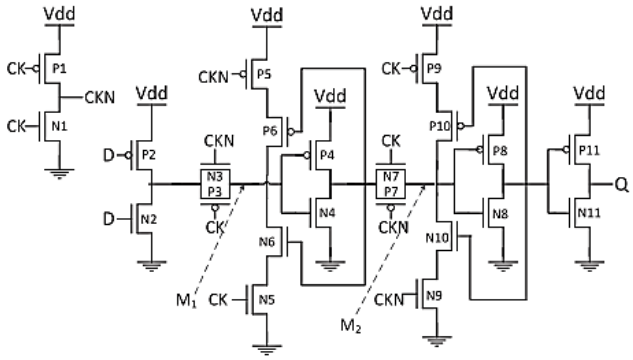


Fig.3. Circuit Diagram of TGFFv2

$$\Delta V_{th\_BTI} = a.(TSP.t)^n \quad (1)$$

where, *a* is the technology and temperature-dependent constant, BTI time exponential constant is *n*, time is *t*, and transistor stress probability is *TSP*. Generally, *TSP* is a procedure that identifies the conditions of transistor stress in any arrangement of the network, considering signal probability.

$$\Delta V_{th\_HCI} = b.(TSwP.t)^m \quad (1)$$

where, *b* is a technology and temperature-dependent constant, HCI time exponential constant is *m*, time is *t*, and the transistor switching stress probability is *TSwP*. For each conditions, we assume the values: *a*=3.9103 for NBTI, *a*= 1.3103 for PBTI, *n*=1/6, *b*=2.2105, *m*=0.5, *k*=51039, and *p*=5. We can assume the signal probability (TSP) equal to be 0.5 for all inputs and internal nodes of memory, and *TSwP* is the switching probability of all signals considered as the same [12].

## 2.4 MODIFIED HYBRID LATCH FLIP-FLOP ARCHITECTURE

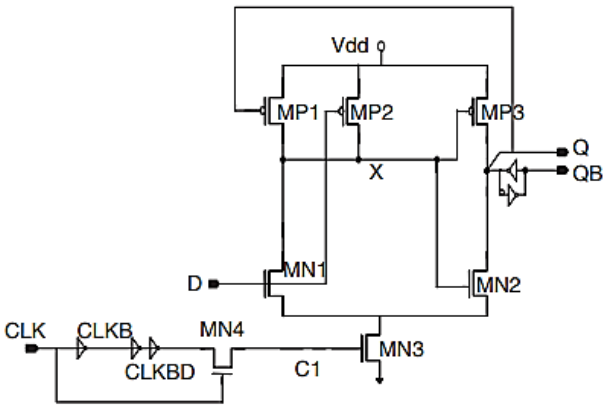


Fig.4. Circuit Diagram of MHLFF

For the avoidance of unnecessary in previous logic circuits, then we simulated an MHLFF, modified hybrid latch flip flop that is shown in Fig.3. Under this flip flop, when we have two different input logic values in successive clocks then the node transition will occur. Here we are explaining the operational principle of this work. If our clock –forms a transition from low to high and CLKB will be high for an equal period to the delay of three inverters making a transparency window. In this cycle, here $C_1$ is high turning ON $MN_3$. Under this window, if *Q* is high and *D* is low then *D* was high in the last clock, where $MP_2$ modifies on turning

on $MN_2$ and pressuring on the output to low. If $Q$ and $D$ both are low, then earlier than the starting of the transparency window $MP_1$ and $MN_2$ are on, and the delay would be zero, this is similar to the previous flip-flops. If $Q$ is low and $D$ is high, then the $X$ node gets low turning on $MP_3$ pressuring the output should be high. Here we noted that $MP_1$ is the weakest transistor, the working problem during the changed output is qualified. If $Q$ and $D$ both are high, then the $X$ node will not change, and here discussed adversary to the flip flops, and avoided the redundant transitions. We can compare another advantage of the logic with the other flip flops; there is no delay for high to high transition [11].

## 3. SIMULATION AND COMPARISON RESULT

Here we are comparing different flip flops architectures in this paper, we have used TSPICE simulation with 90 nm CMOS technology and $V_{dd}$ = 1V at 25ºC for all the flip flops.

### 3.1 DATA ACTIVITY VS. POWER

As the total average power in the flip-flops depends on data activity, an illustration of average power at data activities of 100%, 50%, 25%, and 0% as shown in Fig.5. Data activity of DDFF at 0%, 25%, 50%, and 100% correspond to 1111…., 00000011.., 0011…., and 1010…. data pattern. In all flip-flops the lowest power of MHLFF at 0% data activity. The result shows that the simulated design consumes the lowest total average power for 0% data activity. We can see the average power at different data activity as shown in Table.1.

Table.1. Comparison between Data Activity vs. Power (µw)

| FF | 0% | 25% | 50% | 100% |
|---|---|---|---|---|
| DDFF | 48.196 | 35.891 | 46.44 | 41.3627 |
| HLFF | 267.36 | 220.85 | 267.9 | 272.814 |
| MHLFF | 3.3931 | 4.6005 | 5.9289 | 5.3787 |
| TGFF | 9.0273 | 13.6892 | 16.03 | 20.1626 |

### 3.2 VOLTAGE VS. POWER

As shown in Table.2, we are calculating the average power at 0.7V, 0.9V, 1V, and 1.5V. In all flip-flops, if we are increasing the temperature as well as power will also increase. The TGFF consumes less power at 0.7V and MHLFF is also consumed less power at the same temperature and the highest average power in all flip flops at 1.5V. Here HLFF consumes maximum power at 0.7v as well as 1.5V. We also can see graphical representation in Fig.6.

Table.2. Comparison between Voltage (V) vs. Power (µw)

| FF | 0.7 V | 0.9 V | 1 V | 1.5 V |
|---|---|---|---|---|
| DDFF | 14.2922 | 31.8269 | 59.228 | 871.896 |
| HLFF | 55.5049 | 160.551 | 260.05 | 2116.8 |
| MHLFF | 5.2461 | 7.3517 | 10.595 | 127.526 |
| TGFF | 3.5828 | 8.2661 | 14.877 | 622.669 |

### 3.3 TEMPERATURE VS. POWER

Here we are calculating the average power at the different temperatures at 25-100℃. We are calculating the power of DDFF, HLFF, MHLFF, and TGFF. In DDFF architecture, we will increase the temperature as well as power also increased. HLFF and TGFF are also the same as DDFF in process of temperature. Now we are talking about MHLFF, In MHLFF we are increasing the temperature then the average power will decrease. We can see all the parameters in Table.3 and here graphical representation is also showing in Fig.7. Here all the power comes in µw.

Table.3. Comparison between Temperature (ºC) vs. Power (µw)

| FF | 25 ºC | 30 ºC | 35 ºC | 40 ºC | 45 ºC | 50 ºC | 55 ºC | 60 ºC | 75 ºC | 100 ºC |
|---|---|---|---|---|---|---|---|---|---|---|
| DDFF | 59.227 | 49.985 | 53.757 | 59.160 | 60.535 | 62.758 | 65.31 | 68.240 | 77.739 | 91.60 |
| HLFF | 260.05 | 263.66 | 265.90 | 269.60 | 272.33 | 276.16 | 280.5 | 285.60 | 297.39 | 325.0 |
| MHLFF | 10.595 | 10.167 | 10.156 | 10.110 | 10.068 | 10.023 | 9.980 | 9.9637 | 9.849 | 9.775 |
| TGFF | 14.876 | 15.309 | 15.220 | 15.901 | 16.556 | 17.204 | 17.89 | 18.941 | 21.131 | 25.26 |

In this paper, we are also calculating the average delay. The minimum delay comes in DDFF architecture that is 3.7396 and the maximum delay that comes in TGFF Architecture is 26.9904. In HLFF and MHLFF, the average delay is 18.7292 and 11.2407. We can see the delay in Table.4.

Table.4. Average Delay and No. of Transistors

| FF Designs | DDFF | HLFF | MHLFF | TGFF |
|---|---|---|---|---|
| No. of Transistors | 18 | 20 | 19 | 22 |
| Average Delay | 3.7396 | 18.7292 | 11.2407 | 26.9904 |

As shown in Fig.8, the output waveform of D Flip Flop. In this waveform, we are plotting the CLK, Data, Q and QB. The amplitude of all waveform is 1 volt. Here Data is the input and Q is the output. In this flip flop, if our CLK is HIGH then our output will come same as data. If our CLk is LOW then it will goes to previous state. This is working of D FF. Here the input we are using 11100110.

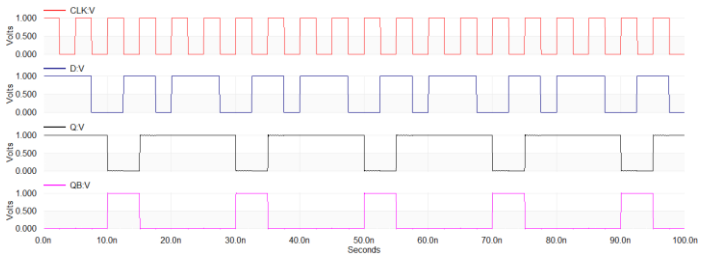


Fig.8. Output Waveform of D Flip Flop

## 4. CONCLUSION

In this paper, we have analyzed the average power of flip flops, here low power D flip flop (MHLFF) reduces the power consumption as compare to HLFF. We have simulated four

circuits in this paper. These circuits are DDFF, HLFF, MHLFF and the last one is TGFF. Overall circuits, if we will calculate the power then MHLFF is less consume power that is 5.2461µw and if we will talk about delay then delay comes very less in DDFF that is 3.7396. In this paper, we are calculating Average power at different voltages, temperatures, and average delay. We are also calculating power at data activity.

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