ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2021.0179

DESIGNING OF VARIATIONS TOLERANT SENSING AMPLIFIER CIRCUIT FOR DEEP SUB-MICRON MEMORIES

Vivek Harshey[1] and S.K. Bansal[2]

[1]*Department of Electronics and Communication Engineering, Sant Longowal Institute of Engineering and Technology, India*
[2]*Department of Electrical and Instrumentation Engineering, Sant Longowal Institute of Engineering and Technology, India*

Abstract

In deep sub-micron memories like DRAM and SRAM, faithful sensing of bit line voltages is becoming very challenging as transistor characteristics mismatch caused by intrinsic variations in manufacturing processes has posed a grave challenge leading to failures of circuits and reductions in yield. This paper addressed these issues and applied a compensation scheme to various schematics of sense amplifiers, which have resulted in a high tolerance to process-induced variations. The schematics, designed with DGFinFET, utilize an enhanced self-compensation technique to surmount disparities in physical transistor characteristics. The recreations of transistor mismatch (threshold voltage, V_t) using the Monte-Carlo technique show that the proposed CCLSA schematic performs correctly even for severe V_t mismatch of 40-50mV. These results are compared with corresponding circuits reported in the literature for the speed, area, and yield. This design also offers up to 20-30% higher yield compared to its uncompensated counterpart and has a reduced penalty for the complexity of circuit and performance. These circuits are easily implementable at 45nm and 32nm technology nodes.

Keywords:

Compensation, Process Variations, DRAM, FinFET Sense Amplifier, Robustness

1. INTRODUCTION

With the emergence of nanoscale devices, FinFET is identified as a potential candidate for replacing planar CMOS by academia and industry experts. For device dimensions below 90nm, a significant challenge arises from process variations due to statistical parameter variation in the manufacturing process. The variations of transistor characteristics cause mismatch and manifest itself in various circuits malfunctioning. Sense amplifier circuits are used to sense the voltage levels on the bitlines [1]. The reliable operation of the circuit requires perfectly matched transistors that are connected in a cross-coupled fashion. This cross-coupling essentially forms a regenerative feedback connection, which gets activated when there is a slight disparity in the voltages of the input signals and amplifies this to rail voltages, which are then latched [2].

Statistical fluctuations in dopant densities, intra-die variations attributable to variations in critical dimensions related to lithography, parametric variations of devices, and oxide thicknesses cause a mismatch in the threshold voltages between the regenerative feedback transistors. If the difference is significant, it may be sufficient to overcome differential bit voltage established on the sense amplifier's bit-lines. In this scenario, there is a very high possibility that the sense amplifier may latch to incorrect rail voltages, thereby critically affecting the functionality of the circuits. This malfunctioning of some sense amplifiers translates to the loss of yields as a typical chip contains thousands of sense amplifiers. Therefore, an attempt should be made to design a robust sense amplifier that compensates for transistor mismatch and has reduced failure probabilities against process variations [3].

Various works of literature have mentioned that the most promising alternatives to traditional bulk CMOS are FinFETs [4]. The larger gate area of FinFET helps improve drive-current, and the reduced channel doping of the FinFET reduces sub-threshold leakages. For circuit design below 45nm, the FinFET is a promising candidate owing to its vertical double gate structure [5]-[6]. Therefore, FinFET is a natural device of choice to mitigate the challenges posed by deep submicron bulk MOSFET and hence used in the design of a sense amplifier.

The scaling of V_t becomes very important at the reduced supply voltages in the deep sub-micron regime for the reliable operations of circuits. The scaling of V_t causes off-current problems, which are also faced in scaled logic devices. Such low-V_t devices are costly for industry-standard DRAM. Additionally, specific lower-voltage sensing circuits can be built [7]-[8]. Current-sensing techniques proved to be very efficient at very low supply voltages to obtain the full charge from the capacitor by holding the bit line voltage nearly constant during sensing [13]. Hence, a current-latch sense amplifier (CLSA) is designed using the compensation technique, which would be robust to process variations. In this study, Predictive Technology Models (PTM) for 45nm, 32nm FinFET devices are used to demonstrate the proposed approach's effectiveness [10]-[11].

2. FINFET BASED LATCH SENSE AMPLIFIER

The circuit diagram of a FinFET-based CLSA is shown in Fig.1. All transistors in this design refer to the nominal 45nm technology node devices [12]. Due to process variations like random dopant fluctuations, oxide thickness, channel length, threshold voltages of transistors have random variations that cause mismatch among transistors. This mismatch can induce the current mismatch in the evaluation branches of the sense amplifier circuit. It is also responsible for trip point mismatch among the cross-coupled inverters of sense amplifiers. The operation of the circuit gets affected, and it malfunctions. The trip point is the point on the inverter characteristic where the input voltage equals the output voltage, i.e., V_{out}=V_{in}. The circuit in Fig.1 is symmetrical in the absence of any parametric variations. The circuit operation can be described in two phases, i.e., precharge phase and sensing phase. During the precharge phase, output nodes are precharged to V_{DD} by the two pre-charging FinFETs X1 and X4; this results in activation of bitline voltages V_{bl} and V_{blbar} to the circuit (e.g., $b_l = V_{DD}/2$ and $b_{lbar} = V_{DD}/2 - \Delta V$, where ΔV is bitline differential voltage). To start the sensing operation sense, enable signal (SEN) is applied, and the circuit begins conducting. Application of SEN signal forces output nodes to discharge. Since

the current through the transistor is proportional to the applied gate voltages in the active region, therefore, current developed in X7 is higher than current developed in X8 (V_{bl}>V_{blbar}), thus forces OUT1 to discharge faster than OUT2. This disparity in the discharging rate of the output node triggers the strong positive feedback of the cross-coupled inverters and turns on the FinFET X3 of OUT2, thus pushes OUT2 back to V_{DD}. Now the output nodes move in the opposite directions, and rail to rail signal voltages are obtained, which corresponds to correct sensing operation.

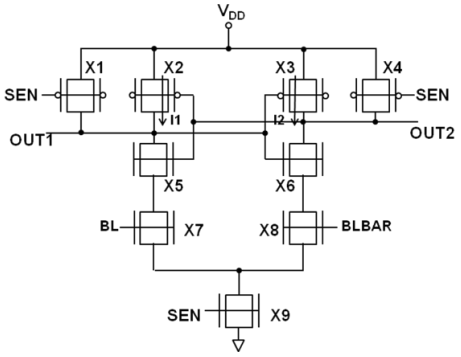


Fig.1. FinFET based Latch Sense Amplifier circuit

2.1 FAILURE IN SENSING OPERATION IN SENSE AMPLIFIER

Due to local variations during manufacturing, a mismatch might occur, causing the sense amplifier structure to become asymmetrical. These imbalances can be modeled by an offset voltage V_{os}. A systematic offset may also arise since matched devices can never be utterly symmetrical in layout. Due to random threshold variations, transistor X7 shown in Fig.1 might develop a higher threshold voltage V_t than the threshold voltage of X8. This increased threshold voltage could negate the current differential developed in X7 and X8 due to differential bitline voltages. It may even cause the current induced in X8 to be more significant than that in X7. In this case, OUT2 has a fast rate of discharging than OUT1, and the circuit flips in the wrong direction, resulting in the incorrect sensing operation.

The input offset voltage (V_{os}) of a sense amplifier is defined as the minimum bit-differential $\Delta V_{IN}^{\min}$ required by a sense amplifier for correct sensing [17]. The sense amplifier circuit of CLSA is considered symmetric if devices are perfectly matched on either side of the centerline. Hence $\Delta V_{IN}^{\min} = V_{os}$ where $\Delta V_{IN} = V_{BL} - V_{BLB}$ and $V_{os} = V_{t_{X7}} - V_{t_{X8}}$, for V_{os}=0, the circuit works perfectly and senses any bit-differential correctly. For illustration, pretend that the threshold voltage of transistor X8 is decreased due to process variations, and the threshold voltage of X7 is increased $V_{t_{X7}} > V_{t_{X8}}$. Under this condition, although (V_{BL}>V_{BLB}), the current I_1 can be lower than I_2 because $I_1 \propto (V_{BL} - V_{t_{X7}})$ and $I_2 \propto (V_{BLB} - V_{t_{X8}})$.

For this situation where I_1<I_2, incorrect sensing operation results due to a faster discharging rate of the output node OUT2. It may also be caused by a mismatch in channel width and channel length in X7 and X8. To ensure reliable operation, we need to provide $\Delta V_{IN} = (V_{BL} - V_{BLB}) > V_{os} (= V_{t_{X7}} - V_{t_{X8}})$, and therefore, the failure probability of this circuit is expressed as $P_F = P(V_{os} > \Delta V_{IN})$ [13].

2.2 EFFECT OF V_T MISMATCH ON SENSING OF CLSA

The threshold voltage V_t variations of circuit transistors result in a normal probability distribution with zero mean for the offset voltage V_{os}[7]. In Monte-Carlo simulations, the threshold voltage V_t mismatch of every transistor in Fig.1 is modeled as a Gaussian random variable. Therefore, it helps us to generate random V_t variations in Monte-Carlo simulations for each transistor independently in each simulation. The yield of the sense amplifier is defined as:

$$\text{Yield} = (\text{Number of Correct Decisions/Total number of simulations}) \times 100\% \quad (1)$$

For proper operation, $\Delta V_{IN} > V_{os}$, where ΔV_{IN} is the minimum bit-differential voltage required for satisfactory operation. Owing to fluctuations in doping densities, oxide thickness variations, offset voltage varies. To lower the failure probability ΔV_{IN} should be increased, or V_{os} be decreased. However, there is a limit to increase the input bit differential voltage ΔV_{IN} beyond which it cannot be increased. So, V_{os} variation must be reduced to reduce failure probability or equivalently to increase yield. The variation in V_{os} of this circuit impacts circuit performance considerably than any other parameter and therefore increases access failure significantly [11]. Hence, the prototype of a robust circuit is necessitated to reduce failures of sensing in memory and can be obtained by modifying the schematic to make it tolerant against V_t variations.

3. COMPENSATED CURRENT LATCH SENSE AMPLIFIER (CCLSA)

The proposed schematic biases transistors X7 and X8 independently and has compensation circuitry, as shown in Fig.2. The front gates of the X7 and X8 transistors still act as inputs to bitline voltages while the remaining transistors have gates that are tied together. The back gates of critical transistors X7 and X8 have the compensation circuitry, which includes capacitance C1 and C2 for storing the reference voltages for compensation. The 'TRAIN' control signal charges C1 and C2. This schematic is a modified version of the IGSSA circuit [14].

There are two N-FinFETs X16 and X17 added to the new circuit to speed-up the charging of the capacitors C1 and C2. They provide a high impedance path for the current flowing through the transistors X7 and X8 when the 'TRAIN' signal is raised high. Hence the current is not divided into the branch consisting of X16 or X17, and full current is available for charging the capacitors. So, for a fixed duration of the TRAIN signal, the voltages developed across capacitors C1, and C2 will be more than the voltages generated in the IGSSA circuit of [14] for the same values of capacitances used. Hence it can withstand a more substantial mismatch in threshold voltage V_t and, therefore, are more robust than the latter. All devices used in the circuit are nominal devices with W=90nm and L= 45nm.

3.1 OPERATION OF CCLSA

The operation of CCLSA can be divided into four stages, (i) precharge, (ii) discharging of capacitance, (iii) training, and (iv) evaluation. The capacitance discharge phase is for fully discharging the capacitors by raising the DISCHARGE signal. When the SEN signal is low, the CCLSA enters the precharge phase, while in the evaluation phase, SEN is turned ON. TRAIN and DISCHARGE signals are generated directly from the sensor signal by using the self-timing circuits [15].

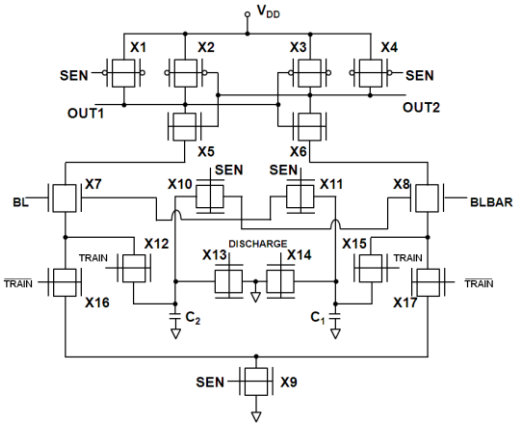


Fig.2. Schematic for compensation technique

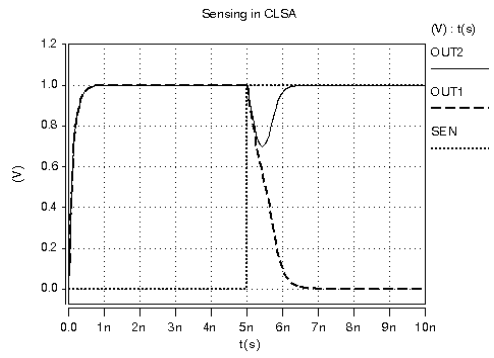


Fig.3. Correct sensing in the CCLSA circuit

The waveform for the CCLSA circuit under threshold voltage V_t variations is depicted in Fig.3. Once the TRAIN phase is turned on, capacitors C_2 and C_1 enable compensation due to mismatch through back gate biasing of the FinFET. This circuit works faithfully even for a threshold voltage variation of 40mV in X7 and X8 as the sense amplifier performs correct sensing, shown in Fig.3.

4. INDEPENDENT GATE SENSE AMPLIFIER

The proposed IGSA circuit using FinFET at 45nm technology node is shown in Fig.4. This schematic has been derived from the circuit schematic reported in [11]. Here the bit-line differential voltages are applied to one gate of the pFinFETs X2 and X3, while the other gate is used to form the cross-coupled inverters' connections.

Using the independent gate operation of FinFET, the current difference in the two pull-down paths is achieved by using a single FinFET in each path. The front gates of X2 and X3 are connected in the cross-coupled inverter configuration, whereas BL and BLBAR are connected to the back gates.

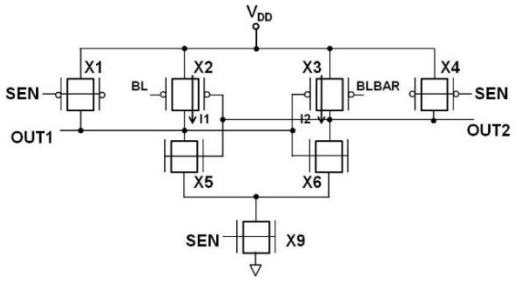


Fig.4. Schematic for independent gate sense amplifier (IGSA)

4.1 IMPROVEMENTS OF IGSA CIRCUIT OVER CLSA CIRCUIT

In the IGSA circuit of Fig.4, the output nodes are discharging through the stack of two transistors compared to the three transistors stack of CLSA. This reduction in the number of stack transistors has a positive effect on reducing sensing delay. In the IGSA circuit, output nodes drive only the front gates of FinFETs X2 and X3 instead of both the front and back gates of FinFET X2 and X3, as in Fig.1. The reduction in the capacitive loads on output nodes results in increased speed and reduced switching power [11]. Also, elimination of X7 and X8 reduces complexity; hence saving of chip area is achieved.

The robustness of the IGSA circuit is better than the directly translated CLSA circuit, and this improvement happens because of the removal of X7 and X8, which eliminates the input offset due to mismatch in transistors, hence reduces the input offset voltage.

4.2 COMPENSATED CIRCUIT FOR IGSA (CIGSA)

The compensation circuitry has been incorporated in the recommended schematic, as Fig.5 depicts.

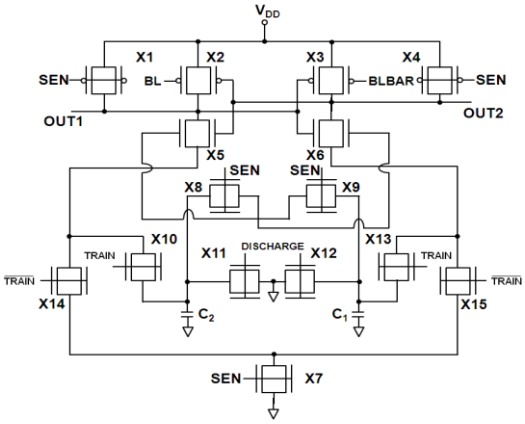


Fig.5. Schematic for compensation technique for IGSA

In the modified circuit, the reference voltages developed across two capacitors C_1 and C_2, are applied to one gate of transistors X5 and X6, which form the cross-coupled inverters. While the bit line voltages are applied to transistors X2 and X3, in this way, the compensation scheme is employed using the back gate of FinFET. The inputs are fed to the X2 and X3 transistors' front gates. The compensation circuitry is provided to the back

gates of the transistors X5 and X6, which consists of C_1 and C_2 capacitances to support the building of voltages for compensation. The 'TRAIN' control signal charges C_1 and C_2.

5. LATCH-BASED SENSE AMPLIFIER

Another sense amplifier circuit called Latch Based Sense Amplifier (LBSA) is shown in Fig.6, which is derived from the circuit reported in [16]. This circuit consists of the cross-coupled inverter latch formed by X2, X4 and X3, X5, and hence the name of the circuit. Before sensing operation, OUT1 and OUT2 are tied to ground (zero volts). The operation of the circuit commences as outputs start charging up to supply voltage V_{DD} via the X2 and X3 transistors. However, the differential voltage on FinFETs X2 and X3 front-gates causes an imbalance in the current flow, which results in slowing down of charging of OUT1 and OUT2.

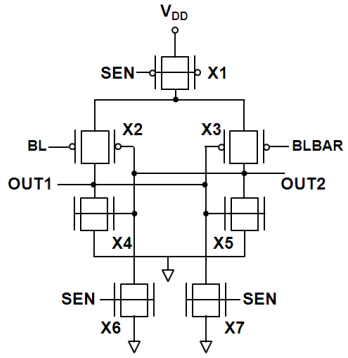


Fig.6. Schematic of Latch Based Sense Amplifier (LBSA)

Owing to positive feedback in the schematic of Fig.6, the growing voltage of one of the output nodes causes cutting-off of the opposite pFinFET, hence reduces the pull-up current of the corresponding transistor.

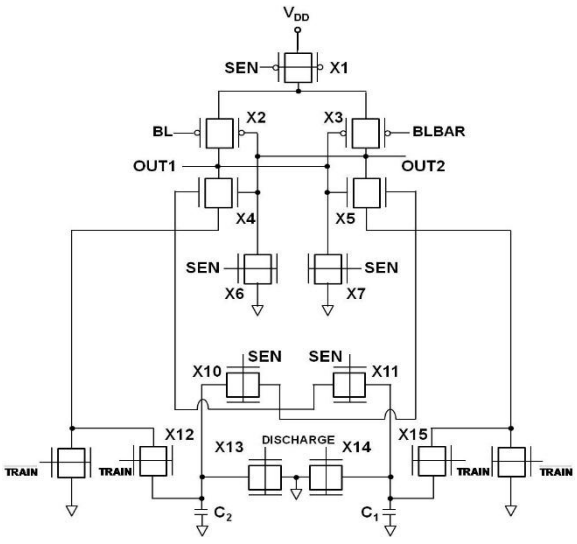


Fig.7. Schematic for compensation technique for LBSA

This cross-coupled connection also causes an increase in conductivity and a better pull-down of the relevant output voltage at the back-gate of nFinFET [16]. This schematic suffers from a disadvantage in that during sensing, an open path from ground to V_{DD} exists since X4, and X5 front-gates are always connected to the bit lines, which are precharged to V_{DD}. The compensation scheme applied to the IGSA circuit has also been used to LBSA (Fig.7) to make it process variation tolerant. The compensation scheme works similarly for LBSA, as explained for IGSA and CLSA.

6. RESULTS AND DISCUSSION

6.1 YIELD vs. V_T MISMATCH

The yield is a crucial characteristic of a sense amplifier, which depends upon several parameters, especially on ΔV_{in}, [17]. For this discussion, it is assumed that the simple layout is fully matched so that no systematic mismatch occurs. The analysis presented here has been adapted from [17] and done for random mismatch but also valid for systematic offset.

From the theoretical point of view, the yield $Y(\Delta V_{in})$ is identical to the probability P for the actual offset voltage V_{os} to lie below ΔV_{in}, where V_{os} follows a Gaussian probability distribution. Yield expression is given as:

$$Y(\Delta V_{IN}) = P(V_{os} \le \Delta V_{IN}),$$

$$Y(\Delta V_{IN}) = \frac{1}{2}\left(1 + erf\left(\frac{\Delta V_{IN}}{\sigma_{os}\sqrt{2}}\right)\right)$$

$$\sigma_{os} = \frac{\Delta V_{IN}}{\sqrt{2}erf^{-1}(2Y-1)}$$

Where σ_{os} is the standard deviation of the input offset voltage, and *erf*() is the error function. So, yield increases if σ_{os} decreases. The compensated circuits are insensitive to the threshold voltage variation or equivalently input offset voltage variation. So, for them, σ_{os} has effectively decreased, and hence they exhibit more yield than their uncompensated counterparts. Moreover, if σ_{os} increase, so from the above expression yield goes down as the erf function decreases with an increase in σ_{os}. The yield can be improved by making the circuit less susceptible to σ_{os} variation hence adopting the compensation scheme.

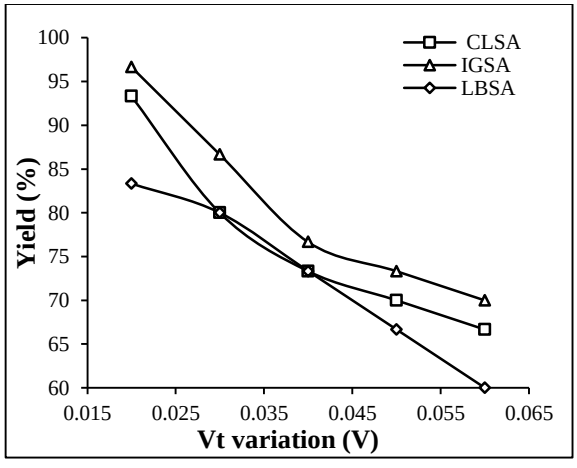


Fig.8. Yield comparisons for different sense amplifiers

The yield comparison of the CLSA, IGSA, and LBSA circuits is shown in Fig.8. As can be seen, IGSA has the highest yield. This improvement in yield happens because the removal of X7 and X8 from the CLSA circuit eliminates the input offset due to a mismatch in these transistors, thereby reducing the input offset

voltage. We see from Fig.8 that IGSA maintains almost 5-7% more yield than the conventional CLSA circuit over the total threshold voltage V_t variation range. Though IGSA has a slightly better yield (nearly 5%) than CLSA, this is still not sufficient yield improvement. To further improve the yield, the compensation scheme has been applied to all the sense amplifier circuits, i.e. CLSA, IGSA, and LBSA.

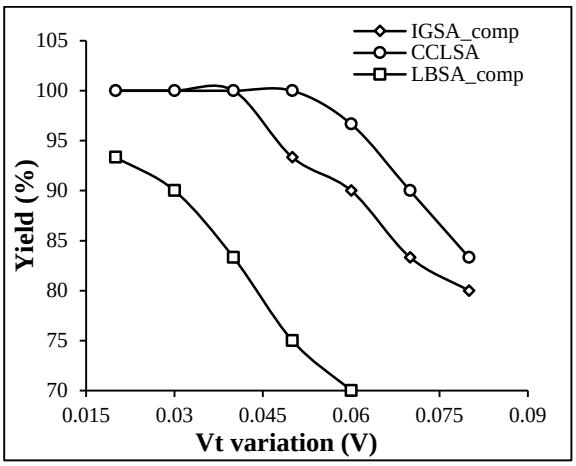


Fig.9. Yield graphs for compensated and uncompensated designs

The yield comparisons of the CCLSA, CIGSA, and CLBSA circuits are shown in Fig.9. As can be seen, CCLSA has the highest yield, as is seen from Fig.9 that for a V_t mismatch of 40mV, which is typically the worst case in manufactured devices, CCLSA maintains its yield close to 100% as compared to the 95% yield of CIGSA. CLBSA yield has dropped considerably to almost 75%. However, still, this is higher than its uncompensated counterpart LBSA. Hence, the yield gain of CIGSA over CLSA and IGSA is almost 25-30% for the same V_t mismatch, which is a significant improvement. Though CCLSA has a higher yield than CIGSA, complexity is sophisticated.

6.2 SENSE DELAY vs. BIT-LINE DIFFERENTIAL VOLTAGE

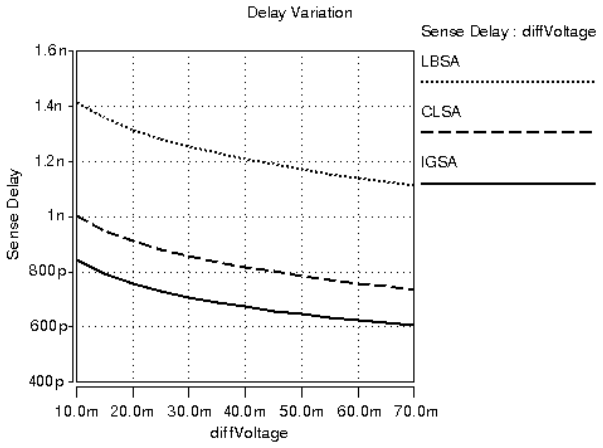
The total sense delay t_{SA} can be expressed as $t_{SA} = t_0 + t_{latch}$, where t_{SA} is the sum of delay t_0 and t_{latch}. The delay t_0 represents the capacitive discharge of a load capacitance C_L at both outputs until the first p-channel transistor turns on. The second term t_{latch} is the latching delay of two cross-coupled inverters. The t_{SA} can be expressed as:

$$t_{SA} = \underbrace{\frac{2C_L V_{th}}{I_0}}_{t_0} + \underbrace{\frac{C_L}{g_{m,eff}} \ln\left\{\frac{1}{V_{th}}\sqrt{\frac{I_0}{2\beta}}\frac{\Delta V_{out}}{\Delta V_{IN}}\right\}}_{t_{latch}}$$

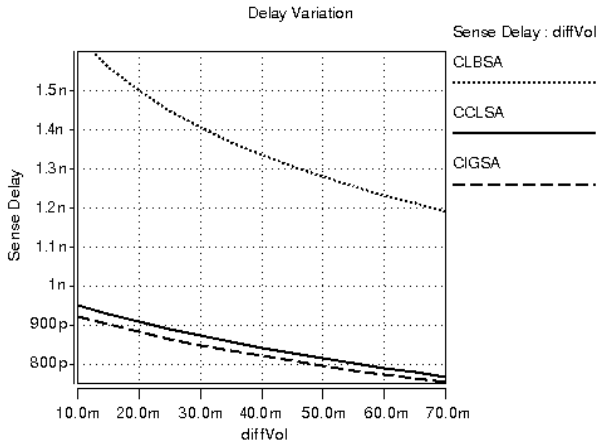
where V_{th} is the threshold voltage of X7 or X8, and I_0 is the total current $I_1 + I_2$. In the second term, ΔV_{in} is the input differential voltage. From the above expression, as ΔV_{in} increases t_{latch} decreases. So, for the CCLSA and other compensated circuit, since the compensation mechanism has the effect of increasing ΔV_{in}, hence t_{latch} goes down. Nevertheless, since its dependence on the ΔV_{in} is logarithmic, so this decrease is small.

On the other hand, for complex topology like CCLSA, overall load capacitance C_L increase, and so the t_0 increases. Also, t_0 has a direct dependence on C_L; therefore, an increase in t_0 is more compared to a decrease in the t_{latch}. The overall effect is that the t_{SA} of CCLSA is more than CLSA, though its value decreases as ΔV_{in} increases. The same reasoning applies to CIGSA and CLBSA circuits.

The sense delay versus bit-line differential voltage for IGSA and CIGSA is shown in Fig.10. Sense delay is measured as the time duration when the sensing starts, up to the time when the output reaches 90% of its final value [11]. As the applied differential voltage increases gradually, the sensing delay decreases since a stronger current is developed in the circuit, which speeds up sensing.



(a)



(b)

Fig.10. Sense delay variations for compensated and uncompensated designs

As is observed in Fig.10 that compensated IGSA (CIGSA) has 15-20% more sense delay than IGSA. This increased delay is attributed to the increased complexity of the CIGSA circuit, i.e., more devices. This delayed penalty is a trade-off between the choice of two designs, which calls for selecting a design style depending on robustness and circuit complexity

Further, the sense delays for CIGSA and CCLSA circuits have been compared in Fig.11 against the varying differential voltages. The CCLSA circuit has a marginally higher delay (3%) than CIGSA because of eliminating two transistors in the CIGSA circuit.

6.3 POWER DISSIPATION vs. BIT-LINE DIFFERENTIAL VOLTAGE

The Fig.11 shows that the average power dissipations of uncompensated and compensated circuits are given for one full sense cycle and plotted for various bit-differential voltages.

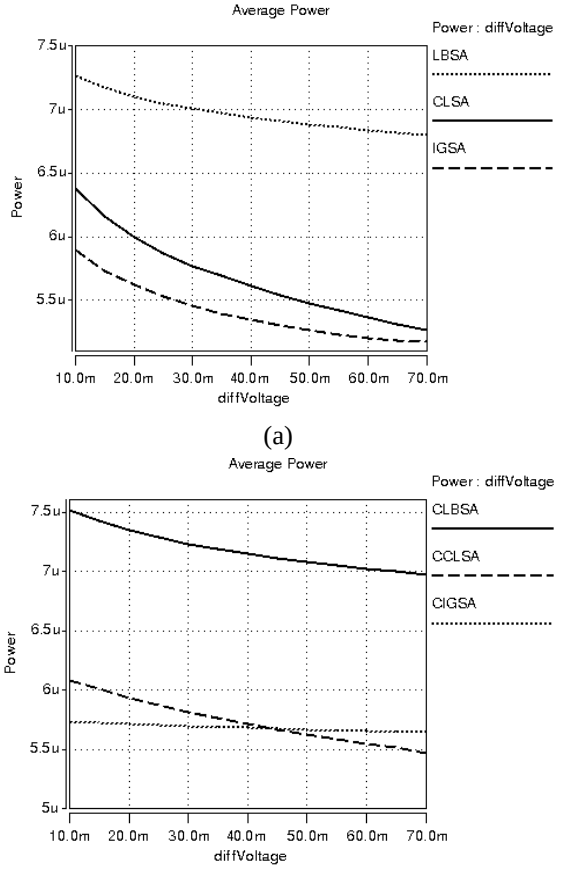


Fig.11. Average power dissipations for compensated and uncompensated designs

It is seen in Fig.11 that CLBSA shows 5-6% more power dissipation than LBSA. This is due to the added complexity introduced by the compensation scheme, hence increasing the number of devices. Power reduces as differential voltage increases since stronger current forces output nodes to reach their final values quickly. Elimination of transistor X7 and X8 from CLSA results in a 7% reduction in power for IGSA.

Also, in the case of compensated circuits, the power dissipations for CCLSA and CIBSA are comparable.

A summary of these circuit results is given in Table.1 and Table.2, and conclusions are drawn. The charts show meaningful comparisons between compensated and uncompensated circuits along with the design metrics. The chip area occupied by the circuit depends upon the width and length of the transistors. It can be approximately calculated by using the layout of the FinFET inverter [18]-[19]. The cell layout area has been expressed in terms of λ, the minimum spacing requirements for the particular technology. The area is found to be $120\lambda^2$.

Table.1. Comparisons for uncompensated sense amplifiers

Metrics	CLSA	IGSA	LBSA
Yield at mismatch of 40mV	72%	77%	70%
Delay at 40mV bitline diff. voltage	0.830ns	0.675ns	1200ps
Power dissipation at 40mV diff. voltage	5.6 µW	5.35 µW	6.95 µW
Area factor	$4.5\times120\lambda^2$	$3.5\times120\lambda^2$	$3.5\times120\lambda^2$

Table.2. Comparisons for compensated sense amplifiers

Metrics	CLSA	IGSA	LBSA
Yield at mismatch of 40mV	100%	95%	85%
Delay at 40mV bitline diff. voltage	0.840 ns	0.825 ns	1.350 ns
Power dissipation at 40mV diff. voltage	5.7 µW	5.67 µW	7.15 µW
Area factor	$9\times120\lambda^2$	$8\times120\lambda^2$	$8\times120\lambda^2$

From the above discussion, it is clear that choosing a particular design style strongly depends upon the requirements. If the circuit has to operate under severe process variation conditions, then CCLSA is the best choice. It has the highest yield among all the circuits giving less delay penalty. The yield gain of CCLSA over the CLSA circuit is almost 30% for a V_t mismatch as high as 40mV. This high yield is due to the introduction of compensation circuitry. Nevertheless, the chip area occupied by CCLSA is almost double that of CLSA.

If at the same time we also want less delay penalization, then the CIGSA circuit schematic can opt. This design maintains the yield close to CCLSA, and delay does not suffer much. The CIGSA circuit has merely 5% less yield than CCLSA, while the elimination of two transistors results in less chip area for CIGSA than in CCLSA. Sensing delays of CCLSA and CIGSA are comparable. CCLSA has just a 3% excess delay as compared to CIGSA.

On the other hand, if reduced circuit complexity is desired and less chip area is a prime requirement, then the IGSA circuit can be picked out. It offers an optimum design for yield, speed, and area. It has the least area among all the circuits. Also, the speed and yield of the circuit are optimum.

As seen in the above table, the speed of IGSA is higher than the other two uncompensated circuits. Moreover, it offers less area along with reduced power dissipation. So among the uncompensated circuits, IGSA is a natural choice for sensing operation for high V_t variation.

Hence even if the area is slightly higher for compensated circuits, they show substantial yield gain for worst-case V_t variations over the uncompensated designs. However, CCLSA has more area than other schemes among compensated circuits and offers the highest yield. Hence this increased area can be traded-off with the yield gain. The LBSA has the smallest area, but its yield deteriorates as variation increases. However, CLBSA improves the yield, but its delay and power dissipation are higher than the other circuits.

7. FUTURE SCOPE FOR WORK

This work concludes with the designs of these robust sense amplifier circuits. In this work, the ptm model is used to simulate FinFET based circuit schematics. These models give reasonably accurate results in less simulation time while avoiding going into the rigor of the device simulation. The possible future path consists of implementing these circuits in a device simulator where fine-tuning of individual transistor parameters, i.e. (oxide thickness t_{ox}, channel doping N_{ch}, etc.), can be done. At the same time, the accurate area can be calculated by drawing layouts of these circuits. Multi-fin structures which are not utilized in this work can be a possible option for reducing the delay.

8. CONCLUSION

In this work, different types of robust sense amplifier circuits are designed. Various process variations tolerant self-compensating FinFET based compensated current latch sense amplifier (CCLSA), CIGSA, CLBSA are presented in this paper. Their yield, sense delay, and power dissipations are measured and compared. The compensation scheme introduced is effective in restoring yield at worst-case process variation conditions. Moreover, the designed circuits do not suffer from any significant delay penalty. The proposed designs are easily implementable at FinFET 45nm and 32nm technology.

These designs can withstand significant mismatches (up to 40mV) in the primary sense transistors and reduce the failure probability to near zero compared to other uncompensated designs. The reduction in failure probability ensures reliable circuit performance for a broad range of V_t mismatch. Further, the robustness of the design is established by the simulations. The marginally higher delay penalty and area introduced by compensated designs can be traded-off with yield gain.

REFERENCES

[1] S.S. Rathod, A.K. Saxena and S. Dasgupta, "A Low-Noise, Process-Variation-Tolerant Double-Gate FinFET based Sense Amplifier", *Microelectronics Reliability*, Vol. 51, No. 4, pp. 773-780, 2011.

[2] B.S. Reniwal, P. Bhatia and S.K. Vishvakarma, "Design and Investigation of Variability Aware Sense Amplifier for Low Power, High Speed SRAM", *Microelectronics*, Vol. 59, pp. 22-32, 2017.

[3] R. Sharma, A. Mowar and A. Johari, "Comparison of Transients and FFT Memory Sense Amplifiers for Semiconductor Memories using 0.3µm CMOS Technology", *Proceedings of International Conference on Advanced Computation and Telecommunication*, pp. 1-7, 2018.

[4] E. Oriero and S.R. Hasan, "Survey on Recent Counterfeit IC Detection Techniques and Future Research Directions", *Integration*, Vol. 66, pp. 135-152, 2019.

[5] Bin Yu, "FinFET Scaling to 10nm Gate Length", *Proceedings of International Meeting on Electron Devices*, pp. 251-252, 2002.

[6] E. J. Nowak, "Scaling Beyond the 65 nm Node with FinFET-DGCMOS", *Proceedings of International Conference on Custom Integrated Circuits*, pp. 339-342, 2003.

[7] K. Itoh, Y. Nakagome, S. Kimura and T. Watanabe, "Limitations and Challenges of Multigigabit DRAM Chip Design", *IEEE Journal on Solid-State Circuits*, Vol. 32, pp. 624-634, 1997.

[8] T. Yamagata, S. Tomishima, M. Tsukude, Y. Hashizume, and K. Arimoto, "Circuit Design Techniques for Low-Voltage Operating and/or Giga-Scale DRAMs", *Proceedings of International Conference on Solid-State Circuits*, pp. 248-254, 1995.

[9] J.A. Mandelman, "Challenges and Future Directions for the Scaling of Dynamic Random-Access Memory (DRAM)", *IBM Journal of Research and Development*, Vol. 46, No. 2-3, pp. 2-6, 2002.

[10] PTM, "Latest Model", Available at http://www.eas.asu.edu/~ptm/, Accessed at 2012.

[11] S. Mukhopadhyay, H. Mahmoodi and K. Roy, "A Novel High-Performance and Robust Sense Amplifier using Independent Gate Control in Sub-50-nm Double-Gate MOSFET", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 14, No. 2, pp. 183-192, 2006.

[12] J. Yeung and Hamid Mahmoodi, "Robust Sense Amplifier Design under Random Dopant Fluctuations in Nanoscale CMOS Technologies", *Proceedings of IEEE International Conference on System on Chip*, pp. 261-264, 2006.

[13] S. Mukhopadhyay, A. Raychowdhury, H. Mahmoodi and K. Roy, "Leakage Current Based Stabilization Scheme for Robust Sense-Amplifier Design for Yield Enhancement in Nano-scale SRAM", *Proceedings of 14th Asian Test Symposium*, pp. 176-181, 2005.

[14] Aarti Choudhary and Sandip Kundu, "A Process Variation Tolerant Self-Compensating FinFET based Sense Amplifier Design", *Proceedings of the 19th ACM Great Lakes symposium on VLSI*, pp. 161-164, 2009.

[15] Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits-A Design Perspective*", 2nd Edition, Prentice Hall, 2006.

[16] P. Pranav, B. Giraud and A. Amara, "An Innovative Ultra Low Voltage Sub-32nm SRAM Voltage Sense Amplifier in DG-SOI Technology", *Proceedings of International Conference on Circuits and Systems*, pp. 205-208, 2008.

[17] B. Wicht, T. Nirschl and D. Schmitt-Landsiedel, "Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier", *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 7, pp. 1148-1158, 2004.

[18] A. Datta, A. Goel, R.T. Cakici, H. Mahmoodi, D. Lekshmanan and K. Roy, "Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 11, pp. 1957-1966, 2007.

[19] D. Nagamani, B.K.V Prasad, K.J.S. Lorraine and B.V.V.S. Kumar, "Fault Diagnosis of a Sense Amplifier Circuit", *Procedia Engineering*, Vol. 30, pp. 937-944, 2012.