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# AN IMPROVED NANOSCALE QUASI-BALLISTIC DOUBLE GATE (DG) MOSFET MODEL WITH DRAIN BIAS DEPENDENCY ON CRITICAL CHANNEL LENGTH NEAR THE LOW FIELD SOURCE REGION BY SEMI-EMPIRICAL APPROACH

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***Abstract***

***This work presents a physically accurate drain current model valid for Double Gate MOSFETs in the nanoscale regime. The model incorporates both diffusive and ballistic carrier transport on the basis of scattering theory. The significance of carrier scattering at the critical channel length near the low field source region is illustrated. The proposed model presents a semi-empirical approach to determine the critical channel length as a function of drain bias applicable for symmetric Double Gate MOSFETs. Fermi-Dirac statistics and Carrier degeneracy are considered in this work for optimal physical accuracy. The proposed quasi-ballistic model captures the signature effect of short channel devices and also exhibits good continuity in terms of drain current, terminal charges and capacitances. A relative analysis of the proposed quasi-ballistic model is done with other recent works.***

***Keywords:***

***Diffusion, Quasi-Ballistic Transport, Scattering, Critical Channel Length, DG MOSFETs.***

## 1. INTRODUCTION

In the recent past Multigate MOSFETs have successfully replaced bulk transistors in digital circuits due to their better performance and scaling abilities. A Double Gate (DG) MOSFET, which is a variant of multiple gate transistors, is considered to be an ideal nanoscale device that scales beyond the bulk CMOS limit [1]. A well designed symmetric Double Gate (SDG) structure offers identical gate work function that enables simultaneous switching of both gates leading to the formation of two inversion channels. The gate function completely determines the threshold voltage. More importantly, the device exhibits a near-ideal sub-threshold swing and also provides a higher transconductance [2].The top and bottom gates provide excellent electrostatic control of the channel resulting in the reduction of drain induced barrier lowering (DIBL) and threshold voltage variation with the channel length.

Several compact models have been proposed in the recent past for both long and short channel devices. When traditional compact models [3]-[5] are compared with the recently proposed models [6]-[11], it is found that although the Poisson's Eq.is still valid, the carrier transport is significantly different in nanoscale. Drift–diffusion transport models fail to capture the velocity overshoot, while the energy transport models omit certain details in the ballistic limit [12]. In a long channel device, the maximum drain current is limited by pinch-off, while in a short channel device it is first the velocity saturation and later the source injection velocity that limits the drain current. The Fig.1 represents different carrier transport phenomena that arise when the proposed device undergoes channel length scaling. Recently developed short channel compact models based on energy band diagrams, virtual source concept [13], Landauer –Boltzmann approach [14] have added new physical insights to the carrier transport in the nanoscale regime. In nanoscale devices, the transport in the channel is limited by diffusion near the virtual source [15]. The dependence of carrier scattering near the virtual source matters the most in defining the charge transport in a nanoscale MOSFET when the channel lengths are below 20nm range. The physics as per the scattering theory [16] clearly demonstrates that the maximum drain current is determined by the velocity saturation at the source and certainly not at the drain.

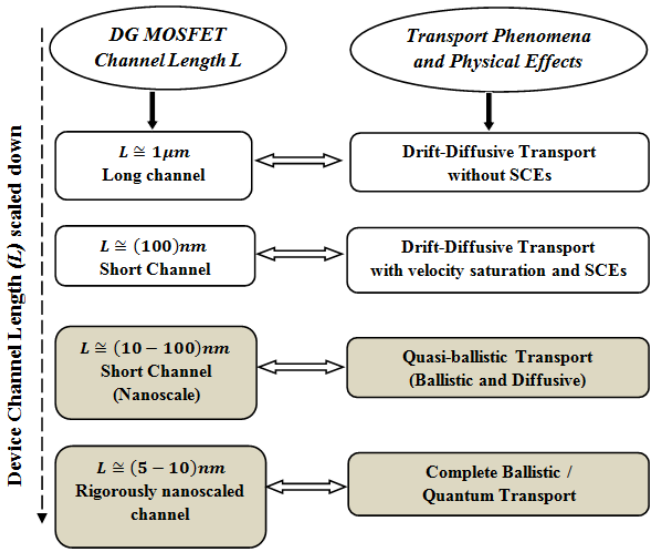


Fig.1. Different carrier transport phenomena arising when device channel length ($L$) is scaled down from micron to nanoscale. The proposed work focuses on the nanoscale regime (grey shaded region)

Contemporary state of art nanoscale devices exhibit quasi-ballistic phenomena, because the maximum drain current is restricted by the rate at which carriers are injected from the source. This bottleneck condition [17] suggests the need to include both diffusive and the ballistic transports aptly with the inclusion of scattering physics during MOSFET modeling in the nanoscale regime. The recent work presented in [18] demonstrates carrier scattering dependency at the critical layer near the low field source region on the drain current characteristics. This dependency is derived from the scattering theory in terms of transmission and reflection coefficients. For simplicity, in [18] arbitrary but meaningful critical lengths were taken near the source end that were comparable with the carrier mean free path, just to demonstrate the quasi-ballistic nature of the drain current in a DG MOSFET. However, the critical scattering length is a function of drain voltage. At very low drain bias, the entire

channel length $L$ acts as critical scattering length, but for moderate to high drain bias the carrier scattering rate depends on the critical length near the source and the velocity with which the carriers are injected from the source into the channel [19]. Hence, a careful analysis suggests the significance of critical channel length determination in the quasi-ballistic transport. The proposed model is an extended, more physically accurate and improvised version of the model presented in [18]. The model partly evolves from Natori's ballistic bulk MOSFET model, which is modified appropriately to be applicable for a Symmetric Double Gate MOSFET in the nanoscale regime. It assumes that gradual channel approximation (GCA) applies only at the beginning of the channel/ virtual source. The critical carrier scattering channel length $\delta$ at the low field source region is determined using a semi-empirical approach [19]. The proposed model is found to be valid in the ballistic, quasi-ballistic and the diffusive limits. The improvised model is shown to be continuous in terms of current, terminal charges and capacitances in all regions of device operation.

Section 2 describes the physical analysis approach and mathematical background of the proposed work. Section 3 illustrates the results obtained for the proposed model. Conclusion is done in section 4.

## 2. MODEL DESCRIPTION

In the first half of this section, a hypothetical fully ballistic drain current model for a DG MOSFET based on Natori's approach [20] is discussed. While in the second half, the model is transformed by including the quasi-ballistic physics. The proposed model further incorporates the impact of scattering at critical channel length semi-empirically near the virtual source on the device current characteristics at nanoscale. In most of the compact models, symmetrical device structures are chosen as they simplify the mathematical analysis and modelling steps. The device structure in Fig.2 represents a rigorously scaled symmetrical DG MOSFET. The silicon film is presumed to be lightly doped and fully depleted so that the discrete dopant fluctuations are avoided. The proposed schematic considers n+ polysilicon gate so that lower threshold voltages are achieved. Both gates have identical work function, give rise to two inversion channels (top and bottom) and also switch together.

As per the work done in [18], the drain current for a fully ballistic symmetric DG MOSFET under non-equilibrium conditions is expressed as:

$$I_{ds} = 2G\left[ F_{1/2}\left( \frac{E_{fs} - E_c^{'} - E_0}{kT} \right) - F_{1/2}\left( \frac{E_{fs} - E_c^{'} - E_0}{kT} - \frac{V_{ds}}{v_T} \right) \right] \quad (1)$$

where the parameter $G = \frac{8\sqrt{2m_t}qW(kT)^{3/2}}{h^2}$. This is similar as mentioned in [9]. Eq.(1) emerges from the concept of flux theory. The significance of the above Eq.is apparent after viewing the energy band diagram of nanoscale MOSFET in Fig.3. In the schematic of Fig.3, $E_{fS}$ and $E_{fD}$ represent degenerately doped source and drain Fermi levels respectively (indicated with dash-dot lines). As per the ballistic transport theory, the highest potential barrier appears to be near the source where the electrons populate with allowed discrete sub-bands. Carriers that are confined in the inversion layer are expected to occupy discrete sub-bands with a minimum energy $E_j$ above conduction band $E_c^{'}$. Further, the energy level is represented as E=$E_c^{'}$+$E_j$+Kinetic Energy). The Eq.(1) represents the net drain to source current using one sub-band approximation (lowest being $j$=0 of unprimed valley).

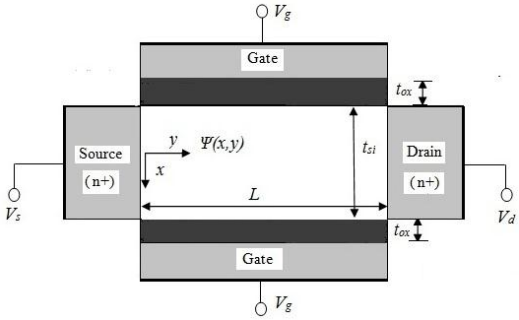


Fig.2. Schematic of the proposed symmetric Double Gate (SDG) MOSFET structure

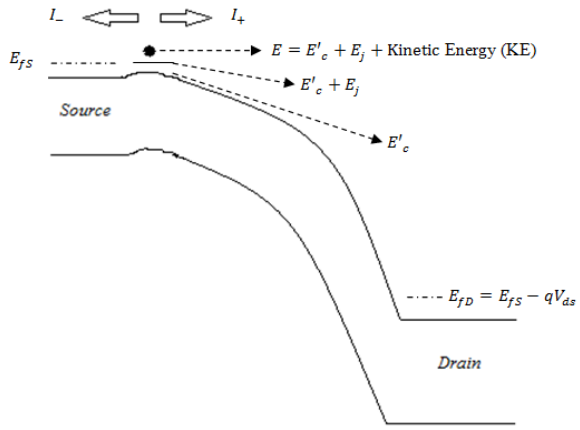


Fig.3. Schematic of a bulk nanoscale MOSFET band diagram under high-drain bias conditions [9]. For the proposed work of SDG MOSFET, a vertical mirror image of the above band diagram is to be considered due to bottom gate

Using Blakemore's explicit analytic approximation function [21], the Fermi-Dirac integral in Eq.(1) can be expressed as:

$$F_{1/2}\left( \frac{E_{fs} - E_c^{'} - E_0}{kT} \right) \approx \frac{2}{3}\left( \frac{E_{fs} - E_c^{'} - E_0}{kT} \right)^{\frac{3}{2}} \quad (2)$$

The expression in the brackets is found in [18] and is expressed here as

$$\left( \frac{E_{fs} - E_c^{'} - E_0}{kT} \right) = \ln\left[ \frac{1}{2}\left\{ \sqrt{\left( e^{\frac{v_{ds}}{v_T}} - 1 \right)^2 + 4\exp(g)} - 1 - e^{\frac{v_{ds}}{v_T}} \right\} \right] \quad (3)$$

where $g$ is an additional intermediary parameter given as:

$$G = \left( \frac{h^2 \varepsilon_{ox}\left(V_{gs} - V_t\right)}{4\pi q k T t_{ox} m_t} + \frac{V_{ds}}{v_T} \right) \quad (4)$$

In the above equations, h is the Plank's constant, $\varepsilon_{ox}$ is the gate oxide permittivity, $t_{ox}$ is the oxide layer thickness, $V_t$ is the threshold voltage, thermal voltage $v_T$=$kT/q$ and $m_t$=0.19$m_0$ where

$m_0$ is the free electron mass. The effective gate capacitance per unit area lumps together the polysilicon gate depletion effects, oxide thickness and inversion layer depth. A careful observation of the equations from Eq.(1) to Eq.(4) indicates that the fully ballistic current and conductance are independent of channel length $L$ and carrier mobility $\mu$. The current however is proportional to the channel width $W$. The drain current Eq.(1) represents the maximum current carrying ability of a fully ballistic hypothetical symmetric DG MOSFET. It is derived by ignoring all scattering processes. However, current state of art nanodevices exhibit quasi-ballistic behaviour [23]. This suggests that the maximum drain current in rigorously scaled MOSFETs is primarily controlled by quasi-ballistic carrier transport. Ballistic transport theory demands for the current evaluation at the top of the barrier. Due to the ballistic injection process, the velocity saturates at the top of the potential barrier where the vertical component of the electric field is zero. The gradual channel approximation can be applied at this position. Since modern nanoscale devices exhibit quasi-ballistic nature, the inclusion of scattering effects in terms of transmission and reflection coefficients becomes a necessity in understanding nanoscale carrier transport.

From the concepts of elementary scattering theory, the scattering equations in terms of transmission coefficient ($T_C$) and reflection coefficient ($R_C$) is given in Eq.(5) as

$$T_C+R_C=1 \tag{5}$$

where

$$T_C=\frac{\lambda}{\lambda+L} \text{ and } R_C=\frac{L}{\lambda+L} \tag{6}$$

In Eq.(6), $\lambda$ represents the mean free path of the carriers and is calculated similarly as in [18]. For simplicity, the proposed work assumes elastic scattering [24]. From Eq.(5) and Eq.(6), a straightforward relation between diffusive and ballistic transport is given. If $T_C$=1 and $L \ll \lambda$, then the transport is strongly ballistic and all injected carriers enter the drain. Else, if $T_C$=0 and $L \gg \lambda$, then the transport is drift-diffusive with significant carrier scattering.

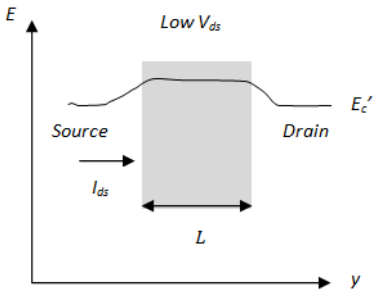


Fig.4. MOSFET band diagram under low drain bias conditions. Here $L>\lambda$ condition is considered, so that scattering is uniform throughout the channel

For realistic quasi-ballistic transport in nanoscale, the transmission co-efficient varies between 0 and 1. The device in the proposed work consists of a low field region near the source that is firmly controlled by gate voltage $V_{gs}$ and high field region near the drain that is very much controlled by drain voltage $V_{ds}$. For low drain bias, as shown in Fig.4, channel length $L$ and the mean free path $\lambda$ are sufficient to determine carrier transport with uniform scattering. However, for high drain bias conditions, the carrier scattering depends on the critical channel length $\delta$ that is positioned near the low field source region (virtual source).

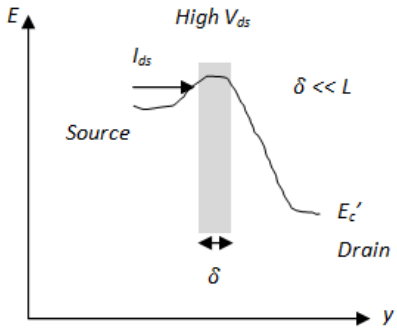


Fig.5. MOSFET band diagram under high drain bias conditions. Here $\delta \ll L$ and $\delta < \lambda$ condition is considered. Carrier scattering depends on the critical length $\delta$, near the low field source region (virtual source)

The Fig.5 suggests that the critical channel length δ at the virtual source controls the scattering and enables for the quasi-ballistic transport in nanodevices. The work done in [18] assumed arbitrary but meaningful critical channel lengths near the source end that were comparable with the carrier mean free path, just to demonstrate the quasi-ballistic nature of the drain current in a DG MOSFET. However, the critical carrier scattering channel length $\delta$ is a function of drain voltage $V_{ds}$. The proposed work provides a semi-empirical solution for determining the critical channel length $\delta$ as a function of drain bias. From Fig.5, the channel potential profile near the beginning of the channel (virtual source) can be approximated in power law form as

$$V(y)=Ky^{\left(\frac{1}{\alpha}\right)} \tag{7}$$

The Eq.(7) suggests that the potential profile curvature at the beginning of the channel depends on the parameter α, which is controlled by self-consistent electrostatics and transport model. The approximate range of $\alpha$ is estimated in two extreme cases, scattering dominated (diffusive) and scattering free (ballistic) transport in the channel [19]. Based on the value of $\alpha$ the parameter $K$ is further determined as similar in [19]. The Eq.(7) assumes that GCA applies only at the beginning of the channel. Referring to Fig.5, the potential at the top of the source channel barrier $V(0)$=0 and at the drain end of the channel $V(L)=V_{DS}$. At $y=\delta$ the potential is given as

$$V(L)=\beta v_T \tag{8}$$

In Eq.(8), $\beta \approx 1$ for non-degenerate carriers. However, carrier degeneracy at the top of the barrier increases the critical region length and hence $\beta$ becomes slightly larger than 1. Based on Eq.(7) and Eq.(8), the critical channel scattering length is given as:

$$\delta=L\left(\beta\frac{v_T}{V_{DS}}\right)^{\alpha} \tag{9}$$

Here, $\delta$ is the distance from the top of the source channel barrier to the point where the potential drops by $\beta v_T$. Eq.(7) to Eq.(9) represent the semi-empirical steps of the proposed work in determining the value of carrier scattering critical channel length

$\delta$ as a function of drain voltage. As $L \rightarrow 0$, $\delta$ becomes greater than channel length, so Eq.(9) breaks down. In such case, $\delta = L$ is assumed. For very low drain voltages, the entire channel length acts as critical channel length with uniform scattering throughout. However, for high drain voltages, the carrier scattering largely depends on the critical length $\delta$ that is positioned just near the low field source region (virtual source). This positional carrier scattering impacts the carrier transport resulting in the quasi-ballistic nature.

Based on the preceding explanation and considering the condition for the critical scattering length near virtual source as $\delta \ll L$, the transmission co-efficient term in Eq.(6) is re-written by replacing $L$ by $\delta$ and expressed in Eq.(10) as:

$$T_C = \frac{\lambda}{\lambda + \delta} \tag{10}$$

Using Eq.(10), the drain current Eq.(1) is modified and expressed in Eq.(11) as:

$$I_{ds} = 2GT_C \left[ F_{1/2}\left( \frac{E_{fs} - E_c^{'} - E_0}{kT} \right) - F_{1/2}\left( \frac{E_{fs} - E_c^{'} - E_0}{kT} - \frac{V_{ds}}{v_T} \right) \right] \tag{11}$$

The Eq.(11) represents the expression for the drain current that includes the quasi-ballistic transport and carrier degeneracy effects at nanoscale. In ultra-short channels, due to the quasi-ballistic transport, the carriers particularly diffuse above the threshold region (top of the barrier near the source) unlike a long channel where it is the drift current during high drain bias voltage. This small bottleneck region that is normally lesser than the mean free path of the carriers, limits the current in a nanoscale device. Beyond the critical scattering length $\delta$, the ballistic transport dominates. The simulation results presented in the next section demonstrate the completeness of the model in terms of current, terminal charges and capacitances.

## 3. RESULTS AND DISCUSSIONS

The results for the proposed quasi-ballistic model are presented in this section. The nanoscale DG device in Fig.2 is considered as reference. As per the scattering theory, the quasi-ballistic transport depends on the mean free path $\lambda$ and the critical carrier scattering channel length $\delta$ near the low field source region. This critical channel length $\delta$ determines the carrier scattering rate and magnitude of diffusive current present in quasi-ballistic MOSFET.

A rigorously nanoscaled n-channel symmetric Double Gate (SDG) MOSFET with the following values is considered for obtaining results: channel width $W$=1 µm, effective channel length (as per the scaling limit of DG MOSFET [25]) $L$=10 nm, silicon layer thickness $t_{si}$=5nm, oxide layer thickness t_ox=1nm, doping density of Si film $N_a = 1\times10^{12}$cm$^{-3}$, bulk electron mobility $\mu$=300cm$^2$/Vs. Effective mobility for electrons $\mu_{eff}$ is computed as a function of surface potential $\psi_s$ and gate voltage $V_{gs}$ and the same is used to estimate the mean free path $\lambda$. Further, the mean free path $\lambda$ and the thermal injection velocity $v_{therm}$ with which the electrons travel are computed as in [18] and are found to be approximately 5nm - 8nm and $1.23\times10^7$ cm/s respectively. The Fig.6 presents and compares the drain current characteristics of the proposed quasi-ballistic model with that of the fully ballistic [20] and a quasi-ballistic model mentioned in the recent work [18]. The model presented in [18] considers the carrier scattering at critical channel length $\delta$ but clearly ignores its dependency on the drain bias. The Eq.(9), Eq.(10) and Eq.(11) in the proposed work noticeably capture this drain bias dependency of $\delta$ near the low field source region. The carrier degeneracy is also considered in the described semi-empirical approach. At the critical channel length $\delta$, carriers cannot diffuse faster than the thermal injection velocity $v_{therm}$. This physical restriction limits the maximum current. Once the carriers cross the critical channel length $\delta$, the transmission becomes ballistic. If $\delta$ increases above mean free path $\lambda$ and approaches the effective channel length $L$, then the drain current scales down towards the quasi-ballistic phase with uniform scattering throughout the channel (represented by lines with star symbols in Fig.6). These results and illustrations justify that the top of the barrier (near the low field source region) characterized by critical channel length $\delta$ matters the most in nanoscale carrier transport. Further, the drain current model in Eq.(11) reflected in Fig.6 describes the quasi-ballistic transport occurring in nanoscale devices and also captures the signature effect of short channel devices with $I_{DS} \sim (V_{GS}-V_t)$ efficiently.

The Fig.7 presents the transfer characteristics exhibited by the proposed model with other relevant models as illustrated. For the completeness of a compact model, the drain current, terminal charges, conductance and capacitances should exhibit continuity. The Fig.8 and Fig.9 exhibit the variation of terminal charges with respect to drain and gate voltages respectively. The conductance and capacitances for the proposed model are calculated as in [18], along with the inclusion of drain bias dependency on the critical channel length. The variation of capacitances as a function of drain and gate voltages are shown in Fig.10 and Fig.11 respectively. In both Fig.10 and Fig.11, the capacitances represented by symbols (only) are as per the model with uniform carrier scattering throughout $L$. The capacitances represented by symbols with lines denote the aptness of the proposed model with the inclusion of scattering at critical channel length $\delta$.

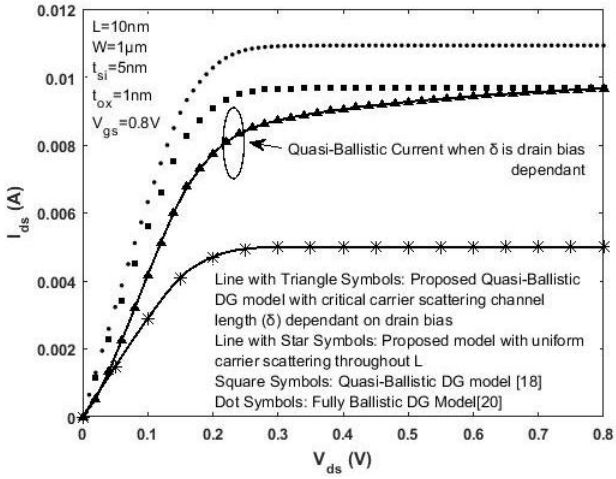


Fig.6. Drain current $I_{ds}$ as a function of $V_{ds}$ at $V_{gs}$=0.8V. The proposed model (Line with Triangle symbols) effectively includes the impact of critical channel length $\delta$ in describing the quasi-ballistic transport and also captures the signature of short channel devices. At $V_{gs}$=0.8V, critical channel length $\delta$ is found to be approximately 1.1nm. The other models [18] and [20] fail to capture the signature effect of short channel devices. The proposed model is verified with the numerical simulation results obtained using MOSFet- PADRE tool [26]

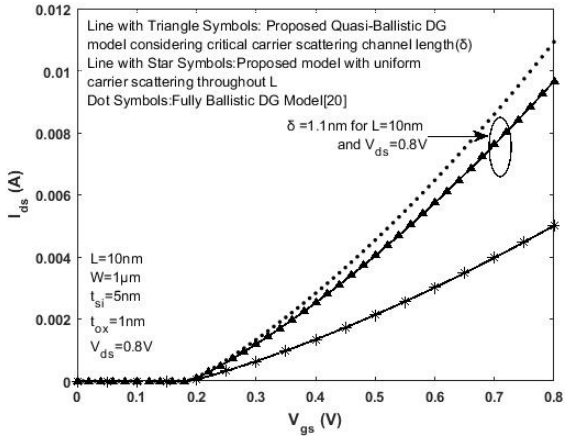


Fig.7. Drain current $I_{ds}$ as a function of $V_{gs}$ at $V_{ds}$=0.8V. The proposed model clearly shows the impact of critical channel length δ in describing quasi-ballistic transport

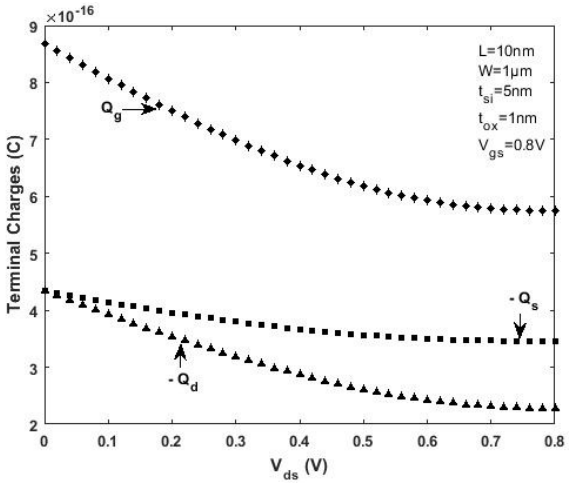


Fig.8. Terminal charges (normalized) varying as a function of drain voltage $V_{ds}$. $Q_g$ (Diamond symbols), $Q_s$ (Square symbols), $Q_d$ (Triangle symbols) represent gate, source and drain charge respectively

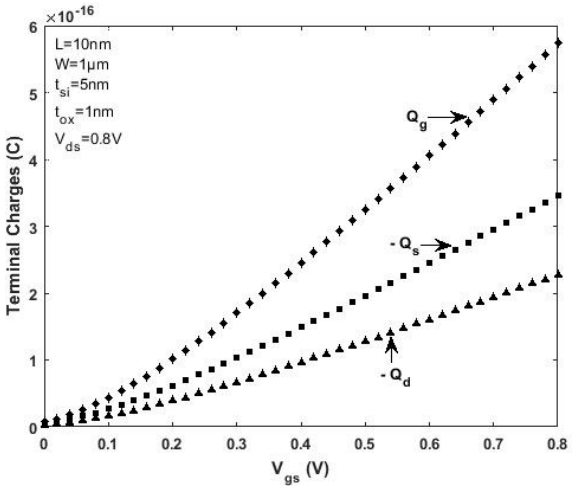


Fig.9. Terminal charges (normalized) varying as a function of gate voltage $V_{gs}$. $Q_g$ (Diamond symbols), $Q_s$ (Square symbols), $Q_d$ (Triangle symbols) represent gate, source and drain charge respectively

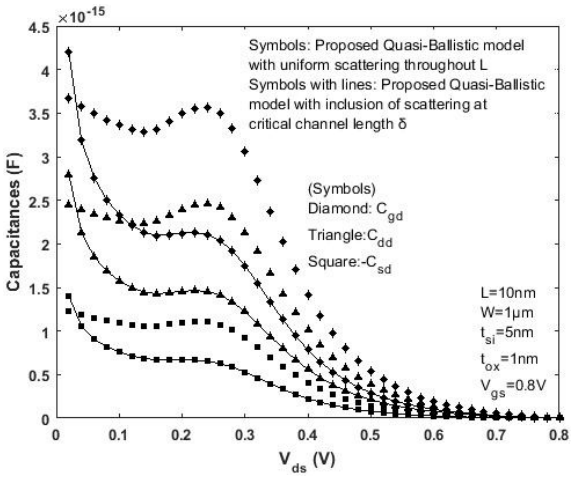


Fig.10. Capacitances $C_{gd}$, $C_{dd}$, $C_{sd}$ as a function of drain voltage $V_{ds}$. The capacitances represented by symbols (only) are as per the model with uniform scattering throughout $L$. The capacitances represented by symbols with lines signify the correctness of the proposed model with the inclusion of scattering at critical channel length $\delta$

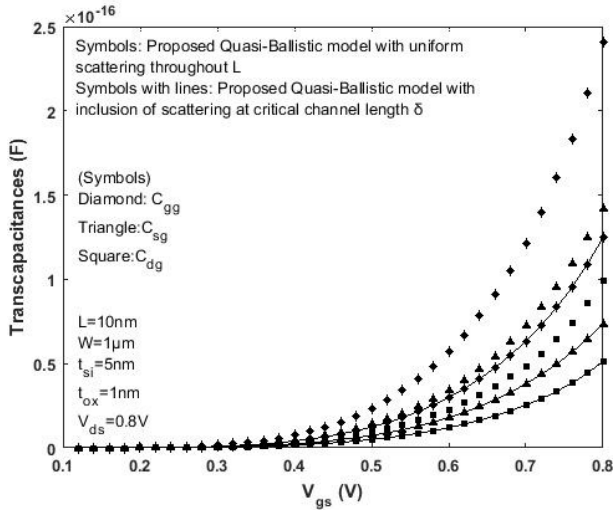


Fig.11. Transcapacitances $C_{gg}$, $C_{sg}$, $C_{dg}$ as a function of gate voltage $V_{gs}$. The transcapacitances represented by symbols (only) are as per the model with uniform scattering throughout $L$. The transcapacitances represented by symbols with lines signify the correctness of the proposed model with the inclusion of scattering at critical channel length $\delta$

The drain characteristics illustrated in Fig.12 effectively captures the signature of a short channel device. Similar to the drain current, the terminal charges and capacitances also display good continuity in all regions of device operation. The model equations are coded and simulated using MATLAB platform [26]. The proposed model is numerically verified using simulation results of MOSFet-PADRE tool [27] and [28].

The proposed quasi-ballistic model is an improvised and physically more accurate model when compared to the model presented in [18]. The semi-empirical approach presented in this work is also different from the unified model discussed in [29]. To achieve a higher performance in a nanoscale MOSFET, the low field mobility should be as high as possible. This is achieved

by ensuring that the channel doping concentration is well within low to moderate limits (unlike a conventional MOSFET), so as to reduce the scattering effects. Moreover, a higher level of degeneracy may reduce the performance of a nanoscale MOSFET and hence must be cautiously considered for inclusion in the models. To summarize, the proposed quasi-ballistic model is physically accurate, exhibits continuity and can be considered in next generation compact models.

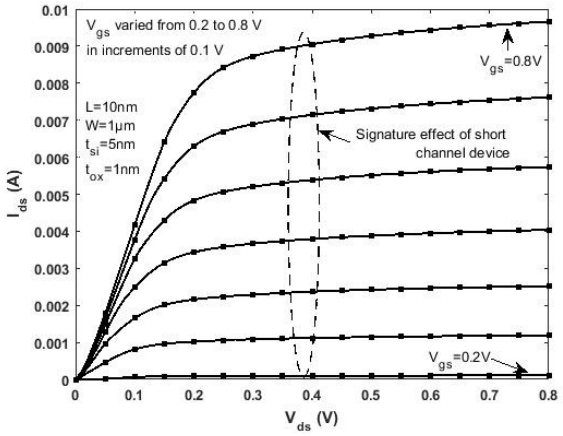


Fig.12. Drain current $I_{ds}$ as a function of $V_{ds}$ for different $V_{gs}$ values. The key signature of a short channel device is effectively captured by the proposed model

## 4. CONCLUSION

The work presents a physically accurate quasi-ballistic drain current, charge and capacitance model valid for Double Gate MOSFETs in the nanoscale limits. The proposed model includes both diffusive and ballistic carrier transport. The model presents a semi-empirical method to determine the critical channel length near the low field source region as a function of drain bias. Fermi-Dirac statistics and Carrier degeneracy are considered in this work for physical appropriateness. The obtained results illustrate that the proposed model significantly captures the signature effect of short channel devices. The proposed model is verified with the numerical simulation values obtained with MOSFet-PADRE tool. The quasi-ballistic model exhibits excellent continuity in all regions of the device operation and hence can possibly be considered in circuit simulators for next generation nanoscale modeling purposes.

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