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DESIGN OF 1KB SRAM ARRAY USING ENHANCED STABILITY 10T SRAM CELL FOR FPGA BASED APPLICATIONS

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Abstract

SRAM used for the FPGA, requires higher stability and low power consumption. 8T SRAM cell has degraded write stability with the decreasing supply voltages. 10T SRAM cell has higher write stability because of the cut-off switch employed in the pull-up path in one of the inverters. The design of SRAM array with low power consumption and higher stability is of major importance. So, 1Kb SRAM array using 8T and 10T SRAM cells has been designed and compared for different design metrics. Write 0 and Write 1 power is lower by 1.98×, 3.52× in 10T SRAM Array than 8T SRAM Array at 0.9V_{DD}, SS corner. Due to the usage of High-V_{th} transistors in 10T SRAM cell, the Read power is lower by 1.6× than 8T SRAM Array for 0.9V V_{DD} at SS Corner. The leakage power while holding 0 is lower by 1.13× in 10T SRAM array than 8T SRAM array at FF corner at 0.9V V_{DD}. The design metrics are evaluated for a wide range of supply voltage. The designs are implemented in Cadence Virtuoso in 45nm Technology node..

Keywords:

SRAM Peripherals, Power, Delay

1. INTRODUCTION

SRAM forms the major part for the implementation of portable systems, which often require low power [1]. Applications like biomedical devices, smartphones, space equipment often require low power. FPGAs use SRAM as the storage device which is used to implement digital systems [2]. FPGA became a suitable choice due to its ability to reconfigure, prototyping and parallelism. To store 1-bit data in FPGA, SRAM cell is used. FPGA comprises of Configurable Logic Blocks (CLBs) and routing switches. CLBs are again made of Look Up Tables (LUTs), Multiplexers and Flip Flops. LUT gives the respective output for a specific input combination. It is like the truth table. For example, 5 input LUT can realize 5 input Boolean function. So total for 2^5 input combinations, there will be 2^5 output values. To store each value, a 1-bit SRAM cell is required. So, to realize the 5 input LUT, 2^5 SRAM cells are required. With the growing complexity, decreasing the power consumption of a single SRAM cell is going to greatly reduce the overall power of LUT which in turn reduces the FPGA power. If the stability of the SRAM is less for lower supply voltages, then the functionality of the SRAM is disturbed which in turn affects the functionality of SRAM-based FPGA. So, the stability of SRAM cell plays a major role in reliable operation of FPGA design.

The increased usage of IoT connected devices also enables to have low power memories. The IoT enables many devices to be communicated simultaneously thereby spreading to consumer and industrial markets [3]. The connected devices work systematically using Wireless Sensor Networks (WSNs). WSN enables connection, transfer of information and data collection between the connected devices. One of the categories of WSN is Body Sensor Network (BSN). Various sensors like EEG, EMG and ECG are used to monitor the physical signals of the human body. This monitored data is then sent to the nearest medical center using the gateway [4]. The sensor nodes which monitor the physical signals of the human body are battery operated. As the sensor node needs to store the temporary data, the requirement of memory is important. On-Chip memory occupies a large portion of the system area and decides the power consumption on SoC designs.

There are many methods to decrease power consumption. However, decreasing the supply voltage has an edge over the other techniques. Scaling of supply voltage results in decreased power consumption [5]. Standby power and dynamic power have an exponential and quadratic dependence on supply voltage [6]. So, it reduces standby as well as dynamic power. But this leads to stability issues in SRAM designs during read and write operations. Also, the effect of process variations increases with lower supply voltages [7]. Reducing the leakage power of the read port can increase the I_{ON}/I_{OFF} ratio which can, in turn, allow to put a greater number of SRAM cells in a single column of SRAM array.

6T SRAM cell though widely used, suffers from read stability issues and half-select issues. 9T SRAM cell [8] though enhances the read stability compared to 6T SRAM cell, but suffers from write stability. 10T SRAM cell [9] offers independent leakage power but suffers from the half-select issue and write ability issues with declining supply voltages. SRAM cell [10] eliminates the half-select issue by introducing the stacked transistors for the access devices. The row and column-based signals for driving the access devices eliminate the half-select issue. Employment of the stacked transistors deteriorates the stability in write mode. With the declining supply voltages, this stacked effect fails the write operation at the worst process corner. PPN based SRAM cell [11] eliminates the half-select issue and enhances the write stability by employing the data-dependent feedback cutting approach. The additional PMOS is added to assist the feedback cutting approach. 9T SRAM cell [12] eliminates the half-select issue by driving the access devices with the pass transistor. Due to this, the voltage swing driving the access transistors reduces. This limits the SRAM cell operating at lower supply voltages. SRAM cells [13] with different read port topologies offer data-independent read port leakage which enhances the number of SRAM cells in a column of SRAM array. As the half-select issue pertains in the SRAM cells, the bit interleaving architecture cannot be used while designing SRAM array. 10T SRAM cell [14] uses PPN device for the inverter. It has addressed the stability in read and write modes. However, the half-select issue has not been addressed. 11T SRAM cell [15] offers lower leakage and also removes the half-select issue. But uses stacked transistors to write the data which limits the write ability with decreasing supply voltages. 12T SRAM cell [16] addresses the write ability by using data-dependent feedback which enhances the stability in write operation. The half-issue has also been addressed by using the row

and column-based signals to drive the stacked access transistors. SRAM cell [17] uses a unique topology that addresses the stability in read and write modes. SRAM cell [18] has improved write margin by employing data-dependent data cut-off during write operation. But the half-select issue has not been addressed. In addition, there are also the write assist methods which try to enhance the write stability for decreasing supply voltages but at the expense of the area.

The SRAM cells seen above may lack in write stability or half-select issue which limits its usage in SRAM Array. So, SRAM array with higher stability during the write, read and hold modes with lower power consumption is required.

The rest of the article is organized as follows. Section 2 deals with SRAM array peripherals. Section 3 deals with the 1Kb SRAM array implementation using 8T and 10T SRAM cells. Section 4 deals with various design metrics like delay, power. Section 5 concludes the paper.

2. SRAM ARRAY PERIPHERALS

SRAM array consists of SRAM cells, pre-charge circuit, row/column decoder, write driver circuits and sense amplifier.

2.1 SRAM CELL

8T and 10T SRAM cells are used to form a 1Kb array. 8T SRAM cell is shown in Fig.1. 8T SRAM cell [19] has isolated read port from the 6T SRAM cell, thereby enhancing the read stability and gives freedom to use minimum size transistor for the pull-down devices in the core cell. However, with declining supply voltages, write ability is limited. It cannot be used in bit interleaving architecture as it suffers from half-select issue. The respective concerns were addressed in 10T SRAM cell [20] which has enhanced write stability and half-select removal which enable to use the design in bit interleaving architecture. The usage of high-V_{th} devices for read port also enables low power consumption, thereby reducing the overall power consumption in an array. In the hold mode, Word Line (WL) is enabled and Column Select Signal (CSL) is disabled which turns off the access transistors NM1, NM2. So, the data already written remains. In the read mode, WL is enabled and CSL is disabled. Read Bit Line (RBL) is precharged through the precharge circuit before the read operation. Then, Read Word Line (RWL) is enabled to perform the read operation. If the data stored is 0, then there is a discharging path for RBL. So, RBL discharges indicating the data read is 0. If the data stored is 1, then there is no discharging path for RBL. So, RBL stays at the precharged V_{DD}, indicating the data read is 1. In write mode, WL is disabled and CSL is enabled which turns the access transistors ON, thereby enabling the write operation. The Data and its complement are put on the Bit Lines (BL) and BLB respectively. During Write 0, the Feedback Control Signal (FCS) is made 0, enabling the Q=V_{DD} to discharge to Gnd at faster speed resulting in write 0 operation. During Write 1, FCS is made 1, enabling the Q=0 to charge to V_{DD} at faster speed resulting in write 1 operation. The absence of a pull-down NMOS device in the right inverter enables QB to discharge at a faster pace which in turn enables Q to charge to V_{DD} at a faster pace.

The 10T SRAM cell is superior in stability and removes half-select issue compared to 8T SRAM cell. 10T SRAM cell is shown in Fig.2. The 10T SRAM cell has superior Hold Static Noise Margin, Read Static Noise Margin and Write Margin than 8T SRAM cell. Due to the usage of the cross-point selection for write operation in 10T SRAM cell, the half-select issue is resolved. The data stored in row and column selected SRAM cells in the array does not get affected. So, the stability of the row and column half-selected cells does not deteriorate. The variability of the HSNM, RSNM and WM in 10T SRAM cell is also less indicating robustness to the Process-Voltage-Temperature (PVT) Variations compared to the 8T SRAM cell [20].

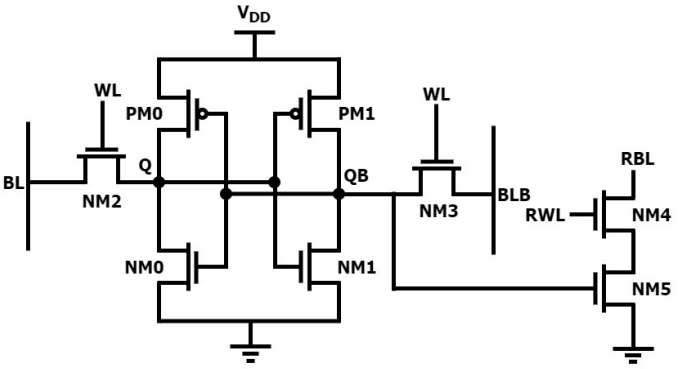

Fig.1. 8T SRAM Cell

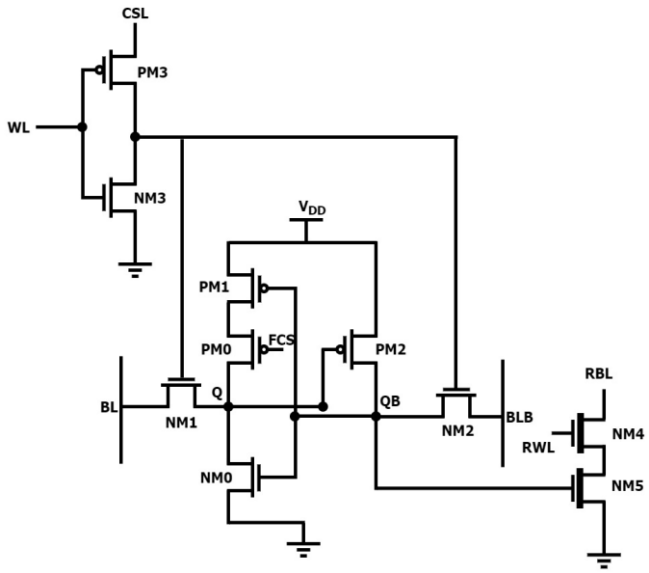

Fig.2. 10T SRAM Cell

2.2 DECODERS

As an array is a two dimensional, a row and column decoder are used to access the SRAM cell. Basing on the address lines given to the decoders the respective SRAM cell will be selected, thereby performing either write or read operation. Decoder consists of n inputs, 2^n outputs and an enable signal. The output of the Row decoders are used to drive the Word Lines. For a particular input combination, the respective output is enabled driving the word lines. The implementation of 5×32 decoder is shown in Fig.3.

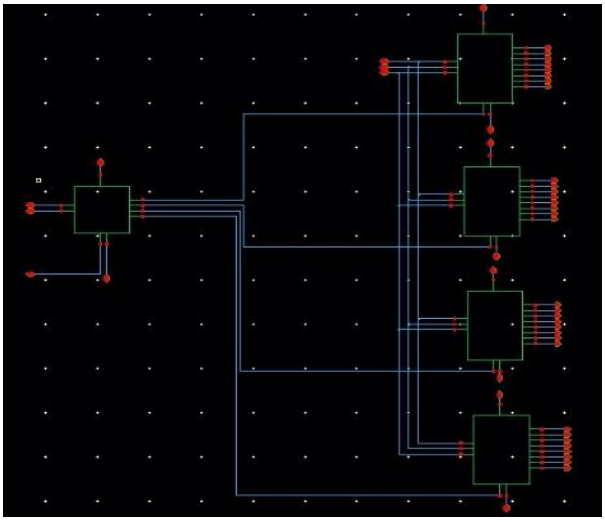

Fig.3. 5×32 Decoder

2.3 PRECHARGE CIRCUIT

A precharge circuit is used to precharge the bit lines before read and write operations. The precharge circuit is constructed using the PMOS Devices. The BL and BLB are precharged using the precharge circuit. To precharge the RBL, a separate PMOS transistor is used. The precharge circuit used to precharge BL and BLB lines are shown in Fig.4. When the precharge signal is low, the bit lines get precharge to $V_{DD.}$ Later it is made high to disable it during read and write operations.

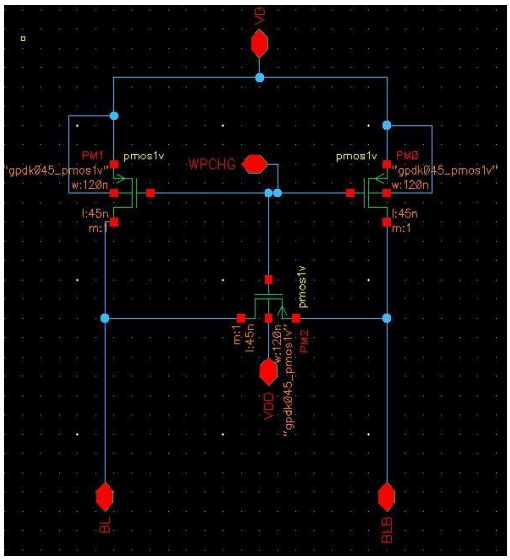

Fig.4. Precharge Circuit

2.4 WRITE DRIVER

The bit lines are precharged to V_{DD} before the write operation. Write driver pulls one of the precharged bit lines to Gnd depending upon the data to be written. The implementation of write driver is shown in Fig.5. If the data to be written in to the SRAM cell is 0, then the write driver pulls down the BL to Gnd and BLB stays at V_{DD}. If the data to be written into the SRAM cell is 1, then the write driver pulls down the BLB to Gnd and BL stays at V_{DD}. The respective SRAM cell, after enabling the word line, writes the respective data into the storage nodes through the access transistors.

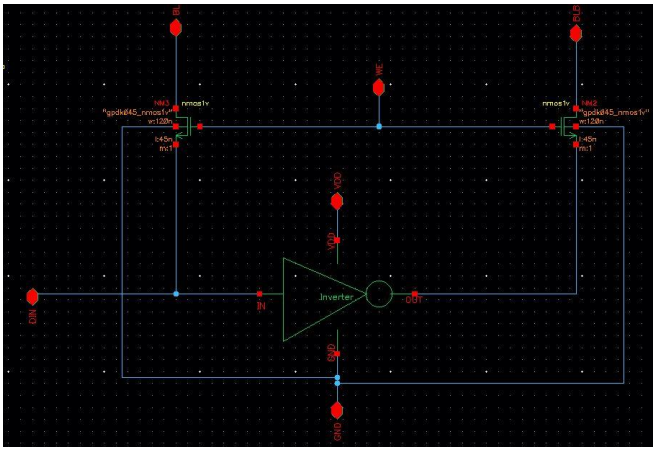

Fig.5. Write Driver

2.5 SENSE AMPLIFIER

Sense amplifier senses the change in the read bit line. Before the read operation, the Read bit line (RBL) is Precharged to $V_{DD.}$ During the read operation, after enabling the Read Word Line (RWL), basing on the data stored in the SRAM cell, the RBL either stays at V_{DD} or discharges to Gnd. These changes in the RBL is sensed by the Sense amplifier which gives the output. In an SRAM array, each column requires one sense amplifier connected to RBL. Inverters are used to sense the changes in the RBL signal during the read operation.

2.6 CONTROL CIRCUIT FOR 10T SRAM CELL

In order to generate the control signals (FCS, CSL) in 10T SRAM cell, control circuitry is used. FCS and CSL control signals vary during different modes of SRAM cell operation. The implementation of control circuit for 10T SRAM cell is shown in Fig.6.

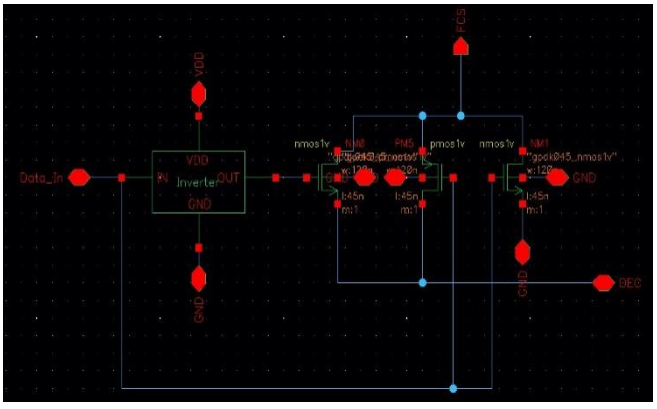

Fig.6. Control Circuit for 10T SRAM cell

3. SRAM ARRAY USING 8T AND 10T SRAM CELLS

1Kb SRAM array is designed using 8T and 10T SRAM cells. 1Kb SRAM consists of 1024 SRAM cells. So, a 32×32 2-

Dimensional array is formed. 5×32 row decoder drives the word lines RWL and WL in 8T and 10T SRAM array. Precharge circuits are used to precharge the bit lines BL, BLB and RBL. Write driver is connected to the bit lines BL, BLB to put the respective data on the bit lines. WL, RWL in both the SRAM cells are Row driven by the decoders. RBL in both the SRAM cells are Column signals. Fig.7 shows the implementation of 1Kb SRAM using 8T SRAM cell.

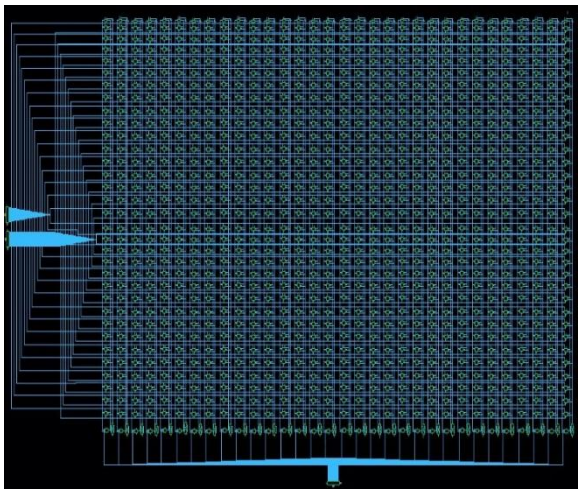

Fig.7. 1Kb 8T SRAM Array

The Fig.8 shows the implementation of 1Kb SRAM using 10T SRAM cell. In 10T SRAM array, the FCS control signal is generated based on the Data input and the column decoder output. The CSL signal is generated from the column decoder.

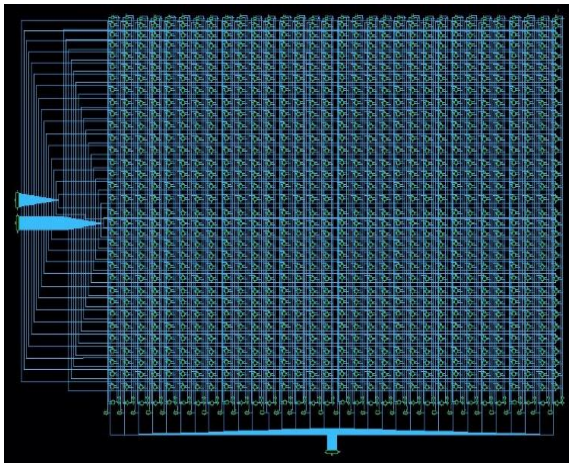

Fig.8. 1Kb 10T SRAM Array

4. RESULTS AND DISCUSSION

The SRAM array has been implemented in Cadence Virtuoso in 45nm technology. Different design metrics have been calculated and compared to evaluate the design's usage based on applications.

4.1 WRITE DELAY AND POWER

Write Delay has been calculated from the moment when Write Enable is active to the moment when the storage node reaches either 90% or falls to 10% in write 1 and write 0 cases respectively. The power consumed during write operation is the write power.

The Fig.9 and Fig.10 plots the write 0/1 delay for varying V_{DD} at SS corner. 8T SRAM cell has better write performance than 10T SRAM when operated in an array. 10T SRAM cell has lower power consumption than 8T SRAM when operated in an array for a wide range of supply voltages. Write 0 and Write 1 power is lower by 1.98×, 3.52× in 10T SRAM Array than 8T SRAM Array at $0.9V_{DD}$, SS corner.

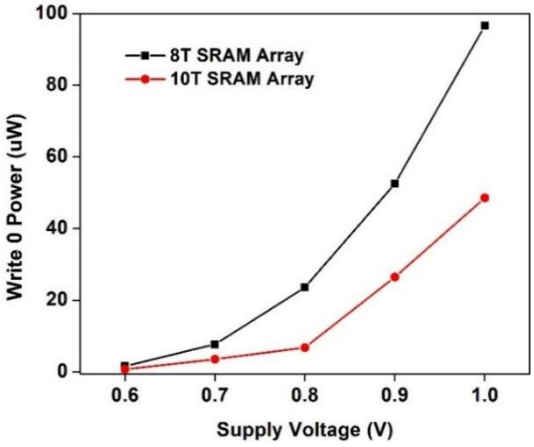

Fig.9. Write 0 Power for varying V_{DD} at SS corner

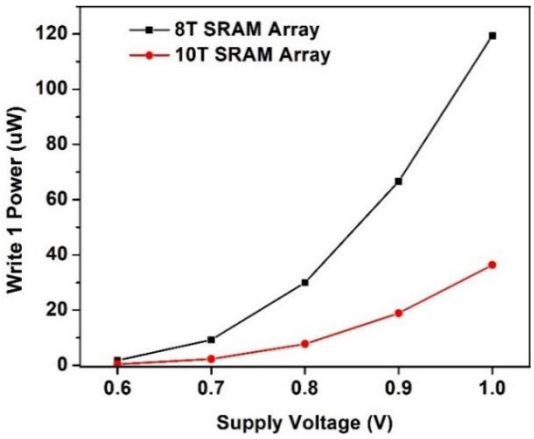

Fig.10. Write 1 Power for varying V_{DD} at SS corner

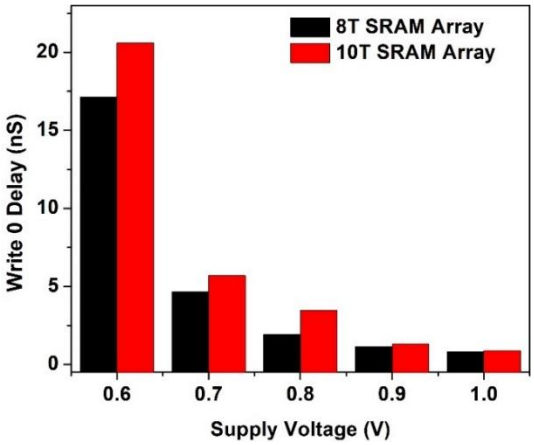

Fig.11. Write 0 Delay for varying V_{DD} at SS corner

The Fig.11 and Fig.12 show the write 0/1 delay for different supply voltages. However, 10T SRAM array has a higher write 0 delay by 1.15× and write 1 delay by 1.37× compared to the 10T SRAM array.

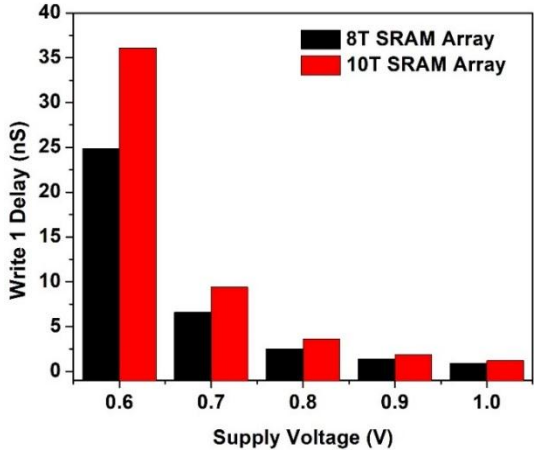

Fig.12. Write 1 Delay for varying V_{DD} at SS corner

4.2 READ DELAY AND POWER

Read Delay has been calculated from the moment when Read Enable is active to the moment when the Data out reaches 50% of the V_{DD}. The power consumed during the read operation is read power. Fig.13 and Fig.14 show the comparison of Read Delay and Read Power for 8T and 10T SRAM array for varying V_{DD} at SS corner. Due to the usage of High-V_{th} devices in the read port of 10T SRAM, there is a high delay and low power than 10T SRAM.

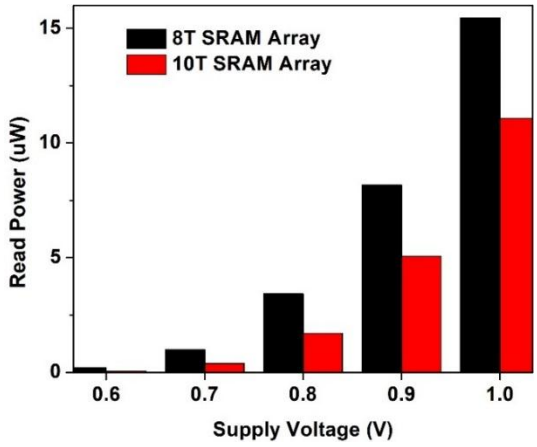

Fig.13. Read Power for varying V_{DD} at SS corner

The Read power is lower by 2.0× for 10T SRAM array than 8T SRAM array for 0.9V supply voltage at SS Corner. The read power for different supply voltages proves to be low for 10T SRAM array than the 8T SRAM array. However, read delay is increased by 1.73× for 10T SRAM array than 8T SRAM array for 0.9V V_{DD} at SS Corner.

4.3 LEAKAGE POWER

It is the power consumed while the SRAM array has been operating in standby mode of operation [21]. The comparison of leakage power for holding 0 and 1 for various supply voltages are plotted in Fig.15 and Fig.16.

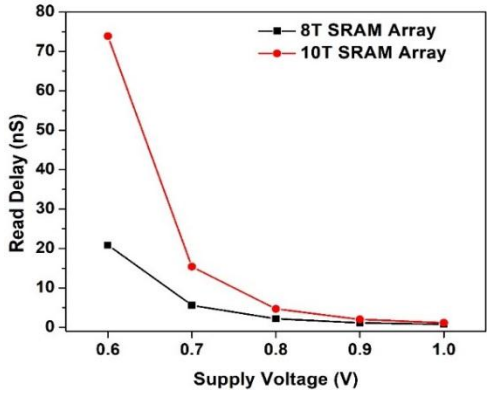

Fig.14. Read Delay for varying V_{DD} at SS corner

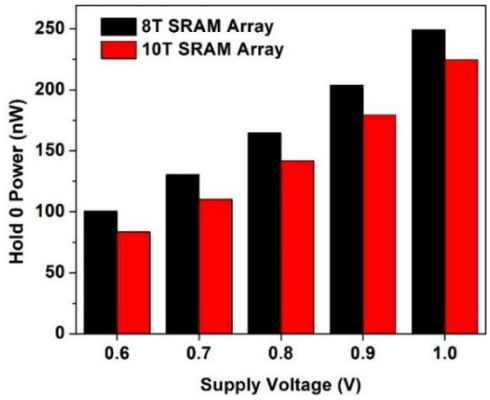

Fig.15. Hold 0 Power for varying V_{DD} at FF corner

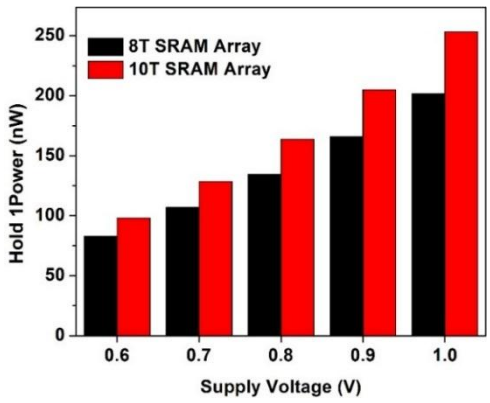

Fig.16. Hold 1 Power for varying V_{DD} at FF corner

The leakage power while holding 0 in 10T SRAM array is lower by 1.16× than 8T SRAM array at FF corner at 0.9V $V_{DD.}$ However, leakage power during hold 1 is large by 1.23× than 8T SRAM array at FF corner at 0.9V V_{DD}. As most of the SRAM cells operate in standby or hold mode, the reduction of leakage power or hold power is of major importance in an SRAM array.

5. CONCLUSION

SRAM forms a crucial block in computing systems that require low power consumption enabling longer life for the battery. To implement digital systems, often FPGA is used due to its features. FPGA comprises of CLBs which in turn is made up of LUTs comprising SRAM cells. So, SRAM is of major

importance in deciding the overall performance, power consumption and stability of FPGA. The various design metrics for the SRAM array has been evaluated at the worst corners. SRAM array using 10T SRAM cell proves to be the preferred choice over 8T SRAM cell due to the lower power consumption in read and write modes of operation. The leakage power while holding 0 is also lower compared to the counterpart.

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