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DESIGN AND FPGA IMPLEMENTATION RING OSCILLATOR USING FINFET TECHNIQUES

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Abstract

This paper presents a new technique to improve performance in terms of low power dissipation of FinFET ring oscillator.5 stage ring oscillator have designed under the concept of FinFET technique. FinFET provides better performance than normal CMOS technology. The presentation of FinFET (FIN type field effect transistor) Technology has opened new parts in Nano-innovation. Arrangement of ultrathin fin enables suppressed short channel effects it is an appealing replacement to the single gate MOSFET by virtue of its superior electrostatic properties and comparative ease of manufacturability. Having reduction of short channel effects in submicron region and making transistors still scalable. Because of this reason, the small- length transistor can have a better intrinsic gain compared to the majority counterpart. Simulation results indicates that using FinFET technique to the ring oscillator having power dissipation of 0.135mwatt power and CMOS ring oscillator provides 0.232 mwatt. I_{on} current for CMOS ring oscillator is 10.632mA whereas FinFET Ring oscillator provides 0.381mA.

Keywords:

FinFET Technique, Ring Oscillator, CMOS Technology

1. INTRODUCTION

The performance of electron devices has been increased after the invention FinFET technology. As compared to CMOS technology, FinFET technology offers low power consumption, reduces short channel effect, reducing Drain Induced Barrier Leakages (DIBL) and also reduces second order effects. The FinFET devices have appreciably quicker switching times and greater current density than planar CMOS technology. FinFET have two different structures. Double gate FinFETs and short gate FinFETs. In FinFET, a thin silicon layer covered over the conducting channel forms the body. Due to scaling down the dimension of MOS transistor, the size of MOS transistor is reduced this will lead to small geometry problems which makes effects in characteristics of devices and modeling. Basically in MOS transistor it consists of three major terminals Gate, Drain and Source. The drain voltages V_{ds} producing an electric field that changes the threshold voltages. In short channel, the threshold voltage is reduced because of increasing drain voltage. This effect is known as Drain Induced Barrier Lowering (DIBL) it can be represented by:

$$V_t = V_{t0} - \lambda V_{ds}$$

where λ is the coefficient of DIBL, in the order of 0.1. V_t is the threshold voltage and v_{t0} is threshold voltage when the source is at body potential. One of the main drawbacks for DIBL is increasing sub threshold leakages for high value of V_{ds}. This will affect for designing digital circuits. So these kinds of second order effects can be reduced with the help of FinFET technology.

FinFET is a non-planar device. Single FinFET device consists of multiple fins, located side by side and all are wrapped by same gate. The less impurity concentration in the fin give results in less channel dispersion when the device is active, increasing the carrier mobility and device current. The performance of the device can be measured by power analysis. Sub threshold leakage power increases exponentially when threshold voltages decreases. Small change in gate voltage will reduce leakage current by the order of 10.so FinFET technology provides much less power consumption than Planar CMOS technology. According to the details International Technology Roadmap for Semiconductors (ITRS), the device gate length can be scaled down to below 3nm in the year of 2022. For nano meter scaling FinFET technology more suitable than CMOS technology. FinFET fabrication process follows the steps: first and foremost step is to prepare substrate formation; this is the base of the FinFET. Second step is etching process where fins are formed by anisotropic etch process method. This layer is available in Silicon On insulator (SOI) models. After etching process next step is oxide deposition in which more aspect ratio is needed to separate fins from each other. After completing oxidization next process is planarization, followed by recess etching, gate oxide formation and deposition of gate.

This paper deals the concept of 5 stage of Ring oscillator can be designed using FinFET technology.

Organization of the paper follows: It has 4 major sections. Section 1 provides the details of Introduction of FinFET techniques. Section 2 provides the details about ring oscillator. Subsection of 2.1 and 2.2 gives the details regarding layout design both CMOS and FinFET technology. Section 3 shows that the experimental results and performance analysis of inverter and Ring oscillator. Section 4 provides the conclusion and future scope details.

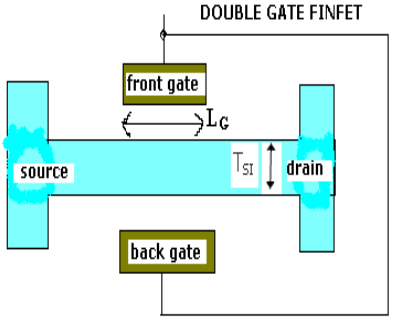

Fig.1. Double gate FinFET

FinFET technology offers two structures as mentioned earlier, double gate or independent gate, front gate and back gate both are electrically independent. The back gate bias can be used to change the threshold voltage. The Fig.2 shows the symbol of double gate.

The Fig.3 provides the symbol of shorted gate. In shorted gate both the gates are connected together to drive the device on. Shorted gate provides much higher value of OFF current (I_{OFF}) of the device than in double gate. But independent gate provides change in threshold voltage due to back gate bias. So that device leakages can be controlled with the help of double gate structure.

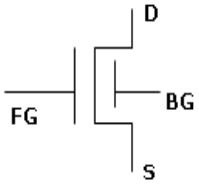

Fig.2. Double Gate Symbol

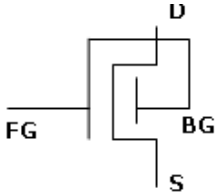

Fig.3. Shorted Gate symbol

The FinFET channel width can be calculated in terms of fin height and fin width [1].

$$\text{Channel width} = N\,(2\times Fin\ Height + Fin\ Width) \quad (1)$$

where N indicates number of fins associated in the structure. *Fin width* indicates the thickness of fin and *fin height* is the height of the fin.

2. RING OSCILLATOR

In this section, provides the information regarding ring oscillator. A ring oscillator is an odd number (N) of inverters joined in sequence with the feedback connection as shown in Fig.1. A ring oscillator also provides with combination of inverting and non-inverting stages, finally the inverting block is odd number. The VCO is constructed from ring oscillator. Jitter of ring oscillators is mostly used in hardware arbitrary number generators. A ring oscillator is used to determine the property of temperature and voltage on a chip. The frequency of oscillation is inversely proportional to the number of inverter and the propagation delay times.

For improving better performances FinFET technology is used in this paper. The Fig.2 shows that five stages of ring oscillator. The frequency of the ring oscillator depends upon the propagation delay τ_p.

$$\text{Frequency} = 0.5N\tau_p \quad (2)$$

where N is the number of inverter.

Due to this delay time τ_p of every stage the entire circuit suddenly starts oscillating at a certain frequency. If the oscillator is made up of single inverter, then the oscillations and gain are not adequate. If the oscillator is designed with two inverters, then the gain and oscillation are much higher than single inverter. So this five-stage oscillator has five inverters that are connected in the form of series with a positive feedback system. So the oscillations & the gain of the system are efficient. This is the reason to choose the five-stage oscillator.

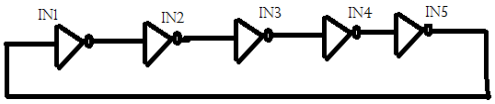

Fig.4. 5 stage ring oscillator

The output of the final stage is connected back to the input. Oscillator must satisfy the Barkhausen criteria $A^*\beta$ = -1. The magnitude of loop gain should be one and phase of loop gain should be unity. The Fig.4 shows that five stages of ring oscillator implemented in CMOS technology. It is the combination of pMOS and nMOS connected in series manner. The output of the first inverter is connected to the input of the next inverter. Finally the last inverter output connected back to the input of first inverter.

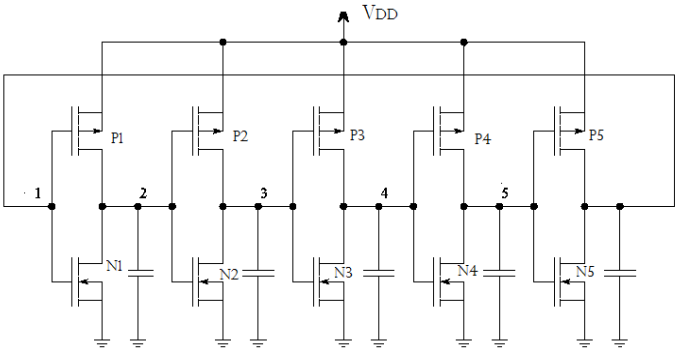

Fig.5. CMOS Ring oscillator

Five stage of ring oscillator is designed in that pMOS and nMOS are connected with the help of polysilicon (RED) and metal (BLUE) are used to connect source and drain of pMOS and nMOS. Output is given as input to next stage. Metal contacts are indicated by BLACK color coding. Each and every pMOS circuit is covered by implant. Poly silicon, active and metal can be used for interconnecting wires. Polysilicon has much higher resistivity than active.

Layout of ring oscillator is designed with the help of microwind tool. The design was implemented because of the some parameters might helpful to reduce the power optimization.

- The size of the inverter kept small.
- It provides much higher I_{on} current.
- High supply voltages can be used to reduce static leakages

2.1 LAYOUT OF INVERTER (CMOS &FINFET)

Inverter is the basic unit for any combinational and sequential circuit. Normally pMOS and nMOS connected in series to make inverter. Both the gates of pMOS and nMOS are connected together to apply input signal. The Fig.6 shows that the layout of inverter. The structure of inverter is pMOS and nMOS are connected in series whereas drain of pMOS is applied to power supply V_{dd} and source of nMOS is connected to ground V_{ss}.

Separate V_{dd} is given for implant which is entirely covering pMOS. The switching speed of nMOS is higher than pMOS due to high mobility of electrons, for improving better rise time, the aspect ratio of pMOS is double the value of nMOS. The input is applied to common to both the gates and output is measured at

that point where the source of pMOS and drain of nMOS are combined.

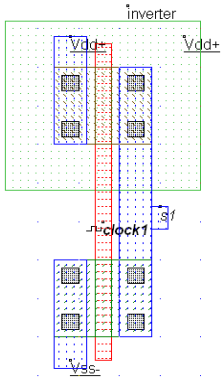

Fig.6. Layout of inverter

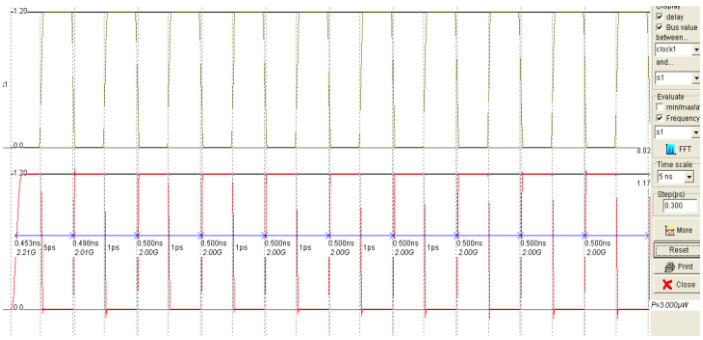

Fig.7. Output of inverter

The output of the inverter is V_{out} = -V_{in}. The Layout of FinFET inverter reduces scalability. In FinFET technique gate oxide tunneling drain to substrate and source to substrate conduction can be minimized. The Fig.7 shows output of inverter having power dissipation of 3µw power and delay is 0.453ns.

2.2 LAYOUT OF FINFET RING OSCILLATOR

The layout design of FinFET Ring oscillator is shown in Fig.8. This layout is implemented by using FinFET technique. Three fins were developed between source and drain. V_{dd} power supply is applied at pMOS transistor and V_{ss} is applied at nMOS transistors. Output of fifth inverter connected as input to the first inverter to make feedback connection. Ring oscillator can be used to measure the analysis of temperature and voltage on chip. During the stage of wafer testing this oscillator is needed. For designing frequency synthesizer ring oscillators are needed.

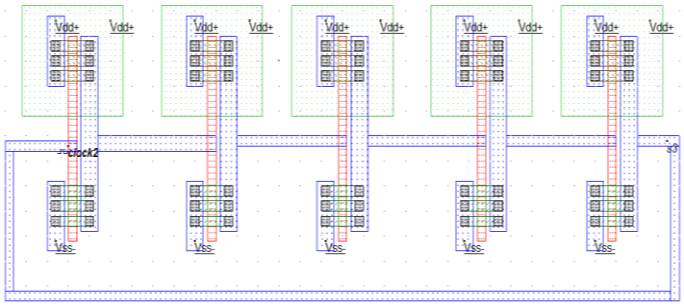

Fig.8. Layout of FinFET Ring oscillator

3. PERFORMANCE ANALYSIS

The important design considerations in nano meter device process are power analysis, delay estimation and leakages. The wide range and low power ring oscillator is designed in this paper. In analysis of below 45nm process, the thickness of gate oxide reduces to the point that gate leakage provides comparable to sub threshold leakages. The sub threshold leakages can be reduced with the help of FinFET technology, the experimental results shows that leakages can be minimized. The CMOS NOT gate is designed and observed the power dissipation is 0.599µW. whereas FinFET NOT gate has power dissipation of 0.072µW. FinFET technique to the ring oscillator having power dissipation of 0.135 mwatt power and CMOS ring oscillator provides 0.232 mwatt. I_{on} current for CMOS ring oscillator is 10.632mA whereas FinFET Ring oscillator provides 0.381mA. The Fig.9 shows that waveform for NOT gate designed by CMOS technology.

The Fig.10 shows the waveform of FinFET inverter. The Fig.11 and Fig.12 shows the I_{on} current analysis for ring oscillator as well as FinFET ring oscillator.

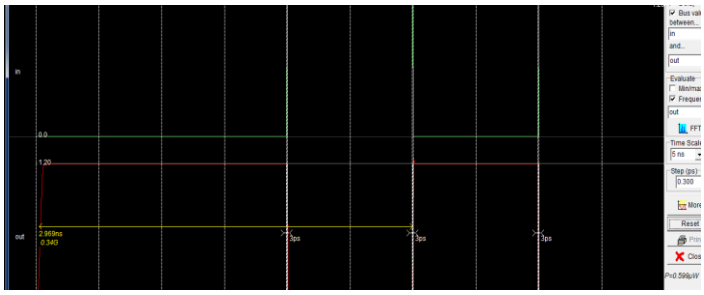

Fig.9. Inverter

The Fig.9 shows that the output of inverter which provides the power dissipation of 0.599 microwatt power. Power dissipation can be calculated by three parameters such as power supply, frequency and capacitance. Dynamic power dissipation can be measured by

$$P = CV_{DD}^2 f$$

where P is power dissipation, C is capacitance of the device, V_{DD} is the supply voltage, f is the frequency.

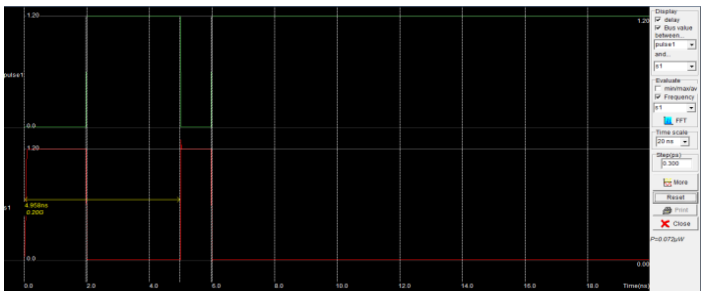

Fig.10. FinFET inverter

FinFET inverter provides a power dissipation of 0.072µw power which is very much less as compared with normal inverter technique. From the above analysis and simulation result shows that FinFET technology provides much better performance than planar CMOS technology. Not only in terms of power, the size of the device also reduces and switching activity improves. FinFET offering greater reduction of sub threshold leakage current.

Leakage power is further reduced with the help of FinFET technology. This paper, we have designed five stage of Ring oscillator offering lower leakage and better power consumption. Sub threshold leakage and threshold voltage variation is the important parameter to analyze the device characteristics and electrical behaviors, so a FinFET technique helps to improve the device performances.

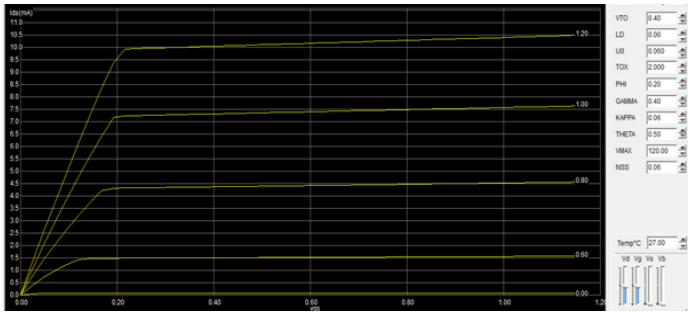

Fig.11. I_{on} current analysis for ring oscillator

I_{on} current analysis is characterized by BSIM simulator. BSIM simulator is suitable for digital circuits. This model includes the I-V characteristics for sub threshold, linear and non-linear regions. The oscillation period of five stage ring oscillator is given as follows:

$$T=2\tau p + 2\tau p + 2\tau p + 2\tau p + 2\tau p = 10\tau p$$

where τp is the average propagation delay.

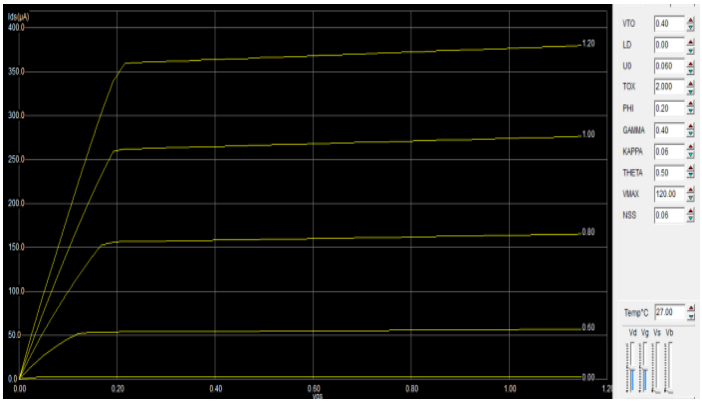

Fig.12. Ion current analysis for FinFET ring oscillator

Table.1. Parameters of FinFET

Parameters	Inverter	FinFET inverter	Ring oscillator	FinFET ring oscillator
Power dissipation	0.599µW	0.072µW	0.232mwatt	0.135mwatt
I_{on} current	0.381mA	0.203mA	10.632mA	0.324mA

On comparing the simulation results shown in Fig.11 and Fig.12. FinFET structure shows less power compared with CMOS structure. This simulation results shows that more than 50% power can be saved. The Table.1 gives the details for various parameter like power dissipation and I_{on} current for inverter, FinFET Inverter, ring oscillator and FinFET ring oscillator.

The power, performance and area are the important parameters for VLSI deign. As compared with two different methodologies FinFET techniques gives better performances.

4. CONCLUSION

Simulation result in this paper provides that five stage Ring oscillator have designed using FinFET technology and compared the result with CMOS technology. FinFET Ring oscillator provides better performance in term of power dissipation and Ion current analysis. Short channel effect, second order effects and area can be minimized with the help of FinFET techniques. FinFET Ring oscillator provides 0.135mwatt power and CMOS Ring oscillator has 0.232mwatt power. FinFET technology not only offering low power consumption, it will reduces the second order effects such as channel length modulation, Drain-induced barrier-lowering, punch through and sub threshold conduction.

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