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EFFICIENT DESIGN OF LVDS TRANSMITTER IN COMPLIANCE WITH IEEE STANDARD 1596.3-1996

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Abstract

Ever increasing processing speed of microprocessors motherboards, optical transmission links, intelligent hubs and routers etc., is pushing the off-chip data rate into the gigabits-per-second range. The LVDS ((low-voltage differential signaling) is used as an interface for avionic communications, surveillance and intelligence where it protects the integrity of the transmitted signals. The main application of LVDS finds in chip to chip I/O communication. Increasing the data rate along with reductions in circuit power and chip area are major concern of high performance I/O's to enable very high levels of silicon integration. The effective solution is proposed here to enable multi-giga-bit transmission with efficient design of LVDS. Proposed design meets the specified characteristics through DC and AC analysis with PVT analysis including all process corner variations.

Keywords:

LVDS, Level Shifter, Pre-Driver, Driver, Signaling, Transient Analysis

1. INTRODUCTION

Optical increasing the processing speed of computational systems is ever increasing day by day coping with advancements in technologies. These devices pushing the off-chip data rate into the gigabits-per-second range. However, unlike internal clocks, chip-to-board signalling gains little benefit in terms of operating frequency from the increased silicon integration. While the reduction of the power consumption is the great concern in battery-powered portable systems, it is also required in other systems to reduce the costs related to packaging and additional cooling systems. Low-voltage differential signaling (LVDS) is a signaling method used for high-speed transmission of binary data over copper. It has advantage of balanced data transmission begin to outweigh the costs over single-ended techniques when signal transition times approach 10ns. This represents signaling rates of about 30 Mbps or clock rates of 60 MHz (in single-edge clocking systems) and above. The low-voltage swing and differential current mode outputs significantly reduce electromagnetic interference (EMI). These outputs have fast edge rates that cause signal paths to act as transmission lines. Therefore, ultra-high-speed board design and differential signal theory knowledge is especially useful for designing I/O blocks of board. LVDS was introduced in the year 1994. LVDS works with both serial and parallel data transmission. LVDS has become the solution for many applications that demand low power consumption and high noise immunity for high data rates. Since its standardization under ANSI/TIA/EIA-644, LVDS has been implemented in a diverse set of applications and industries. IEEE Std 1596.3-1996, an extension to IEEE Std 1596-1992, has defined a lower-voltage differential signal (as low as 250 mV swing) that is compatible with low-voltage CMOS, Bi-CMOS, and GaAs circuitry. The base specification of differential ECL signal provides high transfer rate (16 bits are transferred every 2 ns) of LVDS are well defined. The design of LVDS working at 2 Gbps is explained in [2]. In [3], different architectures of the drivers like Typical LVDS driver: (a) Macro model and (b) Transistor and low-voltage are well addressed. The proposed work [4] describes things like general applicability, electrical characteristics and data signalling rate of a low voltage differential signalling standard.

The proposed LVDS design is considered with objectives defined in section 2 using Cadence virtuoso software. The section also discusses the block diagram of LVDS transmitter. Section 3 describes the schematic design of LVDS transmitter and its parts. Transient analysis results of the LVDS transmitter and its parts are plotted in section 4. Next Section summarises the proposed work.

2. LVDS TRANSMITTER BLOCK

The LVDS transmitter circuit consists of level shifter, logic block, pre driver (to operate at higher frequencies) and driver along with the termination resistance of standard (100Ω). LVDS is used as an interface for avionic communications, surveillance and intelligence where it protects the integrity of the transmitted signals, and is also used in software defined radio devices. The design objectives of the proposed LVDS Transmitter in compliance with IEEESTD. 1596.3-1996 are as specified in the Table.1. The main specification of the LVDS transmitter involves the designing of signalling standard to drive maximum output voltage swing of 1.5V with maximum output impedance of 400 Ohms load.

2.1 LVDS TRANSMITTER SPECIFICATIONS

The block diagram of the transmitter contains the part of signals from the inner core and are converted to differential signals first. Then, the differential signals are fed into a level shifter due to the different power supply between inner core circuit and LVDSI/O driver. Level shifter circuit is needed to accomplish the signal level conversion. Then the signal drive capability of the converted signal is enhanced, usually by inverter buffer chain whose dimensions increase gradually. The block diagram of the transmitter and detailed LVDS transmitter are shown in Fig.1 and Fig.2.

Table.1. Design Objectives of proposed LVDS Transmitter

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	High Output Voltage	R_{Load} = 100Ω±1%		1475	mV
V_{OL}	Low Output Voltage	R_{Load} = 100Ω±1%	925		mV
$\|V_{od}\|$	Output Differential Voltage	R_{Load} = 100Ω±1%	250	400	mV

V_{os}	Output Offset Voltage	R_{Load} = 100Ω±1%	925		mV
R_0	Output Impedance, single ended	V_{cm} = 1.0V and 1.4V	40	140	Ω
ΔR_0	R_0 mismatch between *A* and *B*	V_{cm} = 1.0V and 1.4V		10	%
$\|\Delta V_{od}\|$	Change in $\|V_{od}\|$ between 0 and 1	R_{Load} = 100Ω±1%		25	mV
ΔV_{os}	Change in V_{os} between 0 and 1	R_{Load} = 100Ω±1%		25	mV
I_{sa},I_{sb}	Output Current	Driver shorted to ground		40	mA
I_{sab}	Output Current	Drivers shorted together		12	mA
$\|I_{xa}\|$,$\|I_{xb}\|$	Power-off output leakage current	V_{cc} = 0V		10	mA

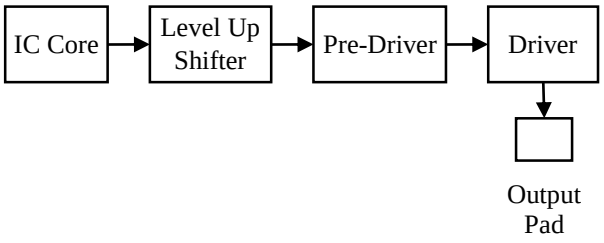

Fig.1. Block Diagram of Transmitter

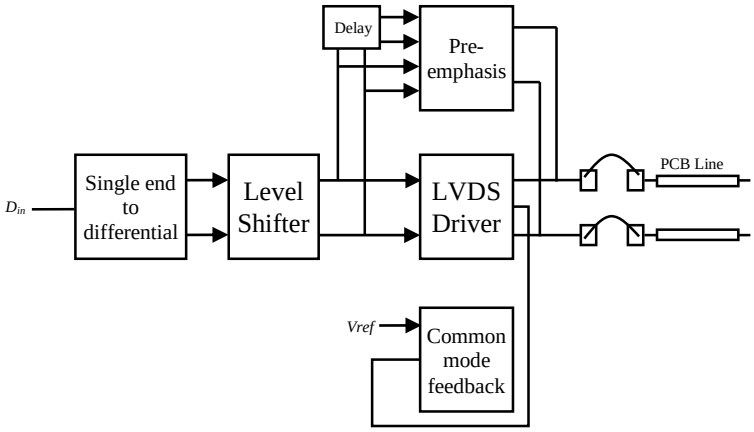

Fig.2. Detailed Block Diagram of LVDS Transmitter

2.2 LVDS TRANSMITTER DESIGN FLOW

The proposed LVDS transmitter is designed as per specifications listed in Table.1 and design procedure of transmitter and the blocks using Cadence virtuoso software is shown in Fig.3.

3. SCHEMATIC DESIGN OF LVDS TRANSMITTER AND ITS BLOCKS

In LVDS transmitter, the first block is conversion of single ended to differential signal conversion. Next the proposed work deals with design of level shifter, pre-driver, driver and control block. The schematic design of all the blocks are discussed in the Fig.4-Fig.6.

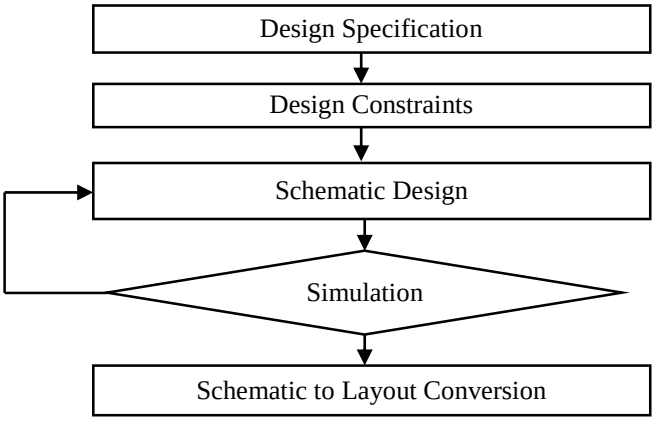

Fig.3. Design Flow LVDS transmitter and its blocks

3.1 SCHEMATIC OF LEVEL SHIFTER

There is different power supply between the core and I/O driver circuit the level shifter is used as converter for required voltage levels.

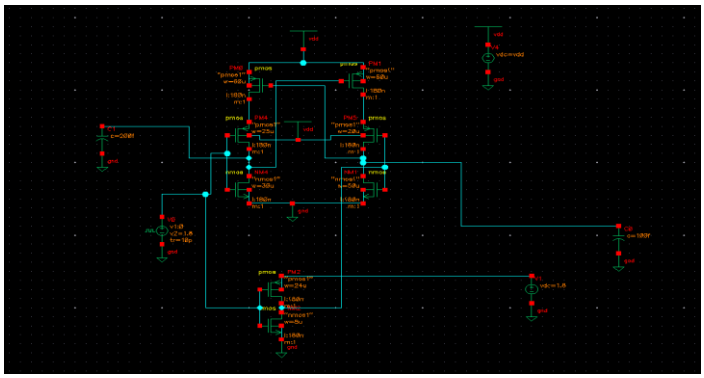

Fig.4. Schematic Diagram of Level Shifter

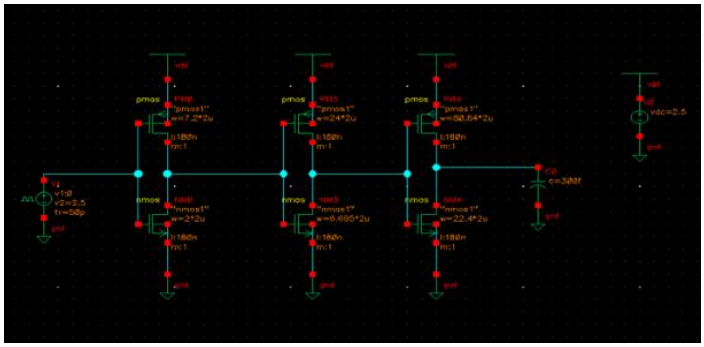

Fig.5. Schematic Diagram of Pre-Driver

It has the advantages of low static power consumption and small propagation delay due to the cross coupled latch structure [5]. Schematic diagram of level shifter is shown in Fig.4. It has two supply voltages, one for each side (V_{DD},V_{DDO}).V_{DD} is connected to same voltage supply for the source of input signal and V_{DDO} is connected to the I/O supply of the LVDS driver.

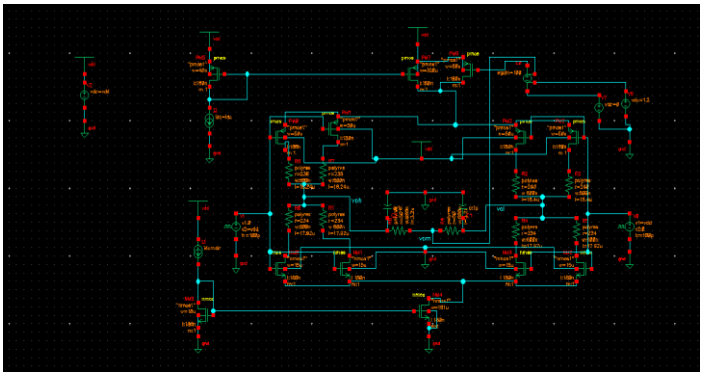

Fig.6. Schematic Diagram of Driver

3.2 SCHEMATIC OF PRE-DRIVER

The pre driver stage controls the voltage swing and common mode voltage at the input of the LVDS driver output stage. This makes the operation of LVDS at low supply voltages and at a higher operating frequency feasible. The pre-driver includes an inverter, high pass filter and a second inverter. The first inverter has an input terminal coupled to an input node of the pre driver and an output terminal coupled to a first inverter. The high pass filter is coupled between the first node and the second node. The second inverter has an input terminal coupled to the second node and an output terminal coupled to an output node of the pre-driver. The high pass filter is configured to improve a high frequency response of the pre-driver. The schematic diagram of pre-driver is shown in Fig.5.

3.3 SCHEMATIC OF DRIVER

Typical bridged-switched LVDS driver behaves as a current source with switched polarity. The bias current I_b is switched through the termination resistors according to the data input, and thus produces the correct differential output signal swing [6] [7]. It uses four transistor switches (M_1-M_4) in a bridged configuration. If switches M_1 and M_4 are on (V_{in} = HIGH), the polarity of the output current is positive together with the differential output voltage. On the contrary, if switches M_1 and M_4 are off (switches M_2 and M_3 are on), the polarity of the output current and voltage is reversed. With a nominal 100 Ω load at the receiver, both the common mode voltage and the differential swing at the output should fall within the LVDS standard [8]. The PVT (process-voltage-temperature) where V_{OD} and V_{CM} are the differential output voltage and the common mode voltage at the transmitter output respectively. The schematic diagram of driver is given in Fig.6.

3.4 SCHEMATIC OF CONTROL BLOCK

Control block receive the data and enable as input from the core and provide the data as output when enable is high and high impedance otherwise. The gate level implementation is shown in Fig.7.

3.5 SCHEMATIC OF LVDS TRANSMITTER

The integrated complete schematic diagram of transmitter block is given in Fig.8. The schematic of the transmitter block is designed as per specifications listed as per section 2.

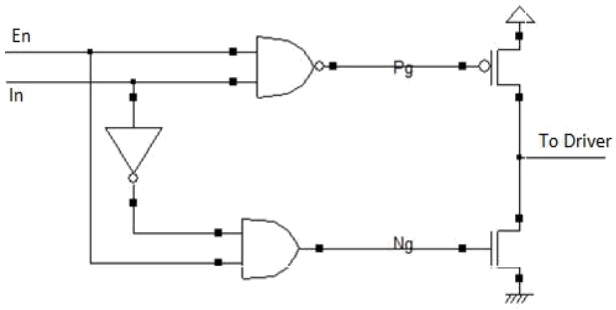

Fig.7. Gate Level Implementation of Control Block

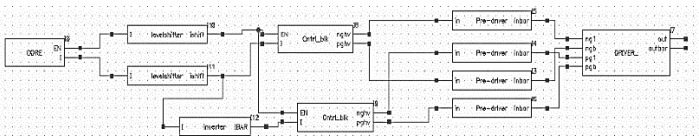

Fig.8. Schematic diagram of Complete Transmitter Block

4. RESULTS AND DISCUSSION

All the individual blocks of LVDS transmitter are designed as per the specifications listed in section 2 using Cadence virtuoso software. Transient analysis results are obtained using ADXL simulator and are shown in Fig.9- Fig.11.

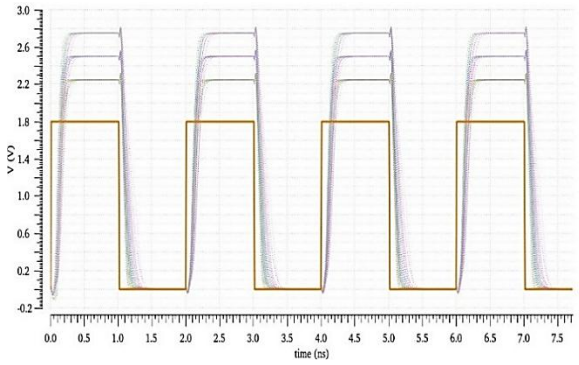

Fig.9. Transient Analysis of Level Shifter across PVT

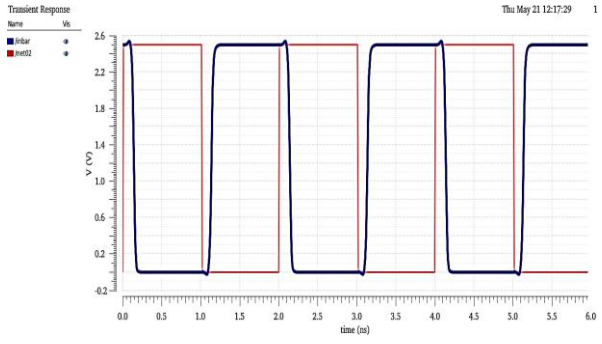

Fig.10 Transient Analysis of Pre-Driver

Level shifter is verified for shifting the core voltage of 0V - 1.8V i.e. the data, to an I/O voltage of to 0V -2.5V. Pre-driver stage is designed considering 3 stage inverter chain. Finally driver is designed to overcome the capacitive load of 2pF and 100Ω. DC and Transient analysis of the Driver circuit is performed in cadence virtuoso and is used to meet the specifications like V_{OH}<1.475V, V_{OL}>0.925V, VOS in the range ADEXL 1.125-

1.275 and V_{OD} in the range 250-400mV across PVT. PVT includes 5 process corner variations (FF, FS, SF, SS, NN), 3 voltage variations (2.5±10%, i.e. 2.25, 2.5, 2.75) and 3 temperature variations (-40^{o}C, 27^{o}C, 125^{o}C). The Table.2 show that results obtained are almost matching with the objectives specified in section 2.

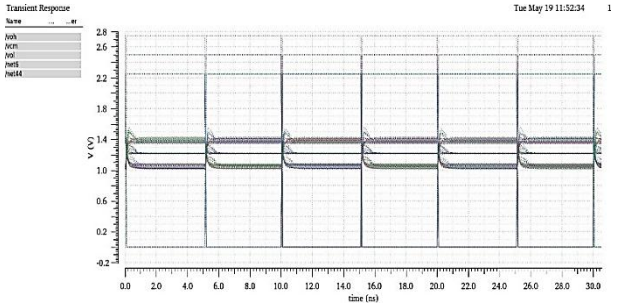

Fig.11. Transient Analysis of Driver

Table.2. Result Summary of LVDS Transmitter

Test	Calculation	Expression	Target	Maximum Value	Minimum Value
Transmitter Driver	V_{OH}	$V(V_{oh\_dc})$	<1.475	1.48	1.345
	V_{OL}	$V(Vol\_dc)$	>0.925	1.012	1.088
	V_{OS}	$V(V_{cm\_dc})$	1.125 to 1.275	1.215	1.221
	V_1	$V(V_{out\_dc})$		1.641	1.938
	V_{DD}	V_{OH}-V_{OL}	0.25 to 0.4	258.9m	413.7m
	Result	(V_1-V_{OH})/2*id		-153.3	-94.94

5. CONCLUSIONS

The LVDS basically protects the integrity of transmitted signal hence it more commonly used in chip to chip communications. LVDS is normally referred as generator in international standards. Propose work is carried out for the efficient design of level shifter, pre-driver, driver and control blocks using Cadence virtuoso software. LVDS Transmitter is designed by combining all the blocks to meet specifications as listed in section 2. Obtained results matches with the desired objectives of LVDS transmitter. The results of the proposed design is compared with [1] [9] found some deviations as there may be technology difference and different methodology.

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