DOI: 10.21917/ijme.2020.0169

DESIGN OF A DATA-INDEPENDENT LOW LEAKAGE POWER 10T SRAM CELL

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Abstract

6T SRAM cell has fast differential sensing and offers high density but read-write conflict exists which puts restrictions on the sizing of the devices. This degrades the stability in read mode with the declining supply voltage. To eliminate it, 8T SRAM cell incorporates decoupled read port to enhance the read stability. But it suffers from the data-dependent leakage which deteriorates the Read Bit Line swing. So, the data-independent and low leakage power is necessary to enhance the read sensing margin. To achieve the above, a new 10T SRAM cell is proposed which incorporates data independency and low leakage power. At the worst process corner FF, there is a reduction of 13.7%, 27.7% in leakage power of P10T SRAM cell compared to 10T1 SRAM and 10T2 SRAM cells at 0.9V while holding 0. The variation of supply voltage and the temperature has been studied on the leakage power. All the designs were implemented in 45nm technology and Post Layout simulation has been carried in Cadence Virtuoso.

Keywords:

Leakage Power, Data Independent Leakage, Process Corner, Stability

1. INTRODUCTION

SRAM contributes to the major portion of SoCs. The portables devices often require stable, low power SRAMs [1]. There is a growing trend to implement SoC based applications using FPGA due to its reconfigurability and prototyping [2]-[3]. There is a huge necessity for the on-chip memory for these FPGA implementations. SRAM is suitable for its faster response for cache memory [4]. Applications like Wireless Sensor Networks (WSN), biomedical devices often require low power. WSN offers a wide range of services like establishing the connection, transfer of information and gathering of data for conventional internet usage and industrial internet. WSN consists of sensor nodes. They communicate with the end-user using gateway which uses internet protocol to link sensor nodes and IP network. As multiple wireless sensor nodes form WSN in a particular remote area, longer battery life is often needed which reduces the burden on humans to replace the batteries every time. So lower power consumption is necessary for SoC using IoTs [5]. With the usage of IoT in the digital health system, Body Sensor Networks (BSN) are widely used. BSN consists of different sensors which monitor the physiological signals from a person [6]. The data, which was monitored, is sent to the nearest medical center for examination through the base station. The BSNs which process and store the data, often require memory to store it before transmitting to the medical center. SRAM plays a vital role in such applications due to its speed response. Portable devices, to enhance their performance, use embedded SRAM as a cache that uses FPGA to realize the digital systems [7]. SRAM design is used to store 1-bit of data. So, SRAM cell is used for FPGA devices. The LUT in FPGA stores the truth table. It is a table that maps to an output for the respective inputs. LUT is realized using SRAM cells. LUT forms the major building block of FPGA, which is realized using SRAM cells. So, decrease in leakage power of SRAM cell will ultimately reduce the overall leakage power of FPGA. With the scaling of technology nodes on the rise, the leakage power consumption is higher than that of the overall power consumption. Many of the SRAM cells for a greater amount of time operates in hold or standby mode [8]. So low leakage power is a significant parameter that needs to be reduced. Leakage currents contribute greater than 40% of active power in SoCs with enhanced performance [9]. So low leakage power is a significant parameter that needs to be reduced. Techniques like operating in subthreshold region, reduction in V_{DD} in idle mode, usage of multi-threshold devices and power gating [10]-[12] can reduce the active as well as the leakage power. However, reduction in V_{DD} leads to declined stability, prone to Process-Voltage-Temperature (PVT) variations.

2. LITERATURE SURVEY

6T SRAM cell is a compact form that has fast differential sensing but lags in read stability because of not having isolated read port. 8T SRAM cell [13] which incorporates a separate read port has higher read stability measured by RSNM than 6T SRAM cell. Though 6T and 8T SRAM cells have their advantages, their performance deteriorates when operated with a large number of cells connected to the bit lines due to the dependence of leakage based on the stored data. 9T SRAM cell [8] provides read stability but suffers from data dependency. An equalized bit line boosting scheme was employed to enhance the sense margin and to remove data dependency [14]. Equalized bit line leakage is achieved by providing the same amount of leakage to flow to GND from RBL for both Hold 0 and Hold 1 cases. RBL boosters were also employed to boost the current into RBL. The combined effect of bit line boosting and equalized bit line leakage increases the RBL sensing margin. 10T SRAM cell [15] uses additional devices to the 8T SRAM cell read port to enhance the read sensing margin. The additional NMOS device pulls down the gate of the NMOS device in the read port to GND irrespective of the data stored in the SRAM cell. The unselected cells during both read 0 and read 1 produce the same leakage current, thereby nullifying the effect which enhances the sense margin. In [16] different topologies of SRAM cells were proposed aiming to reduce the data-dependent leakage in the read port. $10T\text{-}P_1$ SRAM cell reduces the data dependency leakage but it becomes difficult to perform read operation for declining supply voltages. $10\ T\text{-}P_2$ SRAM cell offers data-independent read port leakage. In $10\ T\text{-}P_2$ SRAM cell, there is a leakage path from RBL to GND in both cases of hold 0 and hold 1. Due to an equal amount of leakage from RBL to GND, the data independent leakage is achieved.

The organization of the paper is as follows. Section 2 deals with the literature survey. Section 3 deals with the existing 10T SRAM cells and the proposed P10T SRAM cell. Section 4 deals with leakage power analysis. Section 5 comprises the results and discussion. Section 6 concludes the paper.

3. PROPOSED 10T SRAM CELL

The $10T_1$ SRAM [17] and $10T_2$ SRAM [18] cells are shown in Fig.1 and Fig.2. They eliminate the read disturbance in $6T$ SRAM cell by isolated read port. $10T_1$ SRAM cell employs different read port to reduce the leakage but data dependent leakage is not removed. In the read port, storage node Q_B drives NM_5 and PM_2 devices while NM_4 and NM_6 are driven by Read Word Line (RWL). $10T_2$ SRAM cell though employs data-independent leakage, it has increased leakage power. In the read port, Q_B drives NM_4 device while NM_5, NM_6 and PM_2 are driven by RWL.

The Proposed 10T (P10T) SRAM cell shown in Fig.3 also incorporates a separate read port as in 10T SRAM cell which eliminates the read disturbance. The NMOS devices NM_4 and NM_5 form the stacked devices driven by the storage node Q_B. PMOS device PM_2 is driven by the RWL which pulls up the intermediate node to V_{DD} during standby mode, thereby reducing the subthreshold leakage. The truth table for various modes of operation is presented in Table.1.

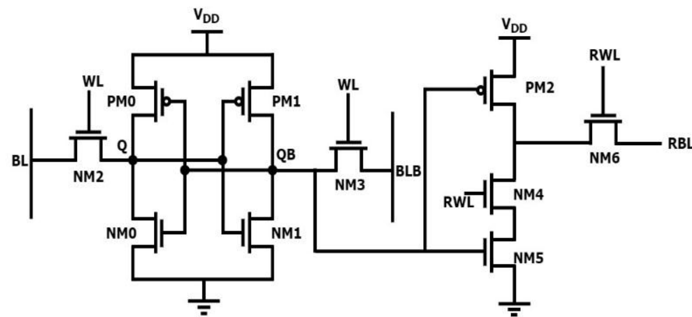

Fig.1. 10T1 SRAM Cell

In the hold mode of operation, Write Word line (WL) and Read Word Lines (RWL) are disabled enabling the back-to-back inverters to hold the data.

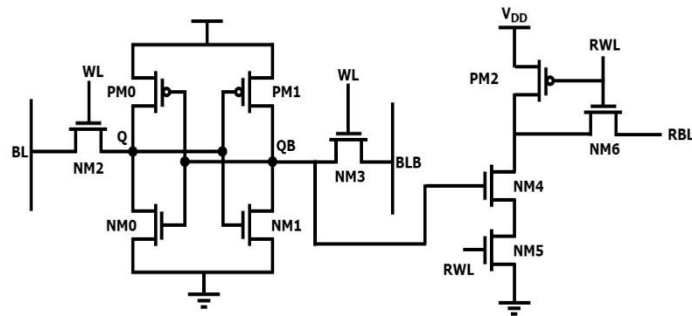

Fig.2. 10T2 SRAM Cell

In read mode, WL is disabled and RBL is Precharged to Logic 1. The RWLB is made Logic 0 and RWL is made Logic 1 which disables PM_2 device, enables NM_6 devices and the storage node QB controls NM_4 and NM_5 devices. When Q=0, Q_B=1, both NM_4 and NM_5 devices turn ON which provides RBL the discharging path to ground, indicating Read 0 operation. When Q=1, Q_B=0, both NM_4 and NM_5 devices turn OFF which doesn't provide RBL the discharging path to ground. So RBL stays at the already precharged value, indicating Read 1 operation.

In write operation, RWL is disabled while WL is enabled. When Q=0 and Q_B=1, BL is set to logic 1 and BLB is set to logic 0, enabling write 1 operation through the access devices NM_2 and NM_3 and vice versa for write 0 operation.

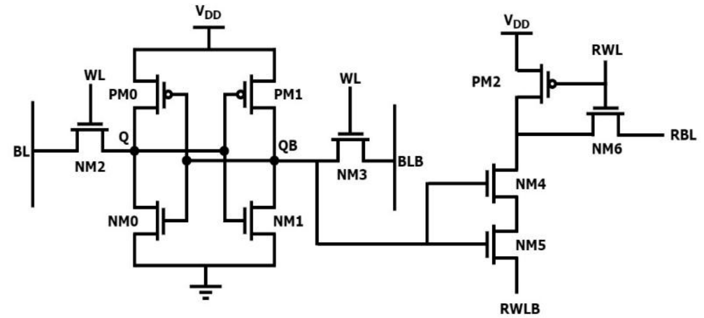

Fig.3. P10T SRAM Cell

Table.1. Control Signals of P10T SRAM cell

Control Signal	Hold	Read	Write 1/0
BL	1	1	1/0
BLB	1	1	0/1
WL	0	0	1
RBL	1	1	0
RWL	0	1	0
RWLB	1	0	1

4. LEAKAGE POWER ANALYSIS

The power consumed during the hold mode of operation is Leakage Power. It is the product of leakage current and V_{DD} [19]. Different leakage components for 10T1 SRAM cell, 10T2 SRAM cell and P10T SRAM cell were indicated in Fig.4 to Fig.6. Sub-threshold leakage, junction leakage and gate leakage mainly constitute the leakage components. Out of these 3 components, Sub-threshold leakage components play important role in deciding the magnitude of the leakage power.

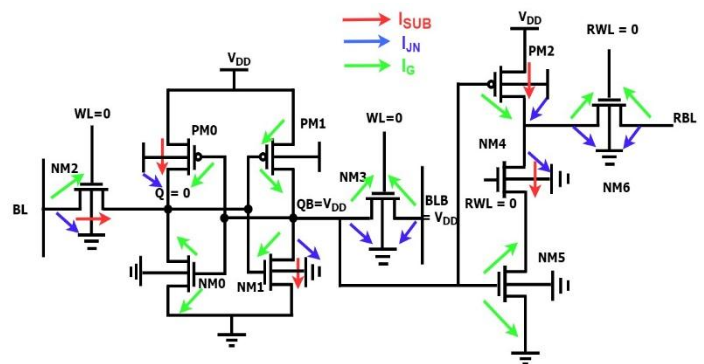

Fig.4. Leakage Components of 10T1 SRAM cell

The various leakage components for 10T1 SRAM cell is shown below.

$$I_{G,10T_1} = I_{DG,NM_2} + I_{GD,PM_0} + I_{GS,NM_0} + I_{GD,NM_0} + I_{DG,PM_1} + I_{SG,PM_1} + I_{DG,NM_1} + I_{SG,NM_3} + I_{DG,NM_3} + I_{GD,PM_2} + I_{SG,NM_5} + I_{DG,NM_5} + I_{GS,NM_6} + I_{GD,NM_6}$$

$$I_{JN,10T_1} = I_{JND,NM_2} + I_{JND,PM_0} + I_{JND,NM_1} + I_{JNS,NM_3} + I_{JND,NM_3} + I_{JND,PM_2} + I_{JND,NM_4} + I_{JND,NM_6} + I_{JNS,NM_6}$$

$$I_{SUB,10T_1} = I_{SUB,NM_2} + I_{SUB,PM_0} + I_{SUB,NM_1} + I_{SUB,NM_4} + I_{SUB,NM_5}$$

$$I_{LEAK,10T_1} = I_{SUB,10T_1} + I_{JN,10T_1} + I_{G,10T_1}$$

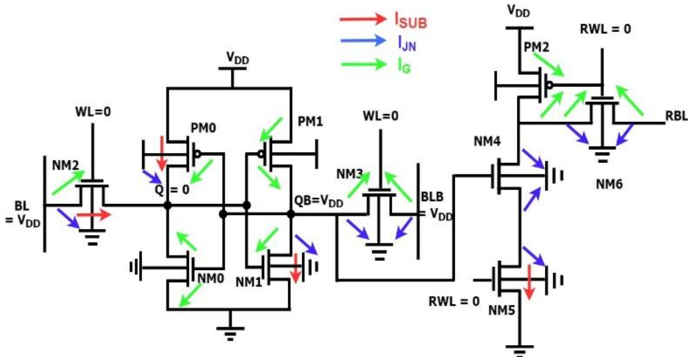

Fig.5. Leakage Components of 10T2 SRAM cell

The various leakage components for 10T2 SRAM cell is shown below.

$$I_{G,10T_2} = I_{DG,NM_2} + I_{GD,PM_0} + I_{GS,NM_0} + I_{GD,NM_0} + I_{DG,PM_1} + I_{SG,PM_1} + I_{DG,NM_1} + I_{SG,NM_3} + I_{DG,NM_3} + I_{DG,PM_2} + I_{SG,PM_2} + I_{GS,NM_6} + I_{GD,NM_6}$$

$$I_{JN,10T_2} = I_{JND,NM2} + I_{JND,PM_0} + I_{JND,NM_1} + I_{JNS,NM_3} + I_{JND,NM_3} + I_{JND,NM_5} + I_{JND,NM_4} + I_{JNS,NM_5} + I_{JND,NM_6} + I_{JNS,NM_6}$$

$$I_{SUB,10T_2} = I_{SUB,NM_2} + I_{SUB,PM_0} + I_{SUB,NM_1} + I_{SUB,NM_5}$$

$$I_{LEAK,10T_2} = I_{SUB,10T_2} + I_{JN,10T_2} + I_{G,10T_2}$$

The various leakage components for P10T SRAM cell is shown below.

$$I_{G,P10T} = I_{GS,NM_0} + I_{GD,NM_1} + I_{SG,NM_3} + I_{DG,NM_3} + I_{DG,NM_1} + I_{GD,PM_0} + I_{DG,PM_1} + I_{SG,PM_1} + I_{DG,NM_2} + I_{DG,PM_2} + I_{SG,PM_2} + I_{GS,NM_6} + I_{GD,NM_6}$$

$$I_{JN,P10T} = I_{JND,NM_2} + I_{JND,PM_0} + I_{JND,NM_1} + I_{JNS,NM_3} + I_{JND,NM_3} + I_{JND,NM_5} + I_{JND,NM_4} + I_{JNS,NM_5} + I_{JND,NM_5} + I_{JND,NM_5} + I_{JNS,NM_5}$$

$$I_{SUB,P10T} = I_{SUB,NM_2} + I_{SUB,PM_0} + I_{SUB,NM_1}$$

$$I_{LEAK,P10T} = I_{SUB,P10T} + I_{JN,P10T} + I_{G,P10T}$$

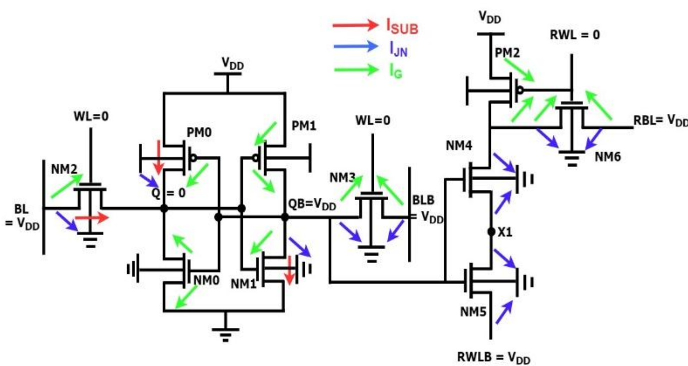

Fig.6. Leakage Components of P10T SRAM cell

The significant leakage component in P10T SRAM cell is the subthreshold leakage component which is produced when the devices are in OFF state. So, PM_0, NM_1 and NM_2 devices produce subthreshold leakage in OFF state as it $V_{DS}>0$. The Gate leakage components are produced between Gate terminal of the device and Source/Drain terminal of the device when the magnitude of the potential difference between both of them is V_{DD}. The Junction leakage is formed between the Source/Drain terminals of the device and the substrate when the magnitude of the potential difference between both of them is V_{DD}.

Subthreshold current can be modeled with the Eq.1 [20]

$$I_{sub}=I_0\exp[(V_{GS}-V_{TH}+\lambda_{BS}V_{BS}+\lambda_{DS}V_{DS})/\eta V_T][1-\exp(-V_{DS}/V_T)] \quad (1)$$

Drain Induced Barrier Lowering Coefficient is λ_{DS}, I_0 is Subthreshold Current for $V_{GS} = V_{TH}$, λ_{BS} is Body Bias Coefficient, η is Subthreshold Swing Factor and V_T is Thermal Voltage.

Subthreshold leakage forms a significant part of leakage power. Junction and gate leakage are comparatively negligible compared to the subthreshold leakage. There are 5 subthreshold leakage components in 10T1 SRAM, 4 in 10T2 SRAM cell and 3 in P10T SRAM cell. In P10T SRAM cell, as RWLB is set to high during hold mode and stacked transistors were used in the read port, there is a reduction in the number of components of subthreshold leakage components. Enabling RWLB reduces the V_{DS} which in turn reduces the leakage current as evident from Eq.(1).

4. RESULTS AND DISCUSSION

All the devices in the P10T SRAM design are considered as minimum sized i.e., L=45nm and W=120nm due to the isolated read port which avoids the read-write conflict. The remaining SRAM designs considered possess isolated read port. So, the minimum sized devices are also used for them. The layout of the P10T SRAM cell is shown in Fig.7. The post-layout simulation has been done in Cadence Virtuoso in 45nm technology.

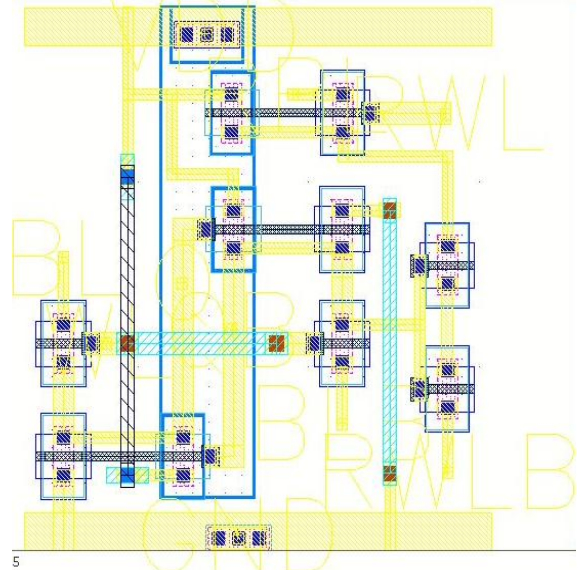

Fig.7. Layout of P10T SRAM cell

4.1 RBL LEAKAGE POWER

The leakage power of the read port in terms of the RBL Leakage ratio is shown in Fig.8. P10T SRAM cell has lower RBL leakage compared to $10T_1$ and $10T_2$ SRAM cells for different V_{DD} at worst corner FF. It is less by 2.34, 4.65 times than the $10T_1$ and $10T_2$ SRAM cells at 0.9V V_{DD}. The stacked NMOS devices and enabling of RWLB during hold mode reduces the RBL leakage power in P10T SRAM cell compared to the counterparts. The subthreshold leakage components of P10T SRAM cell are less

compared to $10T_1$ and $10T_2$ SRAM cells, thereby reducing the RBL leakage power. Enhancement of I_{ON}/I_{OFF} ratio leads to more SRAM cells per column. Reduction of I_{OFF} increases I_{ON}/I_{OFF} ratio which enables more cells per column in P10T SRAM cell.

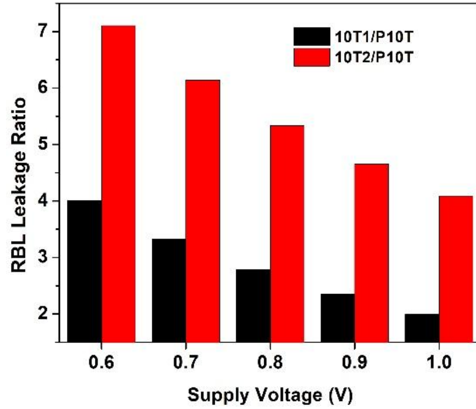

Fig.8. RBL Leakage Ratio for different V_{DD}

4.2 LEAKAGE POWER

Leakage power at different supply voltages and temperatures were shown in Fig.9 and Fig.10.

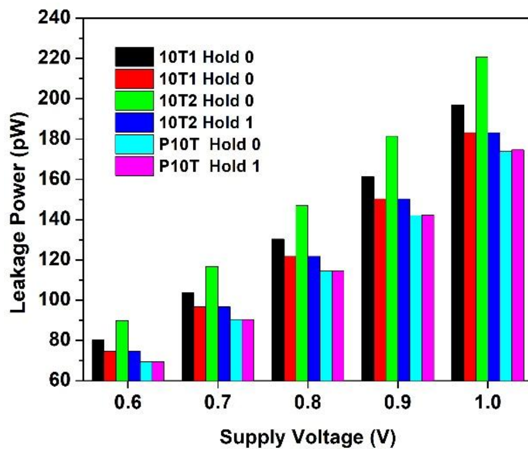

Fig.9. Leakage Power at different V_{DD} for worst process corner FF at 0.9V supply voltage

At the worst process corner FF, there is a reduction of 13.7%, 27.7% in leakage power of P10T SRAM cell compared to $10T_1$ SRAM and $10T_2$ SRAM cells at 0.9V while holding 0. There is a reduction of 5.77% % in leakage power of P10T SRAM cell compared to $10T_1$ SRAM and $10T_2$ SRAM cells at 0.9V while holding 1. Employment of stacked transistors in the read port and enabling RWLB leads to reduced leakage power.

Low leakage power in P10T SRAM cell enables the overall reduction in the leakage power when the P10T SRAM cell is used to realize an SRAM array. From Fig.10, as the temperature increases, there is an increase in leakage power. P10T SRAM cell has lower leakage than their counterparts for all temperatures.

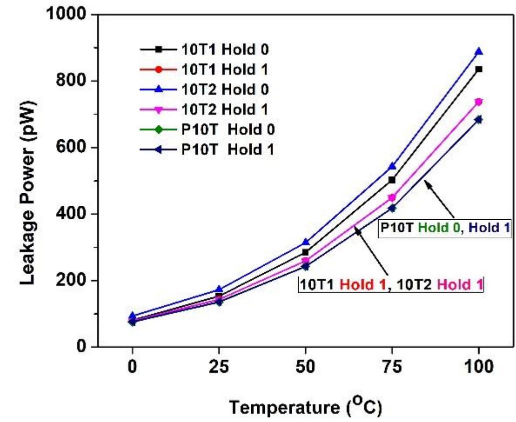

Fig.10. Leakage Power at different Temperatures for worst process corner FF at 0.9V supply voltage

5. CONCLUSION

With the aggressive scaling of technology nodes and supply voltages, low leakage power is necessary for most of the portable applications. The proposed 10T (P10T) SRAM Cell with the requirement of low leakage power was designed by incorporating the stacked devices in read port and enabling RWLB to high. So, it has reduced leakage power at the worst process corner FF for different V_{DD} and temperatures. It also has data-independent leakage which enhances the sensing window and RBL swing during the read operation. This enables to use the P10T SRAM cell in an SRAM array for low power applications. As SRAM cells stay idle for most of the time, the reduced leakage power of P10T SRAM cell will have a significant reduction on the overall leakage power of SRAM array. The data-independent leakage in read port in P10T SRAM cell allows working in longer columns of an SRAM array. The reduced leakage power in P10T SRAM cell can be used to realize the LUTs in FPGA. As the LUT leakage power gets decreased which in turn reduces the overall leakage power of FPGA.

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