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DESIGN OF CARRY DEPENDENT SUM ADDER USING REVERSIBLE LOGIC

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Abstract

Low power is a paramount concern in the design of 'digital signal processor' (DSP) for future multimedia applications. The quest to achieve low power has made the researchers to look into different techniques. In more recent years, the reversible logic is emerged as an alternate and promising low power technique for next generation technologies. It finds vast applications in nanotechnology, low power CMOS circuit design, approximate computing, optical computing, and quantum computing etc. The full adder being critical element of DSP plays an important role in the contribution of overall power of the system under consideration. This paper proposes a design of novel reversible full adder based on 'carry-dependent sum full adder' (CSFA) architecture using the standard reversible logic gates. The proposed reversible FA herein referred to as 'Reversible CSFA' (RCSFA). Two variants of RCSFA namely RCSFA-1 and RCSFA-2 have been proposed and discussed. To assess the merits of proposed RCSFAs, they are compared against the state-of-the-art reversible full adders (RFAs) in terms of quantum gate metrics (QGMs) such as number of gates, 'quantum cost' (QC), constant inputs, and garbage outputs etc. From the comparison results the proposed RCSFAs are found to be an alternative choice for designers in terms of QC, constant inputs and garbage outputs.

Keywords:

Reversible Logic, Low Power, Full Adder, Quantum Gates, Quantum Cost

1. INTRODUCTION

Energy dissipation is inevitable in conventional irreversible logic gates [1]. The energy dissipation occurs mainly due to loss of information. The amount of heat generated per bit of information lost is kTlog2 Joules [2], where k is Boltzmann's constant and T is the absolute temperature at which operation is performed. The problem of information loss can be mitigated by using reversible logic, where the inputs and outputs have one-to-one mapping. And also every input vector can be uniquely recovered from the output vectors and vice-versa [3].

The next generation battery-operated "Internet-of-Things" (IoT) devices and computationally intensive multimedia processors demand low power and high-speed 'Digital Signal Processing' (DSP) architectures. The critical block in any DSP architecture is "Multiply-accumulate" (MAC) unit. The MAC is an important and most expensive operation in many signal processing applications. Apart from DSP, the MAC operations are extensively used in many other applications including audio, video, speech, neural network (NN), tensor processing units (TPUs), filtering, object detection, convolution [3-7] etc. The MAC has two important blocks: a multiplier and an accumulator [8]. The most primitive cell in these blocks is full adder (FA). The FA being a leaf or primitive cell of MAC unit directly influences the overall performance of the DSP architecture. Thus, FA has become the center of attraction for most of the researchers to design energy efficient DSP systems. The various low power techniques have been discussed in the current literature. The power reduction can be achieved at different levels of design abstraction:

- Algorithmic level
- Architecture level
- Gate level
- Transistor level

At the algorithmic level, the low power is achieved by significant driven computation (SDC). In SDC, the computations are classified as significant and non-significant. The significant computations are performed using exact circuits and non-significant computations are performed using approximate computations [9]. At architectural level, the power efficiency can be achieved using the voltage over scaling (VOS) [10]. The VOS is used to achieve low power by scaling down the supply voltage below its lower bound. At gate level, the power reduction using voltage scaling was discussed in [11-12]. The voltage scaling allows to use different supply voltages for different logic gates in the same circuit. The other works discussed extensively on reduction of power at transistor circuit level [13-14]. At circuit level power reduction is achieved by using hybrid logic styles, where in more than one type of logic is used to achieve the low power. For example the static CMOS logic is used along with pass transistor logic style. With the advent of reversible logic, the reversible logic gates have gained more popularity in the design of low power circuits. Thus reversibility will become an indispensable paradigm in future low power circuit design.

Many FA realizations using reversible logic gates have been proposed and discussed in the state-of-the-art literature. The design of a low QC reversible FA was discussed in the [15]. In this the authors used two Peres gates (equal to QC of 2×4=8) to implement the FA. The FA design based on Fredkin gate was proposed and presented in [16], its QC is 5×5=25. In [17], the Fredkin gate based FA circuit that avoids fan-out was proposed, which requires only 4 Fredkin gates equivalent to QC of 4×5=20. The works in [18]-[21] have proposed reversible FAs using either conventional or new reversible logic gates.

Rest of this paper is organized as follows. The next section presents the reversible logic gates and their QGMs. Section 3 reviews the existing reversible FA architectures. Section 4 presents the design of proposed reversible FA. The section 5 presents the design results and discussion. Finally, section 6 concludes the paper.

2. REVERSIBLE LOGIC GATES AND THEIR QUANTUM COST (QC)

This section presents reversible logic gates and their important features. A logic gate is said to be reversible if it satisfies the following conditions:

- Number of inputs must be equal to number of outputs

- Fan-out and feedback paths are not permissible.
- A unique mapping must exist between the input and output patterns, an example of mapping is illustrated in Fig.1.

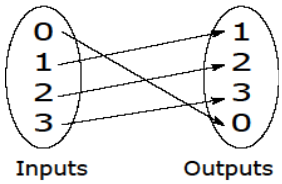
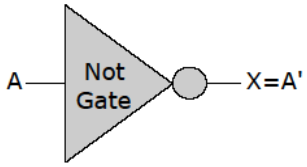


Fig.1. Unique mapping between input and output patterns

The conventional reversible logic gates that are used to design reversible circuits are:

2.1 NOT GATE

The NOT gate is a 1×1 primitive reversible gate shown in Fig.2. It has one input (*A*) and one output (*X*). The QC of NOT gate is zero (0).



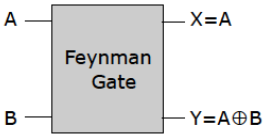
(a)

(b)

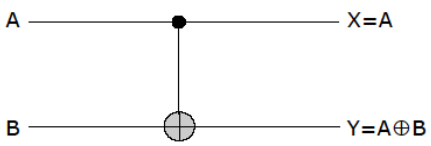
Fig.2: Not gate: (a) Symbol (b) Quantum equivalent

2.2 FEYNMAN GATE/CONTROLLED NOT GATE:

The Fig.3 is a 2×2 Feynman reversible logic gate. It has two inputs (*A*, *B*) and two outputs (*X*, *Y*). The relation between inputs and outputs is given by (*A*, *B*) →(*X*=*A*, *Y*=*A*⊕*B*). Since it passes one of its input to output it is also known as one through gate. Among the inputs: '*A*' is referred to as control signal and '*B*' is the target signal. If *A*=0 irrespective of *B* value, the outputs are equal to *X*=0, and *Y*=*B*. If *A*=1, the corresponding outputs are *X*=1 and *Y*=*B*′, where *B*′ represents the complement of *B*. The *QC* of this gate is '1' [22].



(a)

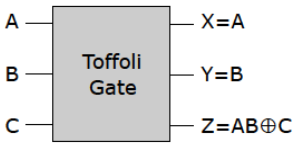


(b)

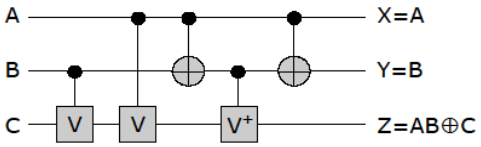
Fig.3: Feynman gate: (a) Symbol (b) Quantum equivalent

2.3 TOFFOLI GATE/ CONTROLLED-CONTROLLED NOT GATE

The symbol and quantum equivalent representation of a 3×3 Toffoli gate is shown in Fig.4 [23]. It is also known as two through gate, this is because two of its outputs are same as two inputs. The unique relation between inputs and outputs is expressed as (*A*, *B*, *C*)→(*X*=*A*, *Y*=*B*, *Z*=*AB*⊕*C*). It can be generalized to *n* inputs × *n* outputs gate. Among *n*-inputs, *n*-1 are control inputs and one is target input. For a 3×3 gate, there are 3-1=2 control inputs and 1 target input. The QC of this gate is 5. In the Fig.4, the symbol *V* is a square-root-of-NOT gate and represents the unitary matrix *V*. The V^+ represents the Hermitian of *V*.



(a)

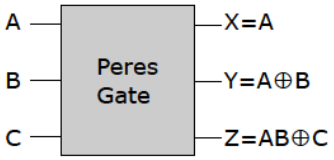


(b)

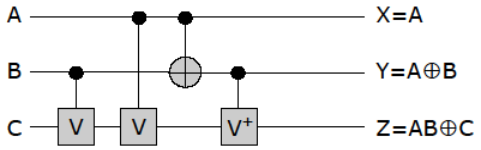
Fig.4. Toffoli gate: (a) Symbol (b) Quantum equivalent

2.4 PERES GATE

A Peres gate [24] shown in Fig.5 is a 3×3 reversible logic gate, which has QC of 4.



(a)



(b)

Fig.5. Peres gate: (a) Symbol (b) Quantum representation

It is a one through gate and has 3 inputs and 3 outputs. The inputs and outputs are related as (*A*, *B*, *C*) → (*X*=*A*, *Y*=*A*⊕*B*, *Z*=*AB*⊕*C*).

2.5 FREDKIN GATE

A Fredkin gate shown in Fig.6 is a 3×3 reversible gate and is also called one through gate [17, 25]. The relation between the inputs and outputs is given by (*A*, *B*, *C*) → (*X*=*A*, *Y*=*A*′*B*+*AC*, *Z*=*A*′*C*+*AB*). It is a conservative gate because the Hamming weight of inputs equals the Hamming weight of outputs [15]. In the Fig.6(b), the dotted rectangular box shown in quantum

implementation is equivalent to a 2×2 Feynman gate. Thus, the quantum cost of each rectangular box is '1'. Further it has one quantum gate V and two Controlled NOT gates. Thus the total quantum cost of this gate is '5', which is same as that of Toffoli gate.

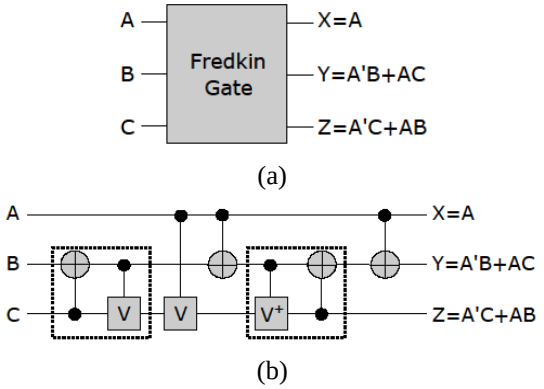
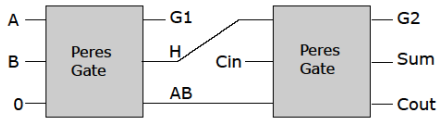


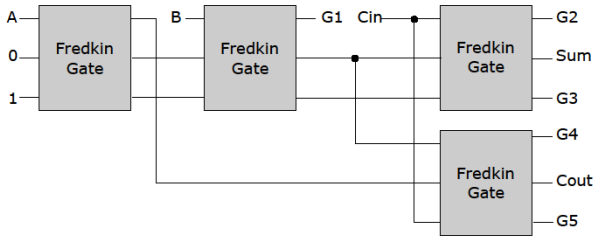
Fig.6. Fredkin gate: (a) Symbol (b) Quantum representation

3. EXISTING REVERSIBLE FA

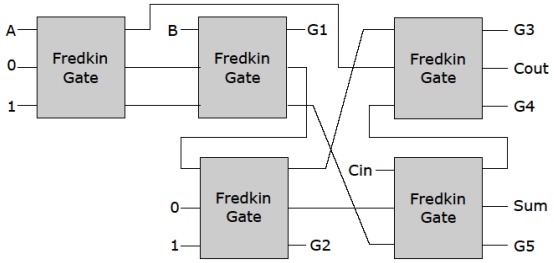
In this section, the state-of-the-art 1-bit 'reversible full adder' (RFA) architectures are presented along with their respective salient features. The block diagrams of various RFAs that were reported in the current literature have been shown in the Fig.7.



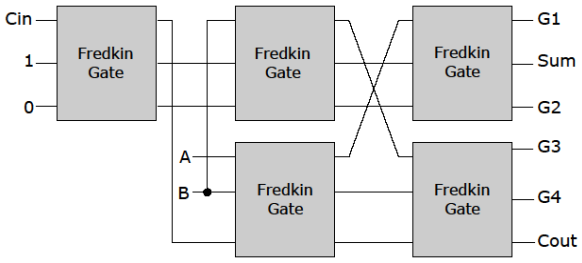
(a) Peres gate based RFA [15]



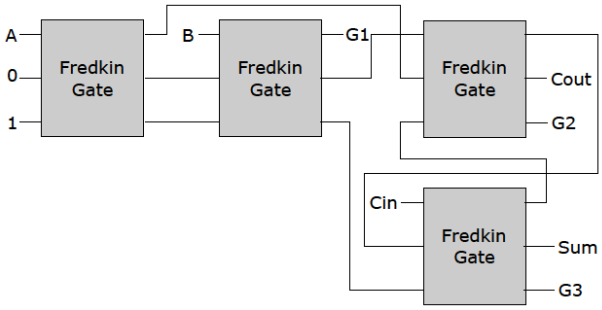
(b) Fredkin gate RFA with fan-out, for carry-skip adder application [17]



(c) Fredkin gate RFA avoiding fan-out, for carry-skip adder application [17]



(d) Conventional Fredkin gate RFA with fan-out [16]



(e) Conventional Fredkin gate RFA avoiding fan-out [17]

Fig.7. State-of-the-art RFA architectures

The Fig.7(a) is the low quantum cost RFA, it is designed by using two Peres gates. This RFA has 1-constant input and 2-garbage outputs. The total implementation *QC* is 2×4=8. The RFAs shown in Fig.7(b) and Fig.7(c) were proposed for carry-skip adder design applications. The RFA shown in Fig.7(b) has fan-out on the input signal, C_{in}. It has 2-constant inputs, 5-garbage outputs with a total *QC*=20. The RFA shown in Fig.7(c) is used to avoid fan-out on the input signal, C_{in}. It has 4-constant inputs, 5-garbage outputs with a total *QC*=25. The conventional Fredkin gate based RFAs, with fan-out and avoiding fan-out on input C_{in}, are shown in Fig.7(d) and Fig.7(e) respectively. The RFA shown in Fig.7(d) has 2-constant inputs, 4-garbage outputs, and QC=25. The RFA shown in Fig.7(e) has 2-constant inputs, 3-garbage outputs, and *QC*=20.

From the Fig.7, it is found that all the reported RFAs (except the RFA shown in Fig.7(a)) conceived more number of constant inputs, more garbage outputs, and also results in high *QC*. Considering these demerits of an existing RFAs, in this research paper a novel RFA is presented based on CSFA architecture [14], this proposed RCSFA conceives smaller or '0' constant inputs, less garbage outputs, and also low *QC*.

4. PROPOSED REVERSIBLE FULL ADDER

The proposed reversible FA is derived based on the carry-dependent Sum full adder (CSFA) architecture [14]. The block diagram and truth table of FA are shown in Fig.8 and Table.1 respectively. The logical expression for the outputs Sum and C_{out} in terms of inputs *A*, *B* and C_{in} are derived as follows. Let $H = A \oplus B$, where the symbol $\oplus$ represents the Exclusive-OR operation (XOR) and H' represents the inversion of *H*. From the truth table:

$$\text{If } H=0, \text{ then } C_{out} = A \text{ else } C_{out} = C_{in},$$

$$\text{If } H=0, \text{ then } Sum = C_{in} \text{ else } C'_{out},$$

where C'_{out} is the complement of C_{out}.

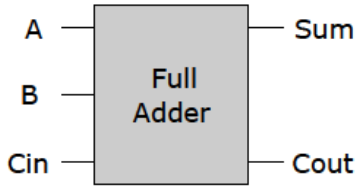


Fig.8. FA block diagram

Table.1. Truth Table of Full Adder (FA)

A	B	C_{in}	*Sum*	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Thus, the expression of Sum and Cout of exact FA are formulated as:

$$C_{out} = H'.A + H.C_{in} \quad (1)$$

$$Sum = H'.C_{in} + H.C'_{out} \quad (2)$$

From the Eq.(1) and Eq.(2), it is found that both Sum and C_{out} can be computed using multiplexor (MUX) operation. Considering the Eq.(1), the C_{out} can be derived by using H as a select signal and A, C_{in} as inputs of MUX. Similarly the '*Sum*' can be computed by using H again as a select signal and C_{in} and C'_{out} as inputs. Further, it is noticed that the Sum depends on carry output (C_{out}) hence the proposed FA herein referred to as Carry-dependent Sum FA (CSFA).

Therefore, to design the proposed CSFA using reversible logic, herein referred to as Reversible CSFA (RCSFA), we need the reversible gates that generate two primitive operations namely Exclusive-OR (XOR) and Multiplexor (MUX). From the Section 2 it is found that the Feynman and Fredkin reversible gates are an ideal choice to implement the XOR and MUX operations respectively. The block diagram of the proposed RCSFA is shown in Fig.9. The Fig.9(a) is the proposed RCSFA with fan-out on input C_{in} (RCSFA-1) and Fig.9(b) is the proposed RCSFA avoiding fan-out (RCSFA-2). In this figure, the Feynman gate is used to generate XOR operation. The Fredkin gate is used to implement 2:1 Multiplexing operation. Thus to implement RCSFA-1, one Feynman gate and two Fredkin gates are required. The QC of Feynman gate and Fredkin gates is 1 and 5 respectively. Hence the total cost of proposed RCSFA-1 is 11 (=1×1+2×5) and RCSFA-2 is 12. In the Fig.7 and Fig.9, the signals G_1, G_2, G_3, G_4, and G_5 represents the garbage outputs.

5. DESIGN RESULTS AND DISCUSSION

To verify the functionality of the proposed RCSFA-1 and RCSFA-2, the designs are described using Verilog hardware-description-language (HDL), based on the gate level description. Further, a Verilog HDL test bench code was used to test the functionality of the proposed RCSFAs. To verify the functionality, simulations have been performed using the Cadence's NC simulator. From the simulated results it is found that the proposed RCSFAs successfully function as per the truth table shown in Table.1. The snapshot of the simulated waveform is illustrated in the Fig.10.

To assess the merits of the proposed RCSFAs, they are compared against the state-of-the-art reversible FAs (RFAs) in terms of QGMs such as number of gates, garbage outputs, constant inputs, and QC etc. The comparison of all the RFAs under consideration is listed in Table.2. From this table the following points can be noticed:

- Considering the number of gates column, it is observed that the Peres gate based FA (Fig.7(a)) has a low QC, this can be attributed to the architecture of RFA which conceived less number of reversible gates.
- Considering the number of constant inputs column, the proposed RCSFA-1 has 0 constant inputs, which is the lowest as compared to any other RFA under consideration.
- From *QC* column, it is found that the proposed RCSFAs are having *QC* of '11' and '12', which are the 3rd and 4th lowest value as compared to other RFAs under consideration.

Thus, the proposed RCSFAs are found to be an alternative choice for designers in terms of QC, constant inputs and garbage outputs and can be a suitable candidates for low power quantum computing applications.

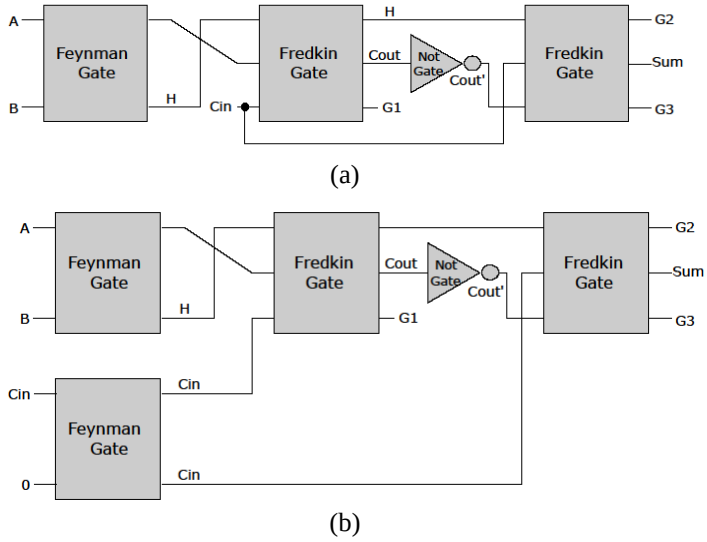


Fig.9. Proposed RFAs based on CSFA architecture (a) RCSFA-1 (b) RCSFA-2

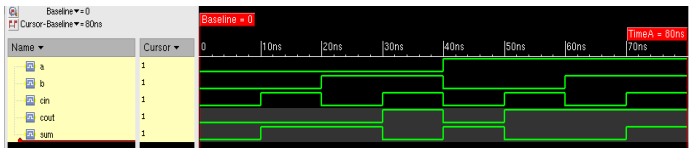


Fig.10. Simulated waveform of proposed RCSFAs

Table.2. Comparison of proposed RCSFAs and state-of-the-art reversible full adders in terms of quantum gate metrics

Reversible FA composition	No. of Gates	No. of garbage outputs	No. of constant inputs	Quantum Cost

Peres (Fig.7(a)) [15]	2	2	1	8
Fredkin (Fig.7(b)) [16]	4	5	2	20
Fredkin (Fig.7(c)) [17]	5	5	4	25
Fredkin (Fig.7(d)) [17]	5	4	2	25
Fredkin (Fig.7(e)) [17]	4	3	2	20
Feynman, Toffoli and New Gate [21]	3	2	1	-
Toffoli, Khan, and Feynman [15]	3	2	1	-
Toffoli and Feynman [15]	4	2	1	10
Khan and Feynman [15]	3	3	2	-
Proposed RCSFA-1 (Fig.9(a))	3	3	0	11
Proposed RCSFA-2 (Fig.9(b))	4	3	1	12

6. CONCLUSION

In this paper, two novel RCSFAs have been proposed and discussed. The proposed reversible FAs are derived based on CSFA architecture. To assess the merits of proposed RCSFAs, they are compared against the state-of-the-art RFAs in terms of QGMs. Based on the comparison results, the proposed RCSFAs are found to be having low QC, less constant inputs, and less garbage outputs. Therefore, the proposed RCSFAs can find a wide scope in the design of reversible based arithmetic systems and hence they can serve as an alternate choice for the researchers and designers, where the low QC, low garbage outputs, and low constant inputs are a paramount concern.

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