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PHASE LOCKED LOOP USING SUB HARMONIC INJECTION TECHNIQUE WITH AUTO ADJUSTED DELAY LOCKED LOOP

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Abstract

For high speed communication applications; jitter, phase noise and power consumption are most critical parameters required to be considered for PLL designs. A sub harmonically injection locking concept can be used in PLL to reduce jitter and phase noise. Such design is very effective for high frequency applications. This article presents design for low jitter, phase noise, power dissipation for 7.5 GHz Phase locked loop using sub harmonic injection technique with auto adjusted Delay locked loop in 180-nm CMOS technology. The measured phase noise at 1 MHz reference offset frequency is 122.31 dBc/Hz with rms jitter is 127 fs. The overall power dissipation is 13.99 mW for proposed design.

Keywords:

CMOS, PLL, Loop Filter, VCO, PFD, Sub Harmonic Injection

1. INTRODUCTION

In today's era jitter, phase noise, power dissipation in phase locked loop is very important specifications for high frequency applications. The voltage controlled oscillator, phase frequency detector and input reference signal are main sources of phase noise. It is known that phase noise is removed by high pass filter at input, while output of PFD is a low pass response. For a design of low jitter with less phase noise, selection of loop bandwidth is very important. If frequency of VCO is increases, phase noise becomes worst for PLL [4] [5].

After making a thorough study of the literature, it is found that, many researchers have been done for developing a PLL which could withstand the process and temperature compensation. Some researchers have concentrated on the VCO design for gain compensation and increasing the stability of the PLL. Few works have been reported for the development of gain boosting structure and current matching characteristics.

Some researchers have concentrated on the development of Low noise based VCO, to have higher PLL locking range in their design. Some researchers have concentrated on the development of Phase Frequency Detector, to achieve minimum dead zone.

Some researchers have concentrated to develop high frequency delay locked loop for similar purpose. Some Researchers have concentrated to achieve stable output with least value of noises and power dissipation with good figure of merit with compromising frequency output. Some researchers have developed high frequency PLLs with compromising key characteristics.

A sub harmonically injection locking concept can be used in PLL to reduce jitter and phase noise. Such design is very effective for high frequency applications. Main issues for such design is locking range and phase matching between injected signal and oscillator [1] [2]. In this article, author has achieved 7.5GHz PLL using sub harmonic injection technique for low jitter; low phase noise with auto adjusted DLL in 180 nm CMOS technology.

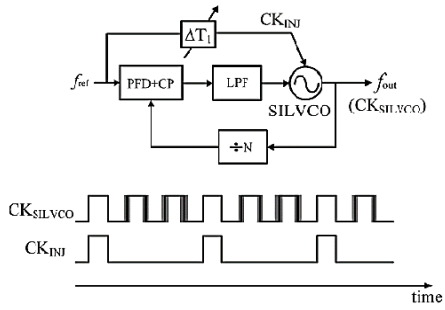

Fig.1. Conventional Phase Locked Loop [1] [2]

The Fig.1 represents the block diagram of phase locked loop. The output waveform with jitter is shown in Fig.3 for most of PLL. In most PLLs, performance degrades due to jitter and noises. SIL PLL and its resulting waveforms are shown in Fig.2. Due to the injection phenomenon, jitter and noises of SIL PLL can be reduced [1] [2].

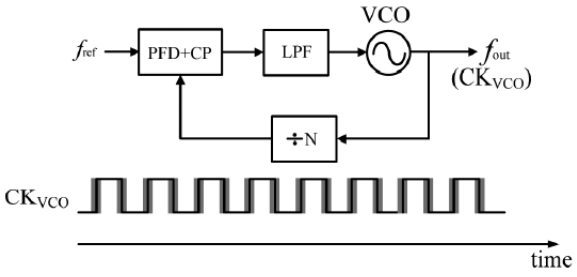

Fig.2. SIL PLL [1] [2] [3]

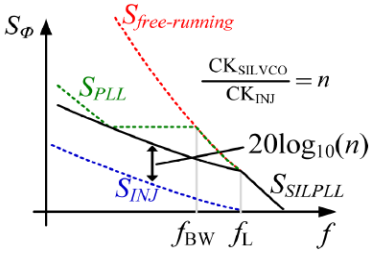

Fig.3. Output Phase Noise for SIL PLL [1] [2]

The SILPLL architecture is shown in Fig.4. Third order phase locked loop with a sub harmonic injected locked VCO and first order Delay locked loop for auto adjusted injection are used in designed architecture. Resulting waveforms of given SILPLL is shown in Fig.5 [1] [2].

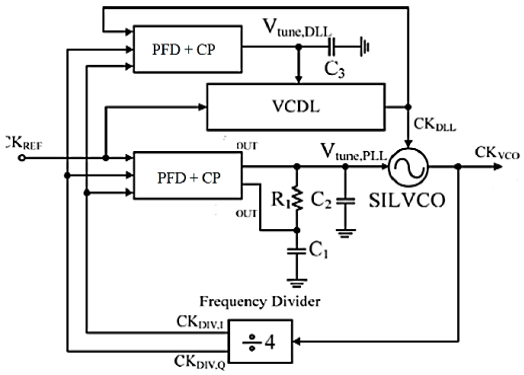

Fig.4. 7.5 GHz PLL using sub harmonic injection technique with Auto Adjusted DLL

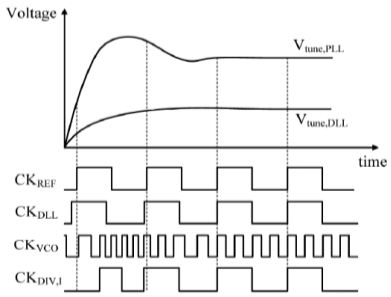

Fig.5. Waveform for SIL PLL [1] [2]

Once PLL runs, output phase and frequency is locked with input reference frequency. Injected phase using sub harmonic injection locked VCO is adjusts automatically using first order DLL. The phase and frequency injected VCO will again relocked to reference signal as the multiple frequencies [1] [2].

2. PHASE FREQUENCY DETECTOR

The two DFF and clock inverter with TSPC logic is used to design phase frequency detector. Such design of flip flop has less number of transistors. Only one transistor is being clocked by short pulse train to DFF [6] [7]. Reset path of phase frequency is modified by direct cross connections of input reference and clock signal of both D flip flop. Such modification reduce dead zone and hence jitter is also reduce [6] [7].

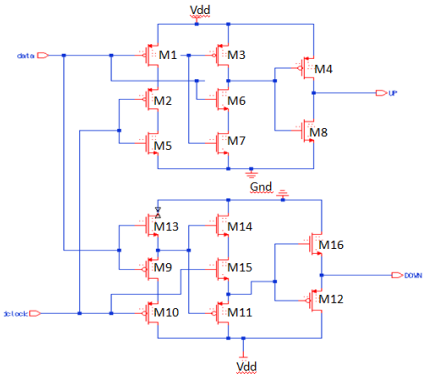

Fig.6. Modified PFD

2.1 CHARGE PUMP

The resulting outputs of phase frequency detectors are directly given to charge pump followed by loop filter.

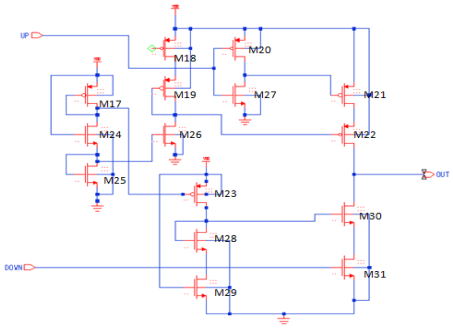

Fig.7. Charge Pump

2.2 VOLTAGE CONTROL DELAY LINE

The voltage controlled delay line with open loop configuration is used for delay locked loop circuit. It consist serially connected delay stages. It does not oscillate and provide proper delay to required design [11] [15].

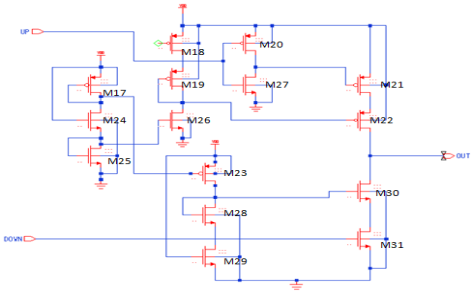

Fig.8. Ring Based VCDL

2.3 SIL VCO

The SIL VCO design is shown in Fig.9. Here, M_3-M_4 receives pulses at gate of M_4, and injects current into LC tank. Dimensions of M_1-M_2 and M_3-M_4 as well as bias circuit Ib_1, M_5, and R_b define overall strength of injection. [1] [2].

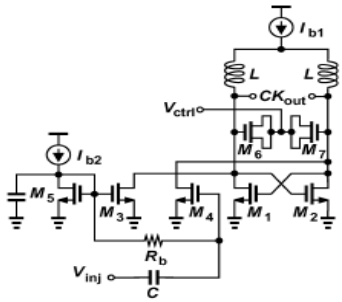

Fig.9. SIL VCO

2.4 DIVIDE BY N NETWORK

The voltage divider network provides feedback to phase frequency detector circuit. Same feedback is again compare with input reference signal.

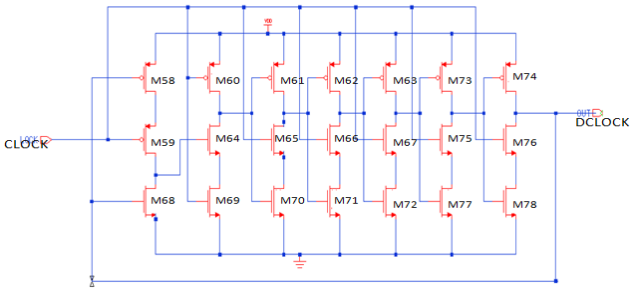

Fig.10. Voltage Divider

3. OPEN AND CLOSED LOOP PLL RESULTS

The resultant waveform of open loop PLL is shown below. The maximum output frequency is 1.8GHz at open loop stable condition. All the required parameters are measured and the waveforms are shown below.

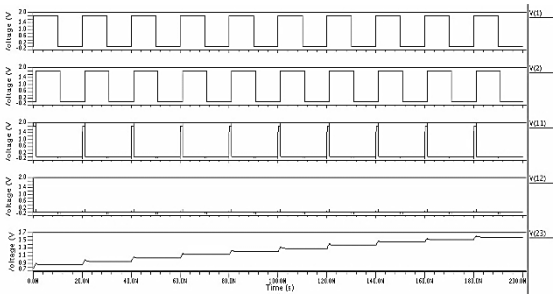

Fig.11. Combine results of PFD, CP and LPF

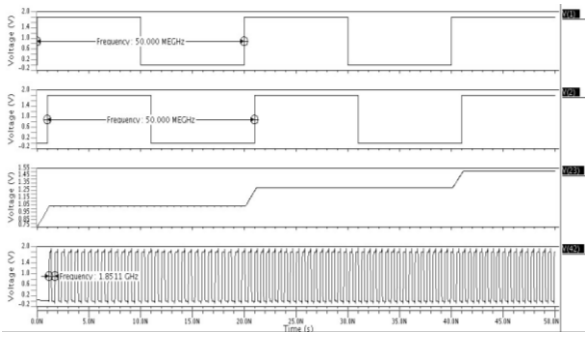

Fig.12. Results of Digital PLL

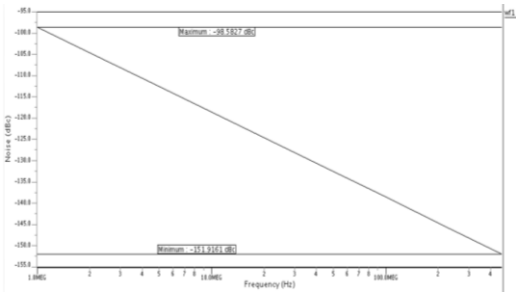

Fig.13. Phase Noise Plot vs. offset Frequency of PLL at 1MHz

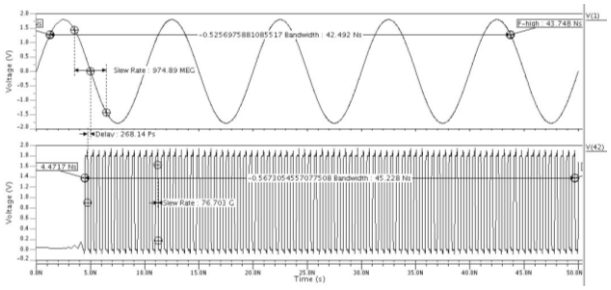

Fig.14. Slew Rate Measurement

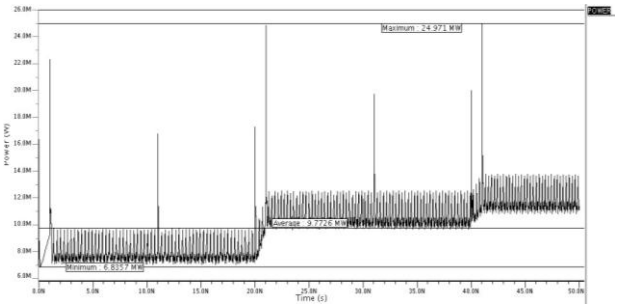

Fig.15. Average Power Measurement

The Fig.11 illustrate the noise measurement with different values of output frequencies. The Fig.12 represents the locked conditions with Up and Down responses of PFD. The Fig.13-Fig.15 shows the measured value of delay including and excluding charge pump circuit.

4. OPEN AND CLOSED LOOP DLL RESULTS

The resultant waveform of open loop and closed loop DLL are shown below. All the parameters are also measured and the waveforms are shown below. The Fig.16 shows the measured value of delay with Charge Pump. In addition, Fig.17 illustrates the delay measurement with different values of output frequencies, which represents the locked conditions with Up and Down responses of PFD.

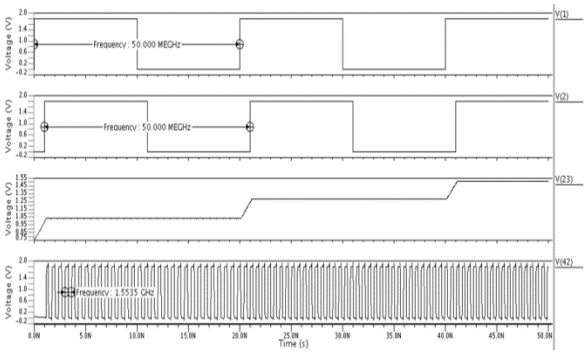

Fig.16. Results of DLL

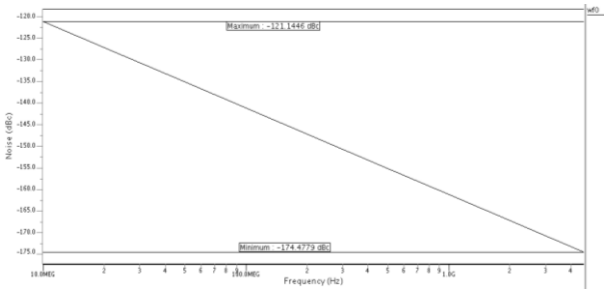

Fig.17. Control Voltage vs. Oscillator Frequency

The Fig.16 – Fig.17 illustrate the open loop output results of DLL including PFD and Charge pump with different values of output frequencies. That also represents the locked conditions with Up and Down responses of PFD. It shows the measured value of phase noise verses offset Frequency of DLL at 1MHz.

5. CLOSED LOOP SIL PLL RESULTS

The Table.1 illustrate the measurement of different parameters and key specifications of proposed Digital Phase Locked Loop. Proposed DPLL provide very wide tunning range. It can vary from approximately 7.25 GHz to 8.24 GHz after post layout results. It is very wide as compared to existing architectures.

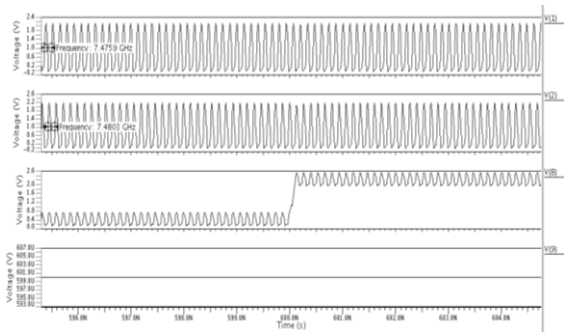

Fig.18. SILPLL Output Frequency at 1.8 V

Table.1. Performance Comparisons of Proposed SILPLL

Parameter	SILPLL Specifications	Ring Based Sub sampling PLL [4]
Technology	180nm	180nm
Power Supply	1.8V	1.8V
Reference Frequency	250MHz	-
Centre Frequency	1GHz	-
Transistor Count	133	-
Tuning Range (GHz)	1 - 7.5	2.4
Lock Range	25 – 60MHz	-
Power Consumption	13.99mW	12.6mW
RMS AC/ TRAN Noise	30.27nV/ 169.22µV	-
Settling Time	31.12nS	-
Phase Noise	-122.31dBc/Hz	-129dBc/Hz
RMS Jitter	127fs	145fs
Figure of Merit	-268.29dB	-246dB

6. CONCLUSION

To verify the proposed design, the author used Tanner EDA and Mentor Graphics tools to carry out simulations in 180 nm CMOS technology. The proposed digital PLL have very stable high frequency signal output with wide tuning range. It is competent to generate high speed clock signal with minimum low phase noise and optimum power consumption. It is most suitable for the high speed ASIC applications. A modified model represents the concept of sub harmonic injection technique for PLL using auto aligned DLL. The phase noise of designed architecture with auto aligned injection at 1 MHz reference offset is 122.31dBc/Hz with RMS jitter of 127fs for 7.5GHz frequency. The total DC power dissipation is 13.99mW.

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