DESIGN OF LOW NOISE AMPLIFIER (LNA) USING ACTIVE AND PASSIVE TRANS-CONDUCTANCE BOOSTING CIRCUIT

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Abstract

In high-speed networks and applications of wireless communication systems, the wideband data transmission system needs to receive the signal with low noise and low power. The Low Noise Amplifier (LNA) improves the signal strength and amplify the signal at the receiver side to reduce the noise and also must work in the high speed switching activity. In the paper work, a low power and low noise with inductor-less active and passive model of trans-conductance (G_m) enhancement system in the 22nm CMOS technology. By using this type of CMOS technology, it reduces the power consumption due to the update channel width and circuit design of G_m enhancement. This paper also highlights in the reduction of overall area consumption with the alignment and other connectivity of amplifier. This amplifier was tested in both e-band and w-band operating frequencies to validate the noise level in high frequency applications. The result analysis and comparison chart shows the performance level of proposed LNA model than other state-of-art models.

Keywords:

Low Noise Amplifier, Trans-Conductance Enhancement, CMOS, High Frequency Applications

1. INTRODUCTION

In wireless communication system the wideband radio frequency receiver requires to enhance the signal to reduce the noise level present in the received signal. For that purpose, the Low Noise Amplifier (LNA) was designed to improve the amplifier gain at high frequency. For the designing of LNA, researchers consider the power consumption and the number of components usage that reduce the complexity of that overall system. Most of the designs are implemented in the CMOS switching technologies that can active at high frequency. In that, the gate controlling made according to that frequency for the switching with signal. In LNA, the power dissipation and consumption can be reduce and enhance the performance by the parameters of active and passive components connected with the amplifier circuit.

In real time application, these LNA were used in the wireless communication system like imaging application, and other high frequency radio signal operating devices. In that, the devices are placed in the low power unit and need to sustain the battery life for long time. Thus the development of LNA focused in the low power with minimum voltage as for VDD. To integrate more components into the chip and for the small size device, the area consumption for the design work of LNA also considering as the parameter to enhance the LNA system. For this process there are several methods to improve the quality of LNA system and reduce the noise level at high frequency operating point. Since there are some limitations in those existing designs like some can manage the power consumption and some can handle noise regulation at high frequency, etc. were need to consider in

account for the designing work of an LNA for W-band and E-band application.

The main contribution of this paper is

1. To design the LNA for W-band and E-band applications with minimum amount of noise figure.
2. Reduce the noise in dB range by the design work of G_m-boosting system with the active and passive models in 22nm CMOS technology.
3. To reduce the power consumption and design by inductor less circuit and test with the amplification process.
4. To reduce the area size of the overall design with minimum number of components in the overall device unit.

The paper work and its designs description has been organized as following sections: The related work discussion is presented in section 2 and proposed work of Active and passive G_m-boosting design was discussed in section 3. In section 4, discussed about the result and comparative study of proposed LNA design with other state-of-art designs that concludes the performance of overall proposed LNA design work and section 5, state about the conclusion and future enhancement of this paper.

2. RELATED WORK

In this section, survey about the existing system that they have developed the LNA in different architecture and in different type of CMOS technologies.

In [1], author proposed CCC cascade common gate amplifier for the Ultra-wideband application in the 0.18 um CMOS technology. The operating frequency is in the range of 3.1 to 10.6GHz. This design consumes the power upto 4.34mW. To reduce the power consumption, [2] proposed an enhanced linearity design for LNA. Since, this is applicable for the GSM bands in the range of 1.86 to 2.4GHz. To improve the wide band range, [3] proposed a W-band CMOS LNA with 29dB gain and with minimum noise for mm-wave imaging applications. In [4], author proposed 22 nm FDSOI with low Noise Figure and low power consumption. In this, the LNA was constructed in 3-stage cascade model to reduce the noise at high frequency. This can reduce the noise up to ~3dB at the frequency range of maximum 43GHz. In [5], capacitive neutralization technique is used to compensate the source-drain parasitic of input stage and boost loop gain of the trans-conductor. This was implemented in the TSMC 28 nm CMOS technology. The operating frequency of this system is in the range of 2~9.6GHz. In [6], tunable negative-feedback capacitor technology was implemented to get variable gain in the range of 4dB to 10dB for the frequency of 2.8GHz.

The Two stage compact wideband flat gain low noise amplifier is proposed in [7]. This was developed with the self-

biased active inductor in compact size. In this, the feedforward path creates another feedback loop that generates the negative capacitance of the circuit. To reduce the area consumption and to eliminate the inductor in circuit, [8] proposed current source loads, common-mode feedback (CMFB), asymmetric capacitive cross-coupling (CCC) and auxiliary common source amplifier to achieve low noise. Since the operating frequency of this LNA design is 0.18 to 2GHz range. To further improve the operating frequency for other wide band application, [9] implemented G_m-Boosting model with transformers for the enhancement of stability in amplifier. This works in the frequency range of 24.9 to 32.5GHz. Even the transform increases the operating frequency, it increase power and area consumption of the amplifier. To improve the performance of LNA, [10] proposed common gate transistor of 65-nm CMOS for the Ka-band application with the frequency range of 30 to 34.5GHz. Here, the phase compensation was achieved by introducing a shunt PMOS and parallel resistor in the common gated differential amplifier output terminal. In the LNA circuit the characteristics may vary with the Electrostatic Discharge (ESD). This can be reduce by stacked diodes with embedded silicon controlled rectifier design [11]. This SCR based power clamping method is tested for the K-band frequency. For the automotive radar application, the operating frequency must be in high range nearly 77GHz. For this process, [12] proposed a compact and high linearity CMOS receiver which is implemented in the TSMC 65nm technology.

In [13], double neutralized LNA technique is used for the high frequency application in the range of 60 to 90GHz. This was achieved by partially distributing the center frequency over three stages. In [14], author proposed active feedback and pole-zero adjustment for noise shaping in the LNA design. In this circuit parameters are updated according to the equation framed for the corresponding transfer function of gain and noise. The parameters are selected according to the feedback model. With this technique of active feedback, [15] proposed derivative superposition (DS) and complementary derivative superposition (CDS) techniques. In this, the low power design was achieved by biasing the transistors in threshold voltage and forward body biasing. In [16], paper work integrates a Trans-impedance Amplifier (TIA), Continuous-Time Linear Equalizer (CTLE), high gain and high bandwidth Limiting Amplifier (LA), and Clock and Data- Recovery (CDR) into a single die. This achieved the Bit Error Rate (BER) is less than 1e-12 by the Automatic Gain Control (AGC) scheme of architecture.

A Q-enhanced inductors were used in [17] to improve the power gain in amplifier. This was designed by using an in-phase current returning path (CRP) technique. In the operational amplifier, fully depleted silicon on insulator (FDSOI) CMOS process are presented in the 22nm CMOS technology for both single stage and two stage design of amplifier in [18]. This reduces the power consumption while driving a 1pF capacitive load. To further reduce the power consumption, [19] proposed forward body bias technique in the 0.13 um CMOS technology. A V-band LNA was designed by the G_m-boosting technique with the Noise Figure (NF) transformer to improve the gain for high operating frequency in the range of 57.1GHz in [20]. Also for the E-band and W-band application in the frequency range of 77 to 94GHz, [21] proposed the gain-boosting with transform in the 22nm CMOS technology.

From the survey of various techniques for the LNA design, the trans-conductance (G_m) boosting technique improves the stability factor of amplifier. This is also effective for high frequency applications that utilize E-band and W-band signal range. In this proposed work, the G_m-boosting is implemented in the 22nm CMOS technology. To further improve the performance, this G_m-boosting is integrating with the Active and passive components for making the inductor less circuit. This will reduce the power consumption and improve the gain of amplifier than other existing methods. The detailed description about the proposed work are in following sections.

3. PROPOSED WORK

This section explains the detailed design of proposed enhancement work in LNA design. In the proposed design, the active and passive G_m-boosting model with inductor less circuit was framed in the 22nm CMOS technology. As we seen in the literature survey, the G_m-boosting model were implemented with the combination of inductive transformer. In that, the transformer helps to improve the sensitivity if the system at high frequency. But, this may consume high power and also increase the space of circuit. In this paper, the circuit is framed by the N-type of CMOS connected with the resistor and capacitors circuit. Here, the resistors are neglected and implemented the capacitor coupled circuit design.

This amplifier was designed in the single stage amplifier driven by the two N-type component powered with the current source to enhance the switching activity. Here, the switches are activated in the high frequency input and the minimum amount of V_{DD} connected as the power source for the circuit. The circuit design for the proposed work is shown in the Fig.1 with the specified parameters of LNA. This proposed circuit was implemented in the Tanner EDA tool and the waveforms of LNA output are analyzed with the W-Edit of it.
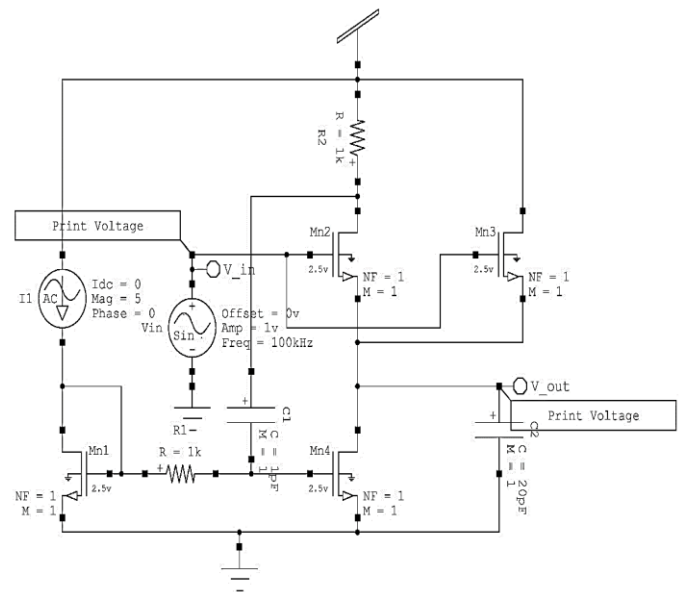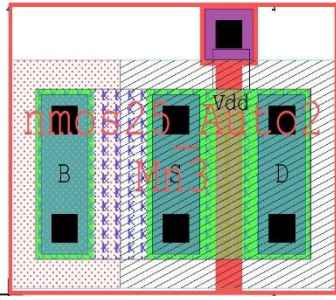

Fig.1. Circuit Diagram of Proposed LNA

Fig.2. Layout design of 22 nm CMOS

The Fig.2 shows the layout design of 22nm CMOS N-type model. This can be export to the L-Edit tool of tanner that scales the layer in the CMOS. In that, each color code represents the different material to design the layout structure. In that, the black color represents the Active / Poly contact point that connects the material of Active layer, P-select and other layers. Finally, the Poly layer is used to form as a terminal point.

The overall design layout can be construct and test with the voltage source connected to the terminal point. For the proposed LNA, the effective trans-conductance can be representing as $1+A$. According to the circuit in the Fig.1, 'A' can be estimate as

$$A = \frac{C_1}{C_1 + C_{gs}} \qquad (1)$$

where, C_1 is the Capacitor and C_{gs} is the Capacitance across Gate to Source of the CMOS

The circuit can be describing as, the 'M_{n1}' source connected to the V_{DD} voltage source and the Drain to the ground. This was driven by the Capacitor 'C_1' along with the V_{DD} connected at the Gate Terminal. The 'R_1' resistor balance the current flow at the gate terminal. The CMOS 'M_{n2}' and 'M_{n3}' are connected in parallel which are driven by the input voltage source 'V_1'. This was protected by the CMOS 'M_{n4}' this is serially connected to the drain of 'M_{n2}'. The output terminal is coupled by the capacitor 'C_2' to reduce the noise at output.
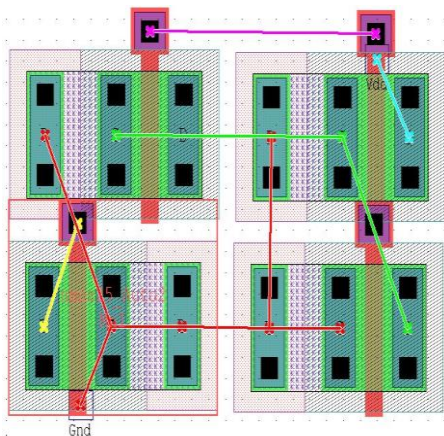

Fig.3. Overall Layout design of proposed LNA

The overall layout design of the proposed LNA is shown in the Fig.3. This shows the arrangement of the CMOS and other connectivity details between the components. The color code represents the legend of each terminal point represented in the circuit diagram. In this layout design, the scale for each grid is

represent in the size of microns. From the scale size we can estimate the area of layout is $6 \times 5 \mu m^2$, which represent that the proposed work achieved reduction in the area consumption better than the other existing design of LNA model. Finally, this L-Edit layout is exported as the spice code and processed in the T-Spice for visualization and analysis report. The results of the active and passive G_m-boosting model is described briefly in the section 4 with comparison statement and other parameter validation.

4. RESULT ANALYSIS

This section analyses the performance of proposed work and compare the parameters to other existing method of [21]. The testing and simulation are processed in the Tanned EDA tool of version 16p3. The parameters that considered for the comparative analysis are

• Noise in (dB),

• Power in (mW),

• Voltage source V_{DD} in (V) and

• Area consumption in (mm^2).

All these parameters are simulated and estimated from the Tanner tool such as the Noise Figure can be estimate by using the FFT analysis in W-Edit, Add and power consumption can be measured from the T-Spice report generator and the area consumption can be measured from the L-Edit tool.

The Table.1 shows the comparison parameter analysis for the proposed work with existing model of FD-SOI. It represents that the frequencies used for the testing are 77 and 92GHz (W-band and E-band frequency range). This table presented for the parameters of V_{DD}, power and area. It shows that the proposed work reduces the power and area consumption better than the existing method of FD-SOI.

Table.1. Comparison Table of proposed and FD-SOI

Methods	Frequency (GHz)	V_{DD}	P_{dc} (mW)	Area (mm^2)
Existing (FD-SOI)	77	1	9	0.35
	77	1.6	16	0.35
	92	1.6	16	0.43
Proposed (G_m method)	77	1	1.612	0.04875
	77	1.6	2.746	0.04875
	92	1.6	2.811	0.05775

The Fig.4 shows the power report exported from the T-Spice tool which gives the average power consumption for the overall circuit design of LNA. This shows that the maximum power consumption for the proposed work is of about 6.856e^{-13} watts at time 0.9984ms from input voltage source and 5.3528e^{-10} watts at time 0.5.06875µs from V_{DD} voltage source at the frequency level of 100MHz.

At the frequency range of 77GHz and 92GHz, the power is estimated as 2.746mW and 2.811mW for the V_{DD} of 1.6 volts. The Fig.5(a) and Fig.5(b) shows the waveform result from the amplifier. In that, the red color waveform indicates the input signal and the green color waveform represent the output signal of amplifier.
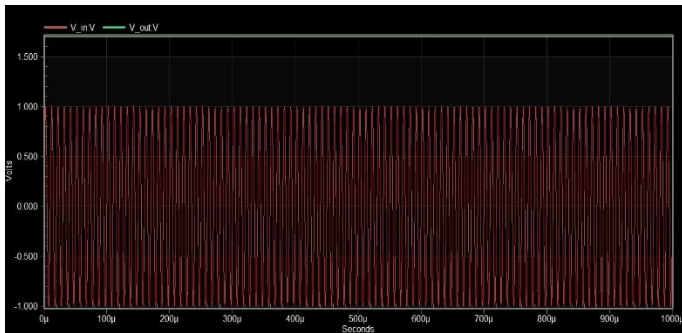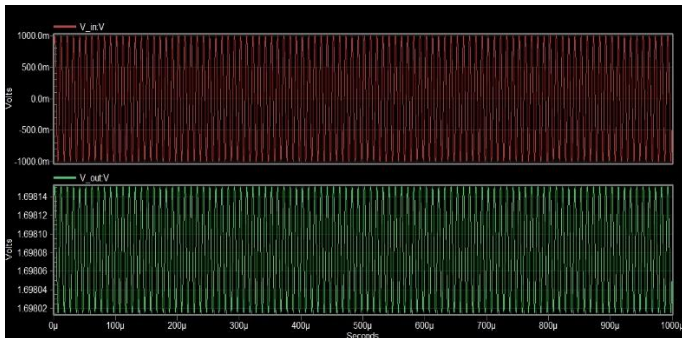
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Power Results

VVin from time 0 to 0.001
Average power consumed -> 6.85551le-013 watts
Max power 1.882935e-009 at time 0.000998469
Min power 0.000000e+000 at time 0

VV2 from time 0 to 0.001
Average power consumed -> 5.352841e-010 watts
Max power 1.079888e-008 at time 5.06875e-006
Min power 3.293575e-010 at time 2.46875e-006
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Fig.4. Power Analysis Report

(a)

(b)

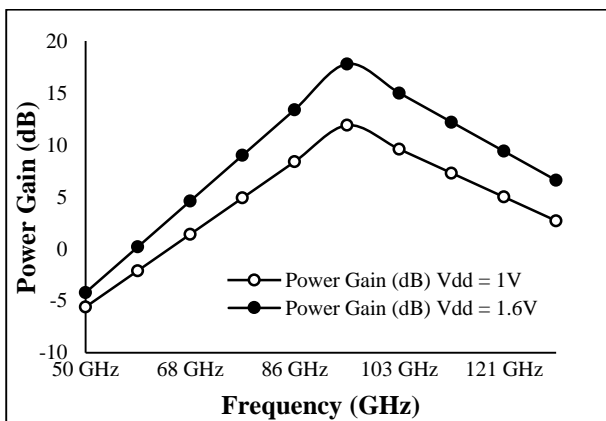Fig.5. Waveform of LNA output (a) Input and output are in same axes (b) Splitted axes

Fig.6. Power Gain chart

From the Fig.6, it shows the power gain chart for the two different source of V_{DD} (1V and 1.6V). It shows the power gain is improved in the proposed work raised upto maximum of ~18dB in range. The peak reaches at the frequency of 94GHz represents that compare to the existing work, the G_m-boosting

method enhanced the signal strength and stability of the system of LNA.

5. CONCLUSION AND FUTURE ENHANCEMENT

This paper proposed an enhanced design of Low Noise amplifier for the high frequency application in W-band and E-band frequency range. This integrates the active and passive Gm (trans-conductance) boosting with inductor less circuit. The main focus of this paper work is to reduce the noise level by improving the power gain (dB). The comparison result presents that the proposed design of LNA achieved high gain for the high frequency application. This also reduce the power consumption and area utilization compare to the existing design of FD-SOI in 22 nm CMOS technology. This concludes that the active passive Gm-boosting technique performs better than other existing methods of LNA.

In future, this type of enhanced work can be implement with different CMOS technology and retrieve the analysis report of that design.

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